Claims:

1. A method of fabricating an interconnect structure comprising:

forming a conductive line;

forming a first capping layer selectively over the conductive line and a dielectric layer;

forming a dielectric barrier layer over the dielectric layer and over the first capping layer;

forming a low-k layer over the first capping layer;

exposing the conductive line including forming a mask layer having an opening over the low-k layer,

narrowing the opening in the mask layer, and

forming a via by extending the narrowed opening through the low-k layer at least to the first capping layer;

forming a first diffusion barrier layer on sidewalls of the via; and

filling the via with a first conductive material.

2. The method of claim 1 wherein forming the conductive line includes

forming the dielectric layer

defining a first trench in the dielectric layer, and

filling the first trench with a second conductive material.

3. The method of claim 2 wherein forming the dielectric layer comprises depositing an organosilicate glass.

4. The method of claim 2 wherein forming the conductive line includes forming a second diffusion barrier layer within the first trench.

5. The method of claim 1 wherein forming the dielectric barrier layer comprises depositing silicon carbide, silicon nitride, or silicon carbon nitride.

6. The method of claim 1 wherein forming the via includes extending the narrowed opening through the first capping layer to the conductive line.

7. The method of claim 1 wherein forming the first capping layer includes electroless plating of cobalt or a cobalt-alloy.

8. The method of claim 1 wherein forming the low-k layer includes depositing an organosilicate glass.

9. The method of claim 1 wherein forming the mask layer includes depositing a photoresist layer and forming the opening in the photoresist layer.

10. The method of claim 9 wherein forming the mask layer includes forming a hard mask layer before forming the photoresist layer.

11. The method of claim 1 wherein narrowing the opening includes forming a conformal deposition layer on sidewalls of the opening.

12. The method of claim 11 wherein forming the conformal deposition layer includes cycling between deposition and etching.

13. The method of claim 1 wherein forming the first diffusion barrier layer includes atomic layer deposition of ruthenium.

14. The method of claim 1 wherein forming the first diffusion barrier layer includes atomic layer deposition of tantalum.

15. The method of claim 1 wherein forming the first diffusion barrier layer includes supercritical CO_2 deposition of ruthenium.

16. The method of claim 1 wherein forming the first diffusion barrier layer includes supercritical CO_2 deposition of tantalum.

17. The method of claim 1 wherein forming the first diffusion barrier layer includes depositing a metal by a method selected from the group consisting of chemical vapor deposition, plasma-enhanced chemical vapor deposition, and plasma-enhanced atomic layer deposition.

18. The method of claim 1 further comprising, after forming the via and before forming the first diffusion barrier layer, forming a second trench in the low-k layer, the trench being aligned with the via.

19. The method of claim 18 wherein forming the first diffusion barrier layer on sidewalls of the via includes forming the first diffusion barrier layer on sidewalls of the second trench.

20. The method of claim 18 wherein filling the via with the second conductive material includes filling the second trench with copper.

21. The method of claim 1 further comprising forming a second capping layer selectively over the via.

22. A method of fabricating an interconnect structure, comprising:

forming a first conductive line in a dielectric layer;

forming a first capping layer selectively over the conductive line;

forming a low-k layer over the first capping layer and in contact with the dielectric layer;

forming a dielectric barrier layer over the dielectric layer and over the first capping layer;

exposing the conductive line including

forming a mask layer having an opening over the low-k layer,

narrowing the opening in the mask layer, and

forming a via by extending the narrowed opening through the low-k layer and the first capping layer and to the first conductive line;

forming a first diffusion barrier layer on sidewalls of the via; and

filling the via with a first conductive material.

23. The method of claim 22 further comprising forming a second conductive line in the low-k layer.

24. The method of claim 23 further comprising forming a second capping layer selectively over the second conductive line.

25. The method of claim 22 wherein forming the first conductive line in the dielectric layer includes forming a second diffusion barrier layer in the dielectric layer.

CLAIMS

What is claimed is:

1. A method of fabricating an interconnect structure comprising:

forming a conductive line;

forming a first capping layer selectively over the conductive line;

forming a low-k layer over the first capping layer;

exposing the conductive line including

forming a mask layer having an opening over the low-k layer,

narrowing the opening in the mask layer, and

forming a via by extending the narrowed opening through the low-k layer at least to the first capping layer;

forming a first diffusion barrier layer on sidewalls of the via; and

filling the via with a first conductive material.

2. The method of claim 1 wherein forming the conductive line includes

forming a dielectric layer,

defining a first trench in the dielectric layer, and

filling the first trench with a second conductive material.

3. The method of claim 2 wherein forming the dielectric layer comprises depositing an organosilicate glass.

4. The method of claim 2 wherein forming the conductive line includes forming a second diffusion barrier layer within the first trench.

5. The method of claim 1 further comprising forming a dielectric barrier layer over the dielectric layer and over the first capping layer and forming the via includes extending the narrowed opening through the dielectric barrier layer.

6. The method of claim 5 wherein forming the dielectric barrier layer comprises depositing silicon carbide, silicon nitride, or silicon carbon nitride.

7. The method of claim 1 wherein forming the via includes extending the narrowed opening through the first capping layer to the conductive line.

8. The method of claim 1 wherein forming the first capping layer includes electroless plating of cobalt or a cobalt-alloy.

9. The method of claim 1 wherein forming the low-k layer includes depositing an organosilicate glass.

10. The method of claim 1 wherein forming the mask layer includes depositing a photoresist layer and forming the opening in the photoresist layer.

11. The method of claim 10 wherein forming the mask layer includes forming a hard mask layer before forming the photoresist layer.

12. The method of claim 1 wherein narrowing the opening includes forming a conformal deposition layer on sidewalls of the opening.

13. The method of claim 12 wherein forming the conformal deposition layer includes cycling between deposition and etching.

14. The method of claim 1 wherein forming the first diffusion barrier layer includes atomic layer deposition of ruthenium.

15. The method of claim 1 wherein forming the first diffusion barrier layer includes atomic layer deposition of tantalum.

16. The method of claim 1 wherein forming the first diffusion barrier layer includes supercritical CO_2 deposition of ruthenium.

17. The method of claim 1 wherein forming the first diffusion barrier layer includes supercritical CO_2 deposition of tantalum.

18. The method of claim 1 wherein forming the first diffusion barrier layer includes depositing a metal by a method selected from the group consisting of chemical vapor deposition, plasma-enhanced chemical vapor deposition, and plasma-enhanced atomic layer deposition.

19. The method of claim 1 further comprising, after forming the via and before forming the first diffusion barrier layer, forming a second trench in the low-k layer, the trench being aligned with the via.

20. The method of claim 19 wherein forming the first diffusion barrier layer on sidewalls of the via includes forming the first diffusion barrier layer on sidewalls of the second trench.

21. The method of claim 19 wherein filling the via with the second conductive material includes filling the second trench with copper.

22. The method of claim 1 further comprising forming a second capping layer selectively over the via.

23. An interconnect structure comprising:

a conductive line having a critical dimension of no more than 60nm;

a first dielectric layer disposed over the conductive line;

a first capping layer disposed between the first dielectric layer and the conductive line and disposed selectively over the conductive line;

a conductive via disposed through the first dielectric layer and at least to the first capping layer; and

a diffusion barrier layer disposed between the conductive via and the first dielectric layer.

24. The interconnect structure of claim 23 wherein the first capping layer comprises cobalt.

25. The interconnect structure of claim 23 wherein the diffusion barrier layer comprises ruthenium.

26. The interconnect structure of claim 23 wherein the diffusion barrier layer comprises tantalum.

27. The interconnect structure of claim 23 further comprising a second dielectric layer disposed around the conductive line.

28. The interconnect structure of claim 27 further comprising a dielectric barrier layer disposed between the first and second dielectric layers.

29. The interconnect structure of claim 23 further comprising a dielectric barrier layer disposed over the first dielectric layer, the conductive via being disposed through the dielectric barrier layer.

30. The interconnect structure of claim 29 wherein the dielectric barrier layer comprises silicon carbide, silicon nitride, or silicon carbon nitride.

31. The interconnect structure of claim 23 further comprising a second capping layer disposed over the conductive via.

32. An interconnect structure comprising:

a first conductive line disposed within a first dielectric layer;

a second dielectric layer disposed over the first conductive line and contacting the first dielectric layer;

a first capping layer disposed between the second dielectric layer and the first conductive line;

a conductive via disposed through the second dielectric layer and at least to the first capping layer; and

a first diffusion barrier layer disposed between the conductive via and the second dielectric layer.

33. The interconnect structure of claim 32 further comprising a second diffusion barrier layer disposed between the first conductive line and the first dielectric layer.

34. The interconnect structure of claim 32 wherein the first diffusion barrier layer comprises ruthenium.

35. The interconnect structure of claim 32 wherein the first diffusion barrier layer comprises tantalum.

36. The interconnect structure of claim 32 further comprising a second conductive line disposed within the second dielectric layer, wherein the conductive via contacts the second conductive line.

37. The interconnect structure of claim 36 further comprising a second capping layer disposed selectively over the second conductive line.

38. The interconnect structure of claim 32 wherein the conductive via is disposed through the first capping layer and to the first conductive line.

39. A method of fabricating an interconnect structure comprising:

forming a first conductive line in a dielectric layer;

forming a first capping layer selectively over the first conductive line;

forming a low-k layer over the first capping layer and in contact with the dielectric layer;

exposing the conductive line including

forming a mask layer having an opening over the low-k layer,

narrowing the opening in the mask layer, and

forming a via by extending the narrowed opening through the low-k layer and at least to the first capping layer;

forming a first diffusion barrier layer on sidewalls of the via; and

filling the via with a first conductive material.

40. The method of claim 39 wherein extending the narrowed opening at least to the first capping layer includes extending the narrowed opening through the first capping layer and to the first conductive line.

41. The method of claim 39 further comprising forming a second conductive line in the low-k layer.

42. The method of claim 41 further comprising forming a second capping layer selectively over the second conductive line.

43. The method of claim 39 wherein forming the first conductive line in the dielectric layer includes forming a second diffusion barrier layer in the dielectric layer.