FIG. 1A

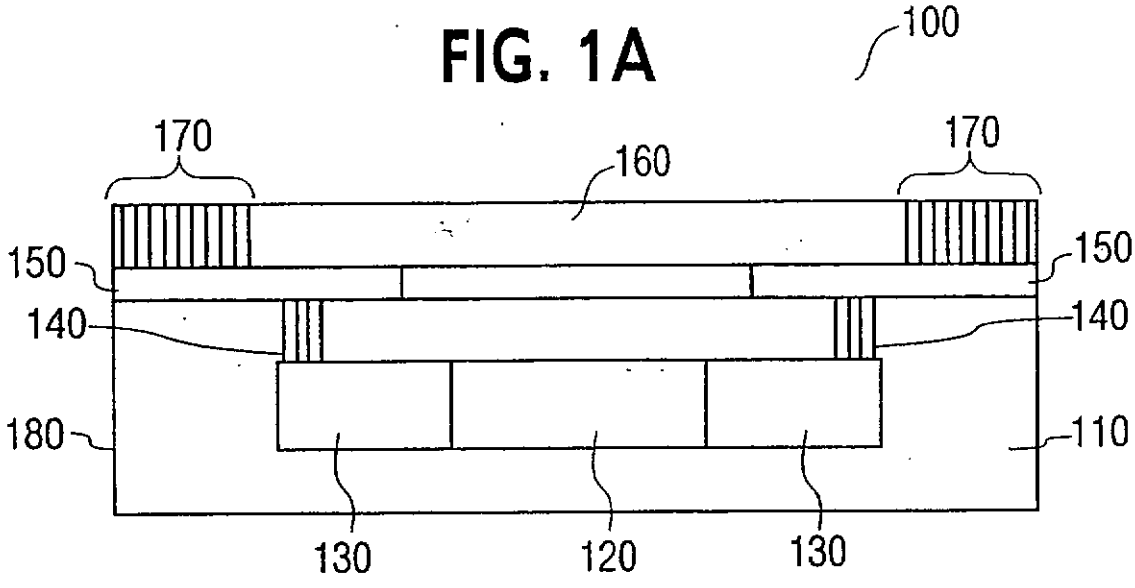

100
170
160
170
150
150
140
140
180
110
130
120
130

FIG. 1B

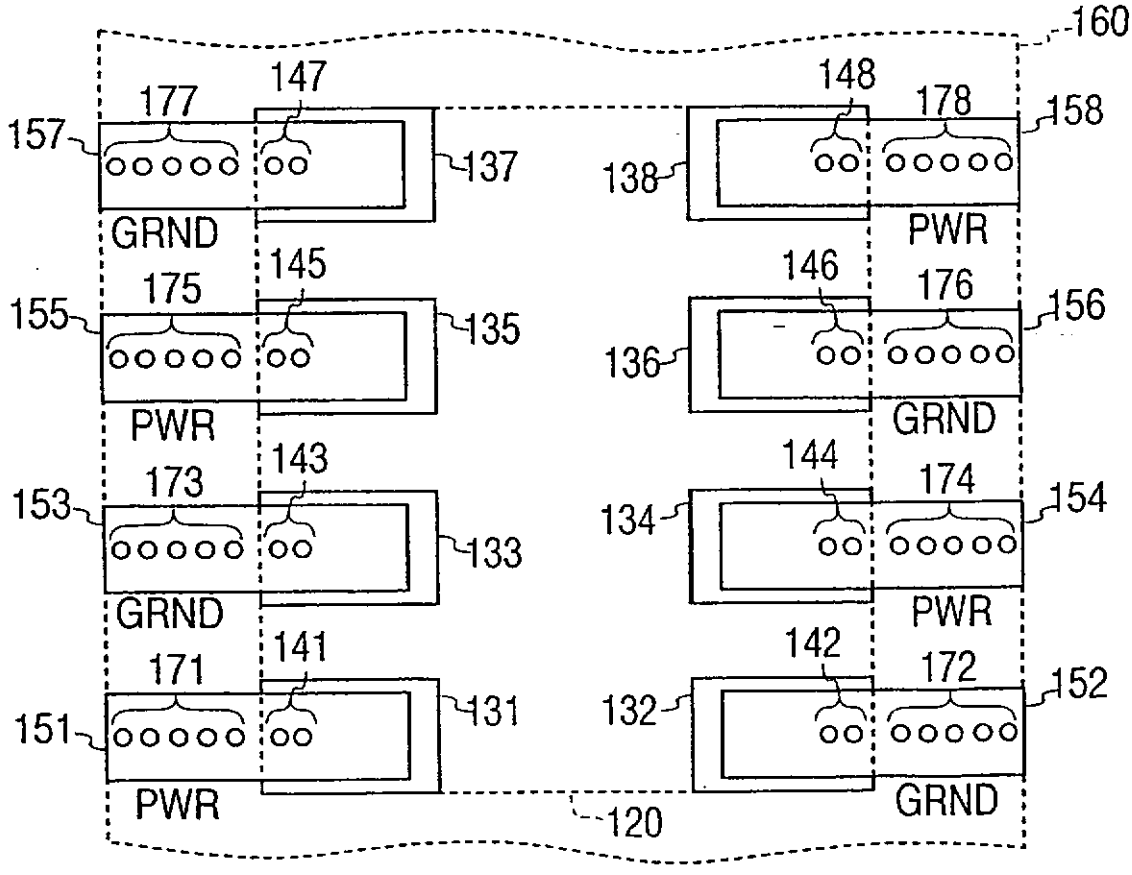

160
177
147
148
178
157
158
137
138
GRND
PWR
175
145
146
176
155
156
135
136
PWR
GRND
173
143
144
174
153
154
133
134
GRND
PWR
171
141
142
172
151
152
131
132
PWR
GRND
120

FIG. 2A

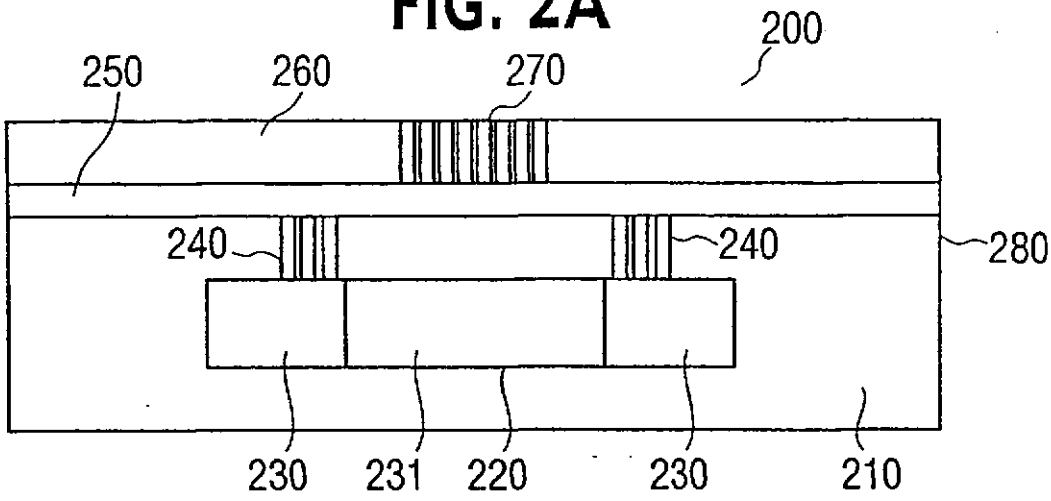

200
250
260
270
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240
280
230
231
220
230
210

FIG. 2B

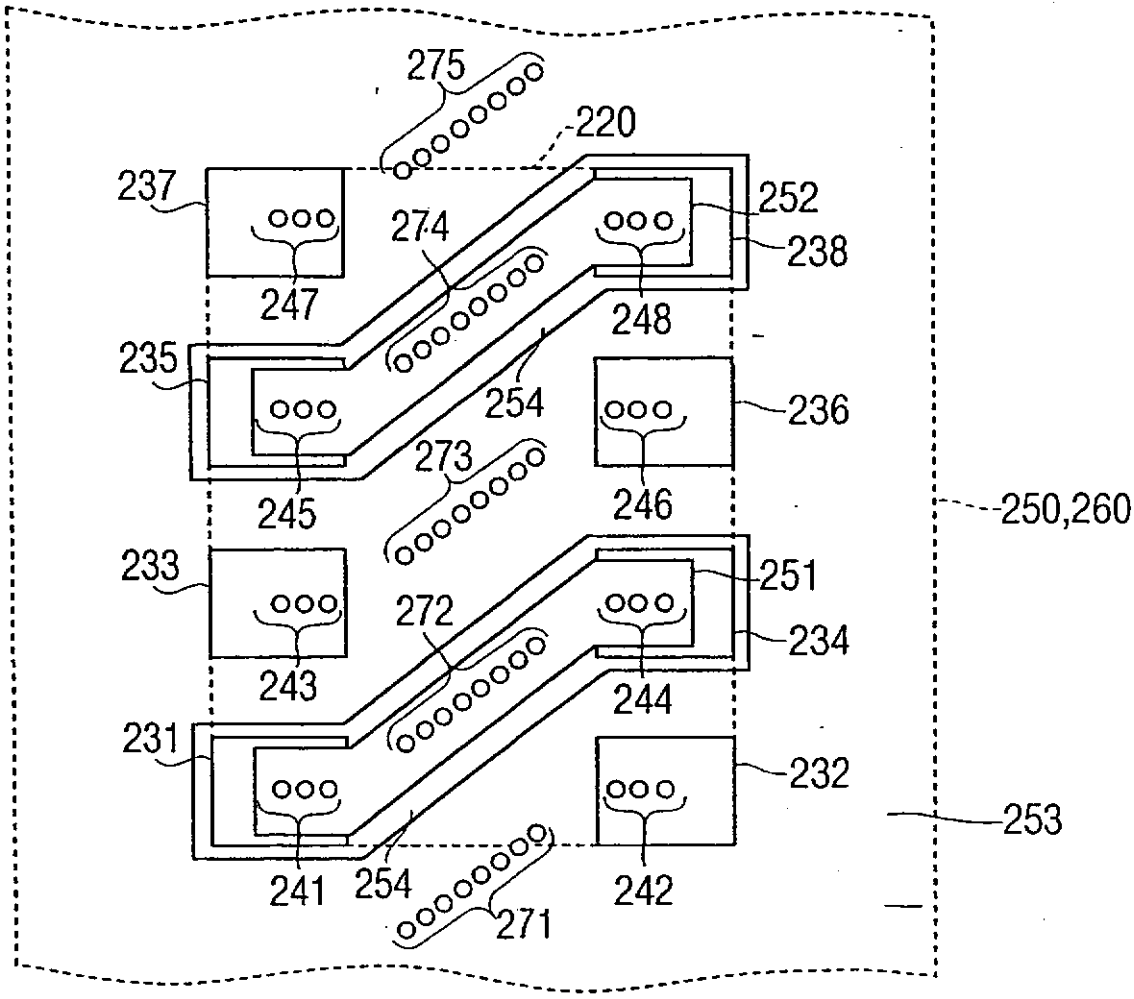

275
220
237
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274
252
238
248
235
254
236
245
273
246
250,260
233
243
272
251
234
244
231
241
254
232
253
242
271

FIG. 3

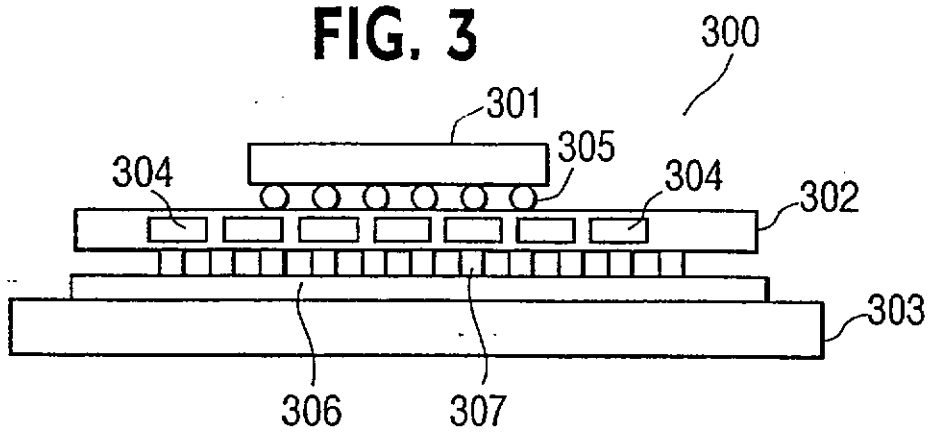


FIG. 4

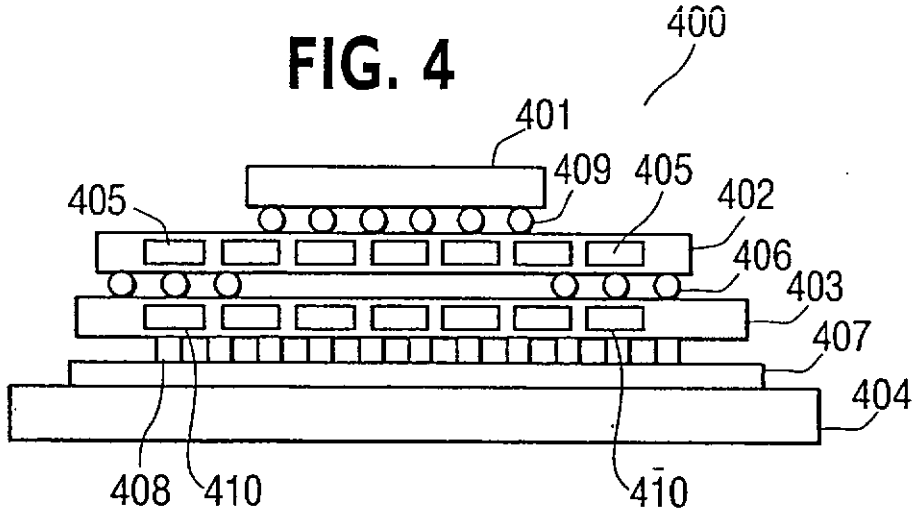


FIG. 5

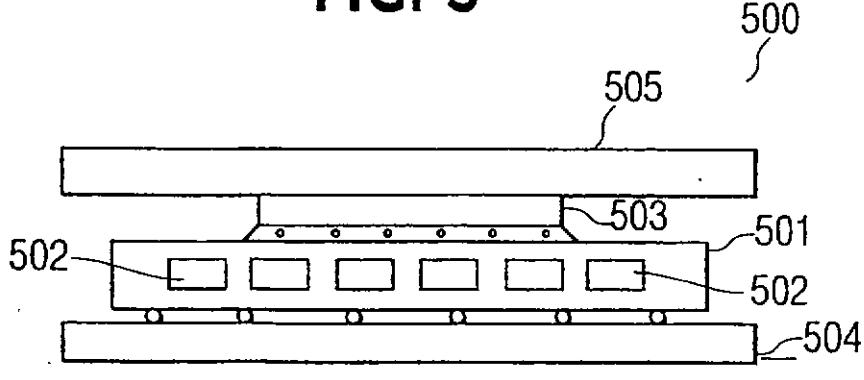


FIG. 6

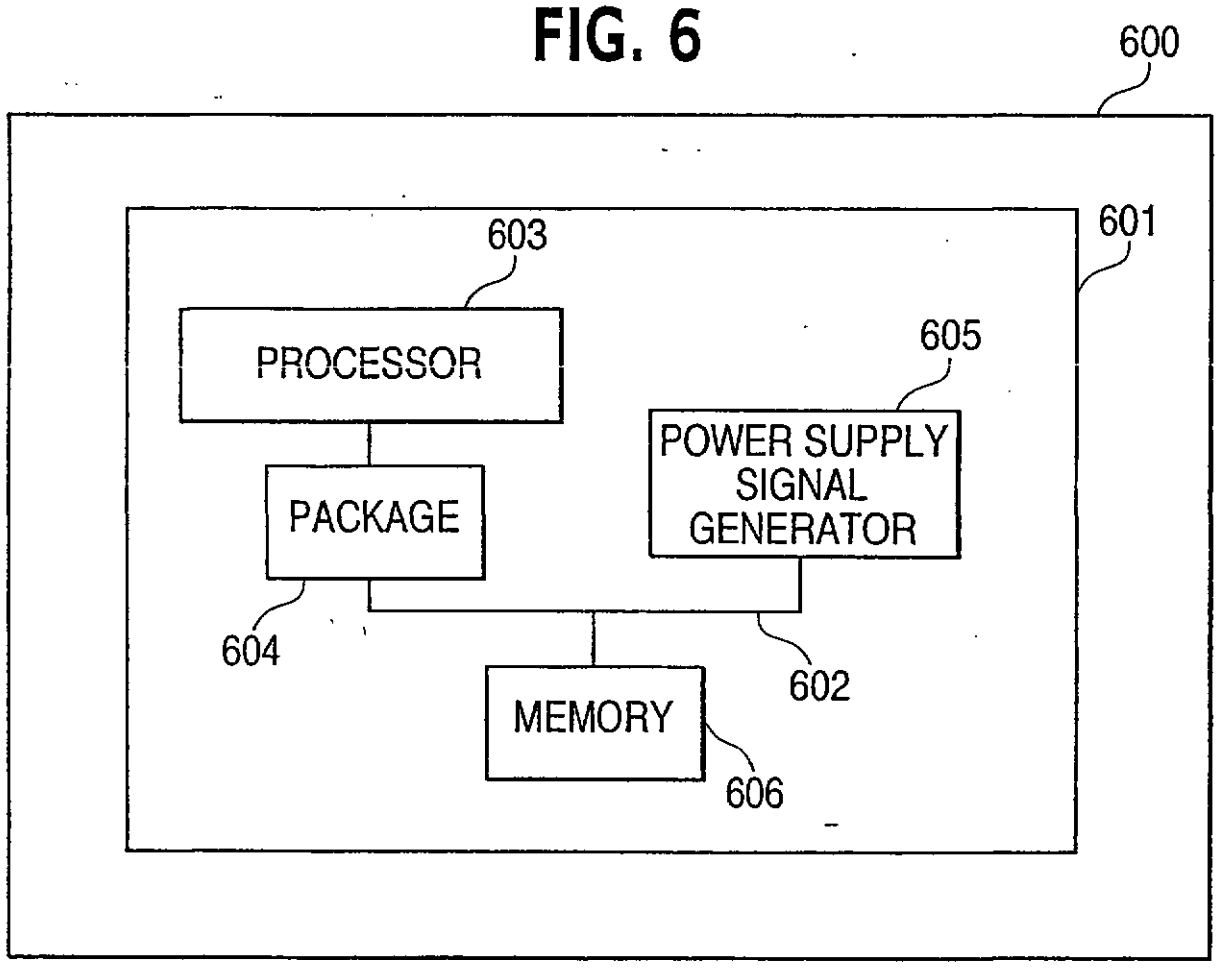
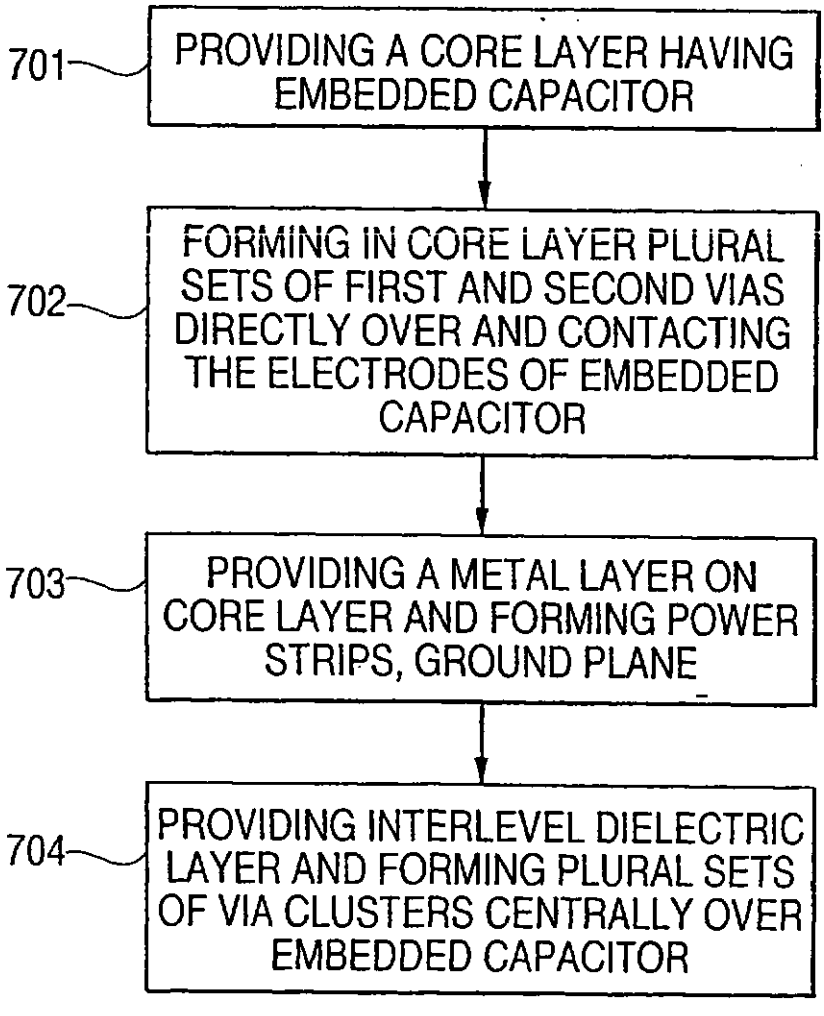

600
601
603
PROCESSOR
605
POWER SUPPLY SIGNAL GENERATOR
PACKAGE
604
602
MEMORY
606

FIG. 7


701
PROVIDING A CORE LAYER HAVING EMBEDDED CAPACITOR
702
FORMING IN CORE LAYER PLURAL SETS OF FIRST AND SECOND VIAS DIRECTLY OVER AND CONTACTING THE ELECTRODES OF EMBEDDED CAPACITOR
703
PROVIDING A METAL LAYER ON CORE LAYER AND FORMING POWER STRIPS, GROUND PLANE
704
PROVIDING INTERLEVEL DIELECTRIC LAYER AND FORMING PLURAL SETS OF VIA CLUSTERS CENTRALLY OVER EMBEDDED CAPACITOR