CLAIMS

1. A method, comprising:

during a first time period, transferring first charge carriers from a first charge storage region to a second charge storage region; and

during a second time period:

receiving second charge carriers at the first charge storage region; and

reading out the first charge carriers from the second charge storage region.

2. The method of claim 1, wherein:

the first and second charge carriers are generated in a photodetection region in response to arrival of incident photons at the photodetection region;

before the first time period, the first charge carriers are received at the first charge storage region from the photodetection region; and

during the second time period, the second charge carriers are received at the first charge storage region from the photodetection region.

3. The method of claim 2, wherein:

over multiple sub-periods within the second time period, the second charge carriers are received at the first charge storage region; and

each sub-period within the second time period follows a respective excitation of a sample that causes the sample to emit the incident photons.

4. The method of claim 2 or 3, wherein:

the second charge carriers are received at the first charge storage region from the photodetection region via a first charge transfer channel that connects the photodetection region to the first charge storage region; and

the first charge carriers are transferred from the first charge storage region to the second charge storage region via a second charge transfer channel that connects the first charge storage region to the second charge storage region.

~~5. The method of claim 2, wherein:~~

~~the second charge carriers are received at the first charge storage region from the photodetection region via a first charge transfer channel that connects the photodetection region to the first charge storage region; and~~

~~the first charge carriers are transferred from the first charge storage region to the second charge storage region via:~~

~~a second charge transfer channel that connects the first charge storage region to an intermediate charge storage region;~~

~~the intermediate charge storage region; and~~

~~a third charge transfer channel that connects the intermediate charge storage region to the second charge storage region.~~

~~6. The method of claim 5, wherein:~~

~~during a first sub-period of the second time period, the first charge carriers are read out from the second charge storage region to a readout region; and~~

~~during a second sub-period of the second time period, third charge carriers are read out from the intermediate charge storage region to the readout region via the second charge storage region.~~

~~7~~5. The method of any one of claims 1-4, wherein reading out comprises transferring the first charge carriers from the second charge storage region to a readout region to be sampled.

~~8~~6. An integrated circuit controllable to perform the method of any one of claims 1-5, the integrated circuit comprising:

a photodetection region configured to generate charge carriers in response to receiving incident photons;

a first charge storage region electrically coupled to the photodetection region to receive charge carriers; and

a second charge storage region electrically coupled to the first charge storage region to receive charge carriers~~,~~

~~wherein the integrated circuit is configured to read out charge carriers from the second charge storage region while the first charge storage region receives charge carriers from the photodetection region~~.

~~9~~7. The integrated circuit of claim ~~8~~6, wherein the integrated circuit is ~~configured~~ controllable to induce a potential barrier between the first and second charge storage regions while the first charge storage region receives charge carriers from the photodetection region and the second charge storage region reads out charge carriers.

~~10~~8. The integrated circuit of claim ~~9~~7, further comprising a first transfer gate positioned, at least in part, between the first and second charge storage region and configured to receive a first control signal that causes the first transfer gate to control the potential barrier between the first and second charge storage regions while the first charge storage region receives charge carriers from the photodetection region and the second charge storage region reads out charge carriers.

~~11~~9. The integrated circuit of claim ~~10~~8, further comprising:

a first charge transfer channel connecting the first charge storage region to the second charge storage region and configured to be biased by the first transfer gate to control the potential barrier between the first and second charge storage regions.

~~12~~10. The integrated circuit of claim ~~11~~9, further comprising:

a drain region electrically coupled to the photodetection region to receive charge carriers from the photodetection region;

a second transfer gate positioned, at least in part, between the photodetection region and the first charge storage region and configured to receive a second control signal that causes the second transfer gate to control a potential barrier between the photodetection region and the first charge storage region while the drain region receives charge carriers from the photodetection region; and

a second charge transfer channel connecting the photodetection region to the first charge storage region and configured to be biased by the second transfer gate to control the potential barrier between the photodetection region and the first charge storage region.

~~13. The integrated circuit of claim 10, further comprising:~~

~~an intermediate charge storage region electrically coupled between the first and second charge storage regions;~~

~~a first transfer gate positioned, at least in part, between the first and intermediate charge storage regions and configured to receive a first control signal that causes the first transfer gate to control a potential barrier between the first and intermediate charge storage regions while the~~

first charge storage region receives charge carriers from the photodetection region and the intermediate and second charge storage regions read out charge carriers;

a first charge transfer channel connecting the first charge storage region to the intermediate charge storage region and configured to be biased by the first transfer gate to control the potential barrier between the first and intermediate charge storage regions;

a second transfer gate positioned, at least in part, between the intermediate and second charge storage regions and configured to receive a second control signal that causes the second transfer gate to control a potential barrier between the intermediate and second charge storage regions while the intermediate charge storage region receives charge carriers from the photodetection region via the first charge storage region and the second charge storage region reads out charge carriers; and

a second charge transfer channel connecting the intermediate charge storage region to the second charge storage region and configured to be biased by the second transfer gate to control the potential barrier between the intermediate and second charge storage regions.

14. The integrated circuit of claim 8, further comprising:

a readout region electrically coupled to the second charge storage region,

wherein the integrated circuit is configured to read out the first charge carriers from the second charge storage region by transferring the first charge carriers from the second charge storage region to the readout region to be sampled.

15. A system, comprising:

an integrated circuit, comprising:

a first charge storage region; and

a second charge storage region electrically coupled to the first charge storage region; and

a control circuit electrically coupled to the integrated circuit and configured to:

during a first time period, control the integrated circuit to transfer, from the first charge storage region to the second charge storage region, first charge carriers; and

during a second time period, control the integrated circuit to:

receive, at the first charge storage region, second charge carriers; and

read out, from the second charge storage region, the first charge carriers.

16. The system of claim 15, wherein:

the integrated circuit further comprises a photodetection region configured to, in response to receiving incident photons, generate the first and second charge carriers; and

the control circuit is configured to control the integrated circuit to:

before the first time period, transfer, from the photodetection region to the first charge storage region, the first charge carriers; and

during the second time period, transfer, from the photodetection region to the first charge storage region, the second charge carriers.

17. The system of claim 16, wherein the control circuit is configured to, over the course of multiple sub-periods within the second time period, control the integrated circuit to transfer, from the photodetection region to the first charge storage region, the second charge carriers, each sub-period within the second time period following a respective excitation of a sample that causes the sample to emit the incident photons.

18. The system of claim 16, wherein:

the integrated circuit further comprises:

a first transfer gate configured to control the transfer of charge carriers from the photodetection region to the first charge storage region; and

a second transfer gate configured to control the transfer of charge carriers from the first charge storage region to the second charge storage region; and

the control circuit is configured to:

apply a first signal to the first transfer gate to transfer charge carriers from the photodetection region to the first charge storage region; and

apply a second signal to the second transfer gate to transfer charge carriers from the first charge storage region to the second charge storage region.

19. The system of claim 16, wherein

the integrated circuit further comprises:

an intermediate charge storage region;

a first transfer gate configured to control the transfer of charge carriers from the photodetection region to the first charge storage region;

a second transfer gate configured to control the transfer of charge carriers from the first charge storage region to the intermediate charge storage region; and

~~a third transfer gate configured to control the transfer of charge carriers from the intermediate charge storage region to the second charge storage region; and~~

~~the control circuit is configured to:~~

~~apply a first signal to the first transfer gate to transfer charge carriers from the photodetection region to the first charge storage region; and~~

~~apply a second signal to the second transfer gate to transfer charge carriers from the first charge storage region to the intermediate charge storage region; and~~

~~apply a third signal to the third transfer gate to transfer charge carriers from the intermediate charge storage region to the second charge storage region.~~

~~20. The system of claim 15, wherein:~~

~~the integrated circuit further comprises a readout region; and~~

~~the control circuit is configured to, during the second time period, control the readout of the first charge carriers from the second charge storage region to the readout region to be sampled.~~

~~21~~11. ~~An~~ The integrated circuit of any one of claims 6-10, ~~comprising:~~

~~a photodetection region;~~

~~a first charge storage region; and~~

~~a second charge storage region,~~

~~wherein~~ the photodetection region and the first and second charge storage regions are configured to induce an intrinsic electrical field in a first direction from the photodetection region to the first charge storage region and from the first charge storage region to the second charge storage region.

~~22~~12. The integrated circuit of claim ~~21~~11, wherein:

the photodetection region has a first intrinsic electric potential level; and

the first charge storage region has a second intrinsic electric potential level that is different from the first intrinsic electric potential level.

~~23~~13. The integrated circuit of claim ~~22~~11, wherein:

the photodetection has a first pinning voltage; ~~and~~

the first charge storage region has a second pinning voltage that is different from the first pinning voltage; and~~.~~

~~24. The integrated circuit of claim 23, wherein~~

the second charge storage region has a third pinning voltage that is different from the first and second pinning voltages.

~~25~~14. The integrated circuit of claim ~~24~~11, wherein:

the photodetection region has a first dopant concentration of a first conductivity type;

the first charge storage region has a second dopant concentration of the first conductivity type that is higher than the first dopant concentration; and

the second charge storage region has a third dopant concentration of the first conductivity type that is higher than the second dopant concentration.

15. A system, comprising:

the integrated circuit of any one of claims 6-14; and

a control circuit configured to control the integrated circuit to perform the method of any one of claims 1-5.

~~26. The integrated circuit of claim 25, wherein the second charge storage region comprises:~~

~~a first doped sub-region having the third dopant concentration; and~~

~~a second doped sub-region having a fourth dopant concentration of the first conductivity type that is higher than the third dopant concentration, wherein the first charge storage region is positioned closer to the first doped sub-region in the first direction than to the second doped sub-region.~~

~~27. The integrated circuit of claim 26, further comprising a readout region spaced from the second charge storage region in the first direction and having a fifth dopant concentration of the first conductivity type that is higher than the third dopant concentration.~~

~~28. An integrated circuit, comprising:~~

~~a first charge storage region configured to receive, generated in the integrated circuit in response to incident light from a light source, charge carriers; and~~

~~a second charge storage region electrically coupled to the first charge storage region and configured to receive, via the first charge storage region, charge carriers,~~

wherein the second charge storage region is further configured to induce, in a first direction away from the first charge storage region, a first intrinsic electric field.

29. The integrated circuit of claim 28, wherein the second charge storage region comprises:

a first doped sub-region having a first intrinsic electric potential level; and

a second doped sub-region spaced from the first doped region in the first direction and having a second intrinsic electric potential level that is different from the first intrinsic electric potential level.

30. The integrated circuit of claim 29, wherein the first doped sub-region has a first pinning voltage and the second doped sub-region has a second pinning voltage that is different from the first pinning voltage.

31. The integrated circuit of claim 30, wherein the first doped region has a first dopant concentration of a first conductivity type and the second doped region has a second dopant concentration of the first conductivity type that is higher than the first dopant concentration.

32. The integrated circuit of claim 31, further comprising a readout region spaced from the second charge storage region in the first direction and having a third dopant concentration of the first conductivity type that is higher than the first dopant concentration.

33. The integrated circuit of claim 32, further comprising a photodetection region, wherein the first charge storage region is spaced from the photodetection region in the first direction and is configured to receive charge carriers generated in the photodetection region in response to incident light from a light source.

34. The integrated circuit of claim 33, wherein the photodetection region has a fourth dopant concentration of the first conductivity type that is lower than the first dopant concentration.

35. A method of manufacturing an integrated circuit, the method comprising:

forming a photodetection region, a first charge storage region, and a second charge storage region in the integrated circuit, with the first charge storage region spaced from the photodetection region in the first direction and the second charge storage region spaced from the first charge storage region in the first direction,

~~wherein the photodetection region, the first charge storage region, and the second charge storage region are formed so as to induce an intrinsic electric field in the first direction.~~

~~36. The method of claim 35, wherein:~~

~~forming the photodetection region comprises doping the photodetection region with a first dopant concentration of a first conductivity type;~~

~~forming the first charge storage region comprises doping the first charge storage region with a second dopant concentration of the first conductivity type that is higher than the first dopant concentration; and~~

~~forming the second charge storage region comprises doping the second charge storage region with a third dopant concentration of the first conductivity type that is higher than the second dopant concentration.~~

~~37. The method of claim 36, wherein forming the photodetection region, the first charge storage region, and the second charge storage region comprises:~~

~~doping the photodetection region, the first charge storage region, and the second charge storage region with first dopants of the first conductivity type; and~~

~~doping the first charge storage region and the second charge storage region with second dopants of the first conductivity type.~~

~~38. The method of claim 36, wherein doping the second charge storage region comprises:~~

~~doping a first doped sub-region of the second charge storage region with the third dopant concentration; and~~

~~doping a second doped sub-region with a fourth dopant concentration of the first conductivity type that is higher than the third dopant concentration, wherein the first charge storage region is positioned closer to the first doped sub-region in the first direction than to the second doped sub-region.~~

~~39. The method of claim 38, wherein forming the photodetection region, the first charge storage region, and the second charge storage region comprises:~~

~~doping the photodetection region, the first charge storage region, and the second charge storage region with first dopants of the first conductivity type; and~~

~~doping the first charge storage region and the first and second doped sub-regions of the second charge storage region with second dopants of the first conductivity type; and~~

doping the second doped sub-region of the second charge storage region with third dopants of the first conductivity type.

40. The method of claim 38, further comprising forming a readout region spaced from the second charge storage region in the first direction by doping the readout region with a fifth dopant concentration of the first conductivity type that is higher than the third dopant concentration.

41. A method of manufacturing an integrated circuit, the method, comprising:

forming a photodetection region, a first charge storage region electrically coupled to the photodetection region to receive charge carriers from the photodetection region, and a second charge storage region electrically coupled to the first charge storage region to read out charge carriers while the first charge storage region receives charge carriers from the photodetection region.

42. The method of claim 41, wherein forming the first and second charge storage regions comprises inducing a potential barrier between the first and second charge storage regions.

43. The method of claim 42, further comprising positioning a first transfer gate, at least in part, between the first and second charge storage region and to receive a first control signal that causes the first transfer gate to control the potential barrier between the first and second charge storage regions.

44. The method of claim 43, further comprising forming a first charge transfer channel connecting the first charge storage region to the second charge storage region to be biased by the first transfer gate to control the potential barrier between the first and second charge storage regions.

45. The method of claim 44, further comprising:

forming a drain region electrically coupled to the photodetection region to receive charge carriers from the photodetection region;

positioning a second transfer gate, at least in part, between the photodetection region and the first charge storage region to receive a second control signal that causes the second transfer

gate to control a potential barrier between the photodetection region and the first charge storage region; and

forming a second charge transfer channel connecting the photodetection region to the first charge storage region to be biased by the second transfer gate to control the potential barrier between the photodetection region and the first charge storage region.

46. The method of claim 43, further comprising:

forming an intermediate charge storage region electrically coupled between the first and second charge storage regions;

positioning a first transfer gate, at least in part, between the first and intermediate charge storage regions to receive a first control signal that causes the first transfer gate to control a potential barrier between the first and intermediate charge storage regions;

forming a first charge transfer channel connecting the first charge storage region to the intermediate charge storage region to be biased by the first transfer gate to control the potential barrier between the first and intermediate charge storage regions;

positioning a second transfer gate, at least in part, between the intermediate and second charge storage regions to receive a second control signal that causes the second transfer gate to control a potential barrier between the intermediate and second charge storage regions; and

forming a second charge transfer channel connecting the intermediate charge storage region to the second charge storage region to be biased by the second transfer gate to control the potential barrier between the intermediate and second charge storage regions.

47. The method of claim 41, further comprising:

forming a readout region electrically coupled to the second charge storage region to read out the charge carriers from the second charge storage region.