

METHODS OF MICRO-VIA FORMATION FOR ADVANCED PACKAGING

BACKGROUND

Field

[0001] Embodiments described herein generally relate to micro-via structures for advanced wafer level semiconductor packaging and methods of forming the same.

Description of the Related Art

[0002] Along with other ongoing trends in the development of miniaturized electronic devices and components, the demand for faster processing capabilities with greater circuit densities imposes corresponding demands on the materials, structures, and processes utilized in the fabrication of integrated circuit chips, circuit boards, and package structures. Accordingly, one area of focus in semiconductor device development is the structure and fabrication methods of device interconnections (i.e., interconnects or interconnect structures) with reduced lateral dimensions.

[0010] As is known, a vertical interconnect access (or “via”) is one example of an interconnect structure, and laser drilling is an established method for forming vias. Despite the trend toward smaller vias for higher interconnect density, conventional approaches for forming vias with such small diameters, e.g., diameters approaching 10 μm or less, particularly in a high-volume manufacturing setting, may sacrifice certain quality parameters of the vias in order to obtain desired dimensions. Examples of such quality parameters generally include via morphology, uniformity, and via pad cleanliness.

[0011] Additionally, current approaches for laser drilling vias typically rely on ultraviolet (UV) laser or pulsed CO₂ lasers to directly drill the vias in panels. Both of these approaches require complex beam shaping optics to convert Gaussian laser beam profiles emitted by the laser sources into top-hat (i.e., flat top) shaped beam profiles, and such top-hat shaped beam profiles are typically not capable of drilling diameters less than 40 μm in a consistent and cost-effective manner. Thus, masks may be used in combination with laser drilling in order to achieve a desired

via size. However, current masking techniques require wet etching and/or laser drilling for mask patterning, which may cause damage to any underlying layers and/or formation of unwanted debris. Further, certain approaches utilize masks formed of substantially the same material as underlying conductive layers and/or interconnects, thus making it difficult to remove the mask upon laser drilling of vias.

[0003] Therefore, there is a need in the art for improved methods of forming high-quality, small-diameter vias, e.g., micro-vias.

SUMMARY

[0004] The present disclosure generally relates to micro-via structures for advanced wafer level semiconductor packaging and methods of forming the same.

[0005] In certain embodiments, a method of forming a micro-via structure in a semiconductor device is provided. The method includes laminating a dielectric layer over the semiconductor device, depositing a metal layer over the dielectric layer, and applying, patterning, and developing a resist over the metal layer to form a trench in the resist layer corresponding to a desired lateral dimension of the micro-via structure. The method further includes etching the metal layer through the trench in the developed resist layer to extend the trench into the metal layer and expose a portion of the dielectric layer. The method also includes laser ablating the exposed portion of the dielectric layer to form the micro-via structure therein having the desired lateral dimension.

[0006] In certain embodiments, a method of forming a micro-via structure in a semiconductor device is provided. The method includes laminating a dielectric layer over a conductive layer of the semiconductor device, depositing a metal layer over the dielectric layer, and applying, patterning, and developing a resist over the metal layer to form a trench in the resist layer corresponding to a desired lateral dimension of the micro-via structure. The method further includes selectively etching the metal layer through the trench in the developed resist layer to extend the trench into the metal layer and expose a portion of the dielectric layer, laser ablating the exposed portion of the dielectric layer to form the micro-via structure therein having the desired lateral dimension, exposing the micro-via structure to a

cleaning process to remove debris therefrom, and selectively removing the metal layer from the dielectric layer.

[0007] In certain embodiments, a method of forming a micro-via structure in a semiconductor device is provided. The method includes laminating a dielectric layer over a conductive layer of the semiconductor device, depositing a chromium layer over the dielectric layer, and applying, patterning, and developing a resist over the chromium layer to form a trench in the resist layer corresponding to a desired lateral dimension of the micro-via structure. The method further includes selectively etching the chromium layer through the trench in the developed resist layer to extend the trench into the chromium layer and expose a portion of the dielectric layer, laser ablating the exposed portion of the dielectric layer to form the micro-via structure therein having the desired lateral dimension, wherein the conductive layer of the semiconductor device is utilized as a laser stop. The method further includes removing the resist from the chromium layer, exposing the micro-via structure to a cleaning process to remove debris therefrom, and selectively removing the metal layer from the dielectric layer with a wet etch process. The cleaning process includes a dry fluorine-based plasma etch and a methanol-based wet clean.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] So that the manner in which the above recited features of the present disclosure can be understood in detail, a more particular description of the disclosure, briefly summarized above, may be had by reference to embodiments, some of which are illustrated in the appended drawings. It is to be noted, however, that the appended drawings illustrate only typical embodiments of this disclosure and are therefore not to be considered limiting of its scope, for the disclosure may admit to other equally effective embodiments.

[0009] **FIG. 1** illustrates a flow diagram of a process for forming a micro-via in a semiconductor device, according to embodiments described herein.

[0010] **FIGs. 2A-2J** schematically illustrate cross-sectional views of a portion of a semiconductor device at different stages of the process depicted in **FIG. 1**, according to embodiments described herein.

[0011] **FIGs. 3A-3B** schematically illustrate cross-sectional views of micro-vias formed by the process depicted in **FIG. 1**, according to embodiments described herein.

[0012] **FIG. 4** schematically illustrates a cross-sectional view of an exemplary semiconductor device that includes micro-vias formed by the process depicted in **FIG. 1**, according to embodiments described herein.

DETAILED DESCRIPTION

[0013] Embodiments of the present disclosure relate to micro-via structures for advanced wafer level semiconductor packaging and methods of forming the same. The ongoing demands for miniaturized package structures with greater densities drive a need for corresponding small-sized interconnects, e.g., vias. However, as circuit densities are being increased and via dimensions decreased, via formation methods become increasingly difficult, largely due to limitations associated with quality and uniformity of laser-drilling narrow via structures. As a result, low quality and non-uniform vias are formed, which may result in reduced performance. The methods described herein provide for improved methods of forming high quality and uniform micro-via structures.

[0014] **FIG. 1** illustrates a flow diagram of a representative method 100 for forming a micro-via in a semiconductor device, such as in a redistribution layer (RDL) of a semiconductor package, according to certain embodiments of the present disclosure. **FIGs. 2A-2J** schematically illustrate cross-sectional views of a portion of a semiconductor device 200 at different stages of the method 100 represented in **FIG. 1**. Accordingly, **FIG. 1** and **FIGs. 2A-2J** are herein described together for clarity. Note that although described in relation to the formation of a single micro-via, the methods disclosed herein may be utilized to form a plurality or array of micro-vias in a semiconductor device simultaneously or in sequence.

[0015] Generally, method 100 begins at operation 102, corresponding to **FIG. 2A**, wherein an insulating layer 208 is laminated over the semiconductor device 200. As described above, in **FIGs. 2A-2J**, only a portion of semiconductor device 200 is shown, and the insulating layer 208 may be utilized to form an RDL thereon. The semiconductor device 200 may be any suitable type of semiconductor device,

including but not limited to a 3D semiconductor package (e.g., 3D wafer level package (WLP), 3D system-in-package (SiP), stacked integrated circuit (SIC), 3D package-on-package (POP), etc.), 2.5D interposer, 2D semiconductor package, and the like. Accordingly, semiconductor device 200 may include one or more embedded active and/or passive devices (e.g., semiconductor dies, memory dies, capacitors, inductors, RF devices, etc.) (not shown) and one or more conductive interconnects routed therebetween (not shown).

[0016] As illustrated in **FIG. 2A**, the semiconductor device 200 includes a substrate 202, which may function as a frame or core structure for the semiconductor device 200. Generally, the substrate 202 is formed of any suitable substrate material including but not limited to a III-V compound semiconductor material, silicon (e.g., having a resistivity between about 1 and about 10 Ohm-cm or conductivity of about 100W/mK), crystalline silicon (e.g., Si<100> or Si<111>), silicon oxide (SiO₂), silicon germanium (SiGe), doped or undoped silicon, undoped high resistivity silicon (e.g., float zone silicon having lower dissolved oxygen content and a resistivity between about 5000 and about 10000 ohm-cm), doped or undoped polysilicon, silicon nitride (Si₃N₄), silicon carbide (SiC) (e.g., having a conductivity of about 500W/mK), quartz, glass (e.g., borosilicate glass), sapphire or aluminum oxide (Al₂O₃), and/or ceramic materials. In certain embodiments, the substrate 202 is a monocrystalline p-type or n-type silicon substrate. In certain embodiments, the substrate 202 is a polycrystalline p-type or n-type silicon substrate. In certain embodiments, the substrate 202 is a p-type or n-type silicon solar substrate.

[0017] The substrate 202 may further have any suitable shape and/or dimensions. For example, the substrate 202 may have a polygonal or circular shape. In certain embodiments, the substrate 202 includes a substantially square silicon substrate having lateral dimensions between about 120 mm and about 220 mm, such as about 160 mm or between about 156 mm and about 166 mm, with or without chamfered edges. In certain other embodiments, the substrate 202 includes a circular silicon-containing wafer having a diameter between about 100 mm and about 450 mm, such as between about 150 mm and about 300 mm, for example about 200 mm.

[0018] Unless otherwise noted, embodiments and examples described herein are conducted on substrates having a thickness between about 50 μm and about 1500 μm , such as between about 90 μm and about 780 μm . For example, the substrate 202 has a thickness between about 100 μm and about 300 μm , such as a thickness between about 110 μm and about 200 μm . In another example, the substrate 202 has a thickness between about 60 μm and about 180 μm , such as a thickness between about 80 μm and about 120 μm .

[0019] In certain embodiments, the semiconductor device 202 further includes an insulating layer 204 formed on the substrate 202. Generally, the insulating layer 204 may be formed of a dielectric and polymeric material, such as an epoxy resin. For example, the insulating layer 204 may be formed of a ceramic-filler-containing epoxy resin, such as an epoxy resin filled with (e.g., containing) substantially spherical silica (SiO_2) particles. As used herein, the term “spherical” refers to any round, ellipsoid, or spheroid shape. For example, in certain embodiments, the ceramic fillers may have an elliptic shape, an oblong oval shape, or other similar round shape. However, other morphologies are also contemplated. Other examples of ceramic fillers that may be utilized to form dielectric film 220 include aluminum nitride (AlN), aluminum oxide (Al_2O_3), silicon carbide (SiC), silicon nitride (Si_3N_4), $\text{Sr}_2\text{Ce}_2\text{Ti}_5\text{O}_{16}$ ceramics, zirconium silicate (ZrSiO_4), wollastonite (CaSiO_3), beryllium oxide (BeO), cerium dioxide (CeO_2), boron nitride (BN), calcium copper titanium oxide ($\text{CaCu}_3\text{Ti}_4\text{O}_{12}$), magnesium oxide (MgO), titanium dioxide (TiO_2), zinc oxide (ZnO) and the like.

[0020] In some examples, the ceramic fillers utilized to form the insulating layer 204 have particles ranging in size between about 40 nm and about 1.5 μm , such as between about 80 nm and about 1 μm . For example, the ceramic fillers utilized to form the insulating layer 204 have particles ranging in size between about 200 nm and about 800 nm, such as between about 300 nm and about 600 nm. In certain embodiments, the ceramic fillers include particles having a size less than about 25% of a width or diameter of a desired structure patterned in the substrate 202, including vias for interconnects and cavities for active and/or passive devices. In certain embodiments, the ceramic fillers have particles having a size less than about 15% of a desired patterned structure's width or diameter.

[0021] In still further embodiments, the insulating layer 204 is formed of a polyimide material, such as a photodefinable or non-photosensitive polyimide material, a polybenzoxazole (PBO) material, a silicon dioxide material, and/or a silicon nitride material.

[0022] As further illustrated in **FIG. 2A**, the semiconductor device 202 includes a conductive layer 206 formed over the insulating layer 204. The conductive layer 206 may represent a trace layer, wiring layer, pad layer, or any other type of lateral interconnect structure for electrically coupling one or more active and/or passive devices. In certain embodiments, the conductive layer 206 has a thickness between about 2 μm and about 20 μm , such as between about 3 μm and about 18 μm , such as between about 6 μm and about 18 μm . The conductive layer 206 is generally formed of one or more layers of any suitable conductive material, including but not limited to copper (Cu), aluminum (Al), gold (Au), nickel (Ni), silver (Ag), palladium (Pd), tin (Sn), or the like. In certain embodiments, an adhesion layer (not shown) and/or a seed layer (not shown) are formed between surfaces of the insulating layer 204 and the conductive layer 206 for better adhesion of the conductive layer 206 thereto and to block diffusion of conductive materials. For example, in certain embodiments, a molybdenum (Mo), titanium (Ti), tantalum (Ta), or titanium-tungsten (WTi) adhesion layer and/or a copper seed layer are formed between the insulating layer 204 and the conductive layer 206.

[0023] Returning back now to **FIG. 1** and method 100, at operation 102, the insulating layer 208 is laminated over the semiconductor device 200. In certain embodiments, the insulating layer 208 is substantially similar to insulating layer 204. For example, in certain embodiments, the insulating layer 208 is formed of a dielectric material, such as a ceramic-filler-containing epoxy resin, a polyimide material, a PBO material, a silicon dioxide material, and/or a silicon nitride material. In certain other embodiments, however, the insulating layer 208 is formed of a different material than insulating layer 204. Generally, the insulating layer 208 has a thickness between about 2 μm and about 20 μm , such as between about 4 μm and about 18 μm , such as between about 6 μm and about 14 μm .

[0024] During lamination, insulating layer 208 (e.g., as a film) is placed over the semiconductor device 200 and is thereafter exposed to elevated temperatures,

causing the insulating layer 208 to soften and adhere to, e.g., the conductive layer 206, of the semiconductor device 200. In certain embodiments, the lamination operation includes a vacuum lamination process that may be performed in a laminator or other suitable device. In certain embodiments, the lamination operation is performed by use of a hot pressing process.

[0025] In certain embodiments, the lamination operation is performed at a temperature of between about 80 °C and about 200 °C and for a period between about 5 seconds and about 90 seconds, such as between about 30 seconds and about 60 seconds. In certain embodiments, the lamination operation includes the application of a pressure of between about 1 psig and about 50 psig while the semiconductor device 200, with insulating layer 208 placed thereon, is exposed to a temperature between about 80 °C and about 140 °C for a period between about 5 seconds and about 90 seconds. For example, the lamination operation is performed at a pressure of between about 5 psig and about 40 psig and a temperature of between about 100 °C and about 120 °C for a period between about 10 seconds and about 1 minute. In some examples, the lamination operation is performed at a temperature of about 110 °C for a period of about 20 seconds.

[0026] Once the insulating layer 208 is laminated onto the semiconductor device 200, a metal mask layer 210 is deposited over the insulating layer 208 at operation 104, which corresponds to **FIG. 2B**. The metal mask layer 210 may be formed of one or more suitable metals, including but not limited to chromium (Cr), tungsten (W), molybdenum, copper, and/or the like. In certain embodiments, the metal mask layer 210 is formed of a refractory metal. Generally, the metal mask layer 210 has a thickness between about 50 nm and about 500 nm, such as between about 100 nm and about 400 nm, such as between about 100 nm and about 300 nm. For example, in certain embodiments, the metal mask layer 210 has a thickness of about 200 nm. The metal mask layer 210 may be deposited over the insulating layer 208 by any suitable deposition techniques, including but not limited to sputtering deposition processes (i.e., sputtering by PVD deposition processes).

[0027] At operation 106 and **FIG. 2C**, a spin-on/spray-on or dry film resist layer 212, such as a photoresist, is applied, laminated, and patterned over the metal mask layer 210. In certain embodiments, the resist layer 212 is patterned by selective

exposure to UV radiation to form one or more patterned regions 213. For example, in certain embodiments, the resist layer 212 is selectively exposed to UV radiation using maskless lithography, such as direct write digital lithography. Upon patterning, the resist layer 212 is developed at operation 108 and **FIG. 2D** to form one or more trenches 214 therein. As shown in **FIG. 2D**, in examples where the resist layer 212 is a negative photoresist, the trenches 212 are formed in regions of the resist layer 212 previously left un-patterned at operation 106. In examples where the resist layer 212 is a positive photoresist, the trenches 212 correspond to the patterned regions 213 formed at operation 106. In certain embodiments, the development process is a wet process that includes exposing the resist layer 212 to a solvent. For example, the development process may be a wet etch process utilizing an aqueous etch process. In other examples, the film development process may be a wet etch process utilizing a buffered etch process selective for a desired material. However, any suitable wet solvents or combination of wet etchants may be used for the resist film development process.

[0028] As depicted in **FIGs. 2C-2D**, the resist layer 212 is patterned and developed according to a desired morphology and lateral dimensions of a subsequently formed micro-via. Generally, the micro-via has a cylindrical or round tubular shape corresponding to a morphology of an interconnect to be routed therethrough. Accordingly, in certain embodiments, the resist layer 212 is patterned and developed to form a cylindrical trench 214 therein, enabling the downstream transfer of the cylindrical pattern to the metal mask layer 210 and insulating layer 208. In further embodiments, however, a non-cylindrical or non-annular interconnect and/or via is desired, and thus, a non-cylindrical trench 214 is formed. For example, in certain embodiments, the trench 214 formed in resist layer 212 at operation 108 may be ovate, ellipsoid, or polygonal in shape.

[0029] At operation 110 and **FIG. 2E**, the semiconductor device 200, now having a patterned and developed resist layer 212 formed thereon, is exposed to an etch process to transfer the pattern of the resist layer 212 to the metal mask layer 210. Accordingly, the trench 214 is extended into the metal mask layer 210, thus exposing the insulating layer 208 below. As shown in **FIG. 2E**, a portion of the resist layer 212 may also be consumed during the process.

[0030] In certain embodiments, the etch process is a plasma-based dry etch process performed in an inductively-coupled plasma (ICP) dry etch chamber. For example, in embodiments where the metal mask layer 210 is a chromium mask layer, the semiconductor device 200 may be exposed to a dry chromium-selective etch process. In such embodiments, the dry etch process may utilize oxygen (O₂), ammonia (NH₃), nitrogen (N₂), helium (He), chlorine (Cl₂), and/or argon (Ar) reactive gases. For example, in certain embodiments, a reactive gas mixture of 90:5:20 Cl₂:O₂:Ar is utilized. The chromium-selective etch process may further utilize a plasma-generating power of between about 200 watts (W) and about 2000 W, such as about 600 W, with a bias power between about 100 W and about 400 W, such as about 220 W, and may be carried out at a pressure of between about 2 milliTorr (mTorr) and about 100 mTorr, such as about 10 mT.

[0031] After etching the metal mask layer 210, the semiconductor device 200 is exposed to a laser ablation process at operation 112 and **FIG. 2F** to ablate the portion of the insulating layer 208 exposed through the metal mask layer 210, thus forming a micro-via 216 therein. The laser ablation process may be performed utilizing any suitable type of laser system with adjustable laser process parameters and characteristics, including but not limited to laser power, focal beam diameter, focus height, pulse energy, pulse width, burst energy, number of pulses per burst train (e.g., sequences of pulses separated by a desired duration of time), pulse frequency, burst frequency, beam spot size, and spatial beam profile (Gaussian or top-hat). Generally, the laser system at operation 112 may generate a laser beam with a spot size larger than the litho-defined hole in the metal mask layer 210, since the metal mask layer 210 will protect portions of the insulating layer 208 disposed thereunder.

[0032] In certain embodiments, the laser ablation process at operation 112 is performed utilizing an ultraviolet (UV) laser, such as a femtosecond (fs) UV laser with an Innoslab laser source, emitting a laser beam with a wavelength between about 180 nm and about 400 nm, such as between about 300 nm and about 360 nm, such as about 345 nm or about 355 nm. In such embodiments, the UV laser may ablate the insulating layer 208 by generating a pulsed laser beam, which may be emitted in one or more fixed-frequency, e.g., 50 MHz or more, pulse-burst trains

with a pulse energy between about 5 nJ and about 10 nJ. Since metals such as copper are not resistant to UV laser beams, utilization of a pulse-burst mode with a precise energy dosage between about 5-10 nJ may facilitate ablation of the insulation layer 208 with reduced debris formation and little to no damage to the underlying conductive layer 206, as compared to a continuous or continuously-pulsed UV laser beam. Thus, the conductive layer 206 may act as a laser stop during the laser ablation process at operation 112. Furthermore, the UV laser conditions described above, in combination with the pre-patterned metal mask layer 210, enable very precise via shape control, including top/bottom opening size, opening morphology, and taper between top/bottom openings.

[0033] In certain embodiments, the laser ablation process at operation 112 is performed utilizing a laser source performing at infrared (IR) wavelengths between about 700 nm and about 1 mm, such as near-infrared (NIR) wavelengths between about 700 nm to about 2.5 μm , or mid-infrared (mid-IR) wavelengths between about 2.5 μm and about 24 μm . For example, in certain embodiments, the laser ablation process at operation 112 is performed using a laser source with a NIR to mid-IR wavelength between about 2 μm and about 3 μm . The 2-3 μm wavelengths are highly selective for polymeric materials relative to metallic materials and thus, allow a higher alignment tolerance between the emitted laser beam and the pre-patterned trench 214 in the metal mask layer 210 since the metal mask layer 210 will simply reflect any misaligned portion of the laser beam. Furthermore, the increased ablation efficiency of the 2-3 μm wavelengths for polymeric materials, such as those of the insulating layer 208, and relatively low ablation efficiency for metals facilitates little to no damage to the underlying conductive layer 206 during operation 112. In certain embodiments, the NIR or mid-IR laser is a fiber laser producing a laser beam via one or more cascaded processes in an optical fiber. For example, in certain embodiments, the fiber laser may inject a nanosecond (ns) or picosecond (ps) seed laser beam, e.g., of wavelength of about 1 μm , into a series of passive or active fibers with extended transmission in the desired IR wavelength range for nonlinear frequency conversion. In certain other embodiments, the fiber laser may pump a short pulse, high intensity, seed laser beam, such as a fs seed laser beam, into a highly nonlinear optical medium with normal dispersion, such as chalcogenide glass

fibers. In still other embodiments, the fiber laser may utilize erbium-doped or fluoride fibers, or other doped mid-IR fibers to emit at wavelengths of about 3 μm .

[0034] In embodiments where a plurality or array of micro-vias 216 are desired, the laser system may include a scanner 220, such as a single- or multi-axis large angle galvanometer optical scanner (e.g., galvo scanner), to facilitate scanning of one or more laser beams from a laser source across a surface of the semiconductor device 200 to form the plurality or array of micro-vias 216. The term “galvanometer scanner” generally refers to any type of device that may change a projection or reflection angle of one or more laser beams to sweep the laser beam(s) across the semiconductor device 200. For example, the scanner 220 may include one or more adjustable and electromechanically-controlled mirrors to diverge (e.g., multiply) and/or steer the laser beam across the semiconductor device 200 during the laser ablation process at operation 112. In certain embodiments, utilization of the scanner 220 enables drilling of a single micro-via 216 in the semiconductor device 200 at a time, multiple micro-vias 216 simultaneously, or scanning of the laser beam across a surface of the semiconductor device 200 to form a plurality of micro-vias 216 with several sweeps.

[0035] At operation 114 and **FIG. 2G**, a resist removal process is performed to strip the resist layer 212 from the semiconductor device 200. Operation 114 may be performed before or after the laser ablation process at operation 112. In certain embodiments, the resist layer 212 is removed by one or more dry processes such as dry etching or ashing. In certain embodiments, the resist removal process includes exposing the semiconductor device 200 to a microwave O_2 plasma while maintaining the semiconductor device 200 at a temperature between about 60 $^{\circ}\text{C}$ and about 100 $^{\circ}\text{C}$, such as about 80 $^{\circ}\text{C}$, which enables the removal of the resist layer 212 without damaging the conductive layer 206 exposed through micro-via 216. Temperature is a critical factor at operation 114, as utilizing too low of a temperature will drastically decrease the resist strip rate, while utilizing too high of a temperature may cause damage to the underlying conductive layer 206.

[0036] After resist removal, the semiconductor device 200 is exposed to a cleaning process at operation 116 and **FIG. 2H** to remove any undesired debris remaining in the micro-via 216 from the prior laser ablation process and smoothen surfaces (e.g.,

walls) of the micro-via 216 exposed to laser drilling. The cleaning process may include any combination of dry and/or wet processes. In certain embodiments, the semiconductor device 200 is exposed to a dry etch process, such as a plasma-based dry etch process. In such embodiments, the plasma-based dry etch process may utilize O₂, CF₄, NH₃, N₂, Cl₂, and/or Ar reactive gases. For example, in certain embodiments, the plasma-based dry etch process utilizes a reactive gas mixture of 50:3:5 O₂:CF₄:Ar, a plasma-generating power of between about 200 watts (W) and about 2000 W, such as about 500 W, and a bias power between about 25 W and about 100 W, such as about 50 W. In further embodiments, the semiconductor device 200 is exposed to a wet process, which may be used in combination with one or more dry processes. For example, in certain embodiments, the semiconductor device 200 is exposed to an aqueous solution of 5% methanol:cupric chloride (CuCl₂) 3:1, which may be utilized in combination with a plasma-based dry etch process, such as a plasma-based dry etch process utilizing a reactive fluorine gas.

[0037] At operation 118 and **FIG. 2I**, the semiconductor device 200, now cleaned, is selectively etched to remove the metal mask layer 210. Thus, unlike some conventional methods, the metal mask layer 210 does not remain on the semiconductor device 200 during downstream formation of interconnects and therefore, enables the deposition of a seed layer and/or barrier layer directly over the insulating layer 208 prior to interconnect formation. In certain embodiments, the etch process at operation 118 is a wet etch process utilizing any suitable wet etchant or combination of wet etchants in aqueous solution. For example, for embodiments wherein the metal mask layer 210 comprises chromium, the semiconductor device 200 may be immersed in an aqueous etching solution comprising 50% NaOH and 33% K₃[Fe(CN)₆] (1:3) at about room temperature (27 °C) for a duration between about 2 to about 10 minutes, such as between about 3 to about 5 minutes.

[0038] Upon selectively etching the metal mask layer 210, an interconnect 222 may be formed within the micro-via 216, as illustrated in **FIG. 2J**. The interconnect 222 may be formed over sidewalls of the micro-via 216 that are defined by the insulating layer 208 and extend through the micro-via 216 to the underlying conductive layer

206. The interconnect 222 may be deposited in the micro-via 216 by any suitable methods including electroless deposition or a combination of physical vapor deposition (PVD) and electrochemical deposition (ECD). In certain embodiments, the interconnect 222 is deposited to fill or “plug” the micro-via 216, thus creating a solid or filled conductive body therein. In certain other embodiments, however, the interconnect 222 is deposited to only line surfaces of the micro-via 216.

[0039] The interconnect 222 may generally be formed of one or more layers of any suitable conductive material, including but not limited to copper (Cu), aluminum (Al), gold (Au), nickel (Ni), silver (Ag), palladium (Pd), tin (Sn), or the like. In certain embodiments, as described above, an adhesion layer (not shown) and/or a seed layer (not shown) may be formed over the surfaces of the micro-via 216 prior to deposition of the interconnect 222. For example, in certain embodiments, a molybdenum, titanium, tantalum, or titanium-tungsten adhesion layer and/or a copper seed layer are deposited over sidewalls of the micro-via 216 prior to deposition of the interconnect 222 to improve adhesion thereof and block diffusion of conductive materials.

[0040] **FIGs. 3A** and **3B** schematically illustrate cross-sectional views of exemplary micro-via structures which can be formed in, e.g., the semiconductor device 200 by the method 100 described above, according to certain embodiments. Note, that only a portion of the semiconductor device 200 is shown in **FIGs. 3A-3B**.

[0041] As shown in **FIG. 3A**, micro-via 316a is an example of a micro-via formed in a redistribution layer of the semiconductor device 200, which may be a semiconductor package. Accordingly, the micro-via 316a is depicted as being disposed through the insulating layer 208 above the substrate 202, which further includes the insulating layer 204 and the conductive layer 206 formed thereon. Generally, the micro-via 316a is formed through an entire thickness of the insulating layer 208 and therefore, the conductive layer 206 may be used as a laser stop during laser ablation of the micro-via 316a. In certain embodiments, the micro-via 316a has a height between about 2 μm and about 20 μm , which may be equivalent to a thickness of the insulating layer 208. In certain embodiments, the micro-via 316a has substantially vertical sidewalls, and thus, may have a uniform diameter between about 2 μm and about 10 μm , such as a uniform diameter between about

3 μm and about 7 μm . In certain embodiments, a ratio of the micro-via 316a diameter to a thickness of the insulating layer 208 is between about 1:2 and about 1:1.

[0042] In certain other embodiments, as shown in **FIG. 3A**, the micro-via has tapered or angled sidewalls. For example, the sidewalls of the micro-via 316 may have a taper angle α between about 60° and about 90°, such as a taper angle α between about 80° and about 90°. In such embodiments, a top diameter D_T of the micro-via 316a is between about 2 μm and about 15 μm , such as between about 4 μm and about 12 μm , and a bottom diameter D_B of the micro-via 316a is between about 1 μm and about 8.5 μm , such as between about 2 μm and about 6 μm . Formation of tapered or conical morphologies may be accomplished by, e.g., moving the laser beam of the laser system utilized, e.g., at operation 112, in a spiraling (e.g., circular, corkscrew) motion relative to the central axis of the micro-via 316a. The laser beam may also be angled using a motion system to form the tapered micro-via 316a.

[0043] As shown in **FIG. 3B**, micro-via 316b is an example of a micro-via formed through the substrate 202 of the semiconductor device 200, e.g., extending from a first surface 303a of the substrate 202 to a second surface 303b. In such embodiments, the micro-via 316b is laser-ablated through the insulating layer 204 of the semiconductor device 200, which encapsulates (e.g., surrounds) the substrate 202 and passes through a through-silicon via 314 formed in the substrate 202. Accordingly, in order to form the micro-via 316b, the through-silicon via 314 must first be formed through the substrate 202 by any suitable substrate patterning method(s) prior to the method 100 described above, after which the insulating layer 204 may be laminated over the substrate 202 to adhere thereto and flow into the through-silicon via 314 at operation 100.

[0012] In certain embodiments, the through-silicon via 314 is formed via laser ablation, e.g., using an IR, UV, or CO₂ laser. For example, the laser utilized to ablate the through-silicon via 314 may be a ps or fs UV laser. In certain examples, the laser is a fs green laser. In still other embodiments, the through-silicon via 314 is formed via a suitable etching process, e.g., a dry etching process, or a bead blasting process. Generally, the through-silicon via 314 may have a cylindrical or

tapered morphology, as shown in **FIG. 3B**. Similar to the micro-via 316a, formation of tapered or conical morphologies may be accomplished by, e.g., moving the laser beam of a laser utilized during substrate patterning in a spiraling (e.g., circular, corkscrew) motion relative to the central axis of the through-silicon via 314. The laser beam may also be angled using a motion system. Similar methods may also be utilized to form a cylindrical through-silicon via 314 having a uniform diameter therethrough.

[0044] Upon formation of the through-silicon via 314, insulating layer 204 may be placed over the substrate 202 and laminated, e.g., at operation 102 of the method 100, thus flowing into and filling the through-silicon via 314. In certain embodiments, the lamination process is a vacuum lamination process that may be performed in an autoclave or other suitable device. In certain embodiments, the lamination process is performed by use of a hot pressing process. In certain embodiments, the lamination process is performed at a temperature of between about 80 °C and about 140 °C, and for a period between about 5 seconds and about 1.5 minutes. In such embodiments, the lamination process may be performed at a pressure between about 1 psig and about 50 psig. For example, the lamination process may be performed at a pressure between about 5 psig and about 40 psig and a temperature of between about 100 °C and about 120 °C for a period between about 10 seconds and about 1 minute.

[0045] After lamination, the micro-via 316b is formed in a portion of the insulating layer 204 extending through the through-silicon via 314, as shown in **FIG. 3B**, using the method 100. Generally, the micro-via 316b may have a similar lateral shape and/or dimensions to micro-via 316a, e.g., tapered or conical morphology.

[0046] **FIG. 4** illustrates a schematic cross-sectional side view of an exemplary semiconductor package 400 having micro-vias formed by the method 100 described above, according to certain embodiments. As shown, the semiconductor package 400 includes a substrate 402, e.g., a silicon substrate, which functions as a package frame and has one or more cavities 408 and one or more through-silicon vias 414 formed therein. An insulating layer 404 is laminated over the substrate 402 and extends through the cavities 408 and the through-silicon vias 414 from a first side 403a of the substrate 402 to a second side 403b. One or more

semiconductor dies 406 are disposed in each cavity 408 and are embedded within the insulating layer 404 therein. Similarly, one or more interconnects 412 are disposed in each through-silicon via 414 and are surrounded by the insulating layer 404 therein. On either side of the semiconductor package 400 is a redistribution layer 420, which is comprised of one or more redistribution interconnects 422 in electrical communication with the one or more interconnects 412. The redistribution interconnects 422 may include vertical interconnects and lateral interconnects, such as traces, wires, and pads.

[0047] During the formation of the semiconductor package 400, the lamination of the insulating layer 404 causes the dielectric material thereof to flow into and fill the through-silicon vias 414. Therefore, in order to form channels or pathways for the interconnects 412 through the entirety of the substrate 402 after lamination of the insulating layer 404, vias 416a may be laser drilled through the dielectric material of the insulating layer 404 within the through-silicon vias 414, thus forming a via-in-via structure for routing of interconnects 412. Similarly, after formation of the interconnects 412, redistribution interconnects 422 may be formed on either side of the semiconductor package 400 within redistribution vias 416b, which can be laser drilled into the insulating layer 404 as well. Accordingly, the vias 416a and redistribution vias 416b formed in the insulating layer 404 may be micro-vias formed by the methods described above with reference to **FIG. 1** and **FIGs. 2A-2J** above.

[0048] In summary, the methods and micro-via structures described above provide many advantages over methods and architectures implementing conventional via fabrication techniques for semiconductor devices. Such benefits include the capability of forming high-quality, low-aspect-ratio micro-via structures that advantageously enable high-density packaging architectures for advanced integrated semiconductor devices with improved performance and flexibility, and relatively low manufacturing costs as compared to conventional packaging technologies.

[0049] While the foregoing is directed to embodiments of the present disclosure, other and further embodiments of the disclosure may be devised without departing from the basic scope thereof, and the scope thereof is determined by the claims that follow.

Claims:

1. A method of forming a micro-via structure in a semiconductor device, comprising:
 - laminating a dielectric layer over the semiconductor device;
 - depositing a metal layer over the dielectric layer;
 - applying, patterning, and developing a resist over the metal layer, wherein developing the resist layer forms a trench in the resist layer corresponding to a desired lateral dimension of the micro-via structure;
 - etching the metal layer through the trench in the developed resist layer, wherein etching the metal layer extends the trench into the metal layer and exposes a portion of the dielectric layer; and
 - laser ablating the exposed portion of the dielectric layer, wherein laser ablating the exposed portion of the dielectric layer forms the micro-via structure therein having the desired lateral dimension.
2. The method of claim 1, wherein the dielectric layer comprises an epoxy resin material having a ceramic filler.
3. The method of claim 1, wherein the metal layer comprises chromium (Cr), tungsten (W), molybdenum, or copper.
4. The method of claim 3, wherein the metal layer comprises chromium (Cr).
5. The method of claim 3, wherein the metal layer is deposited over the dielectric layer by physical vapor deposition (PVD).
6. The method of claim 1, wherein the resist is a photoresist and is patterned via selective exposure to UV radiation.
7. The method of claim 1, wherein the resist is patterned using direct write digital lithography.

8. The method of claim 1, wherein the metal layer is dry-etched using an oxygen-based plasma.
9. The method of claim 1, wherein the dielectric layer is laser ablated using a near-infrared (NIR) or mid infrared (mid-IR) laser.
10. The method of claim 1, wherein the dielectric layer is laser ablated using an ultraviolet (UV) laser with a pulse-burst mode.
11. A method of forming a micro-via structure in a semiconductor device, comprising:
 laminating a dielectric layer over a conductive layer of the semiconductor device;
 depositing a metal layer over the dielectric layer;
 applying, patterning, and developing a resist over the metal layer, wherein developing the resist layer forms a trench in the resist layer corresponding to a desired lateral dimension of the micro-via structure;
 selectively etching the metal layer through the trench in the developed resist layer, wherein selectively etching the metal layer extends the trench into the metal layer and exposes a portion of the dielectric layer;
 laser ablating the exposed portion of the dielectric layer, wherein laser ablating the exposed portion of the dielectric layer forms the micro-via structure therein having the desired lateral dimension;
 exposing the micro-via structure to a cleaning process to remove debris therefrom; and
 selectively removing the metal layer from the dielectric layer.
12. The method of claim 11, wherein the metal layer comprises chromium (Cr).
13. The method of claim 12, wherein the metal layer is deposited over the dielectric layer by physical vapor deposition (PVD).

14. The method of claim 11, wherein the resist is patterned using direct write digital lithography.
15. The method of claim 11, wherein the metal layer is selectively dry-etched using an oxygen-based plasma.
16. The method of claim 11, wherein the dielectric layer is laser ablated using a near-infrared (NIR) or mid infrared (mid-IR) laser.
17. The method of claim 11, wherein the dielectric layer is laser ablated using an ultraviolet (UV) laser with a pulse-burst mode.
18. The method of claim 11, wherein the micro-via structure has a lateral dimension between about 2 μm and about 10 μm .
19. The method of claim 11, wherein the micro-via structure has a first lateral dimension between about 2 μm and about 15 μm , and a second later dimension between about 1 μm and about 8.5 μm .
20. A method of forming a mico-via structure in a semiconductor device, comprising:
- laminating a dielectric layer over a conductive layer of the semiconductor device;
 - depositing a chromium layer over the dielectric layer;
 - applying, patterning, and developing a resist over the chromium layer, wherein developing the resist layer forms a trench in the resist layer corresponding to a desired lateral dimension of the micro-via structure;
 - selectively etching the chromium layer through the trench in the developed resist layer, wherein selectively etching the chromium layer extends the trench into the chromium layer and exposes a portion of the dielectric layer;
 - laser ablating the exposed portion of the dielectric layer, wherein laser ablating the exposed portion of the dielectric layer forms the micro-via structure

therein having the desired lateral dimension, and wherein the conductive layer of the semiconductor device is utilized as a laser stop;

removing the resist from the chromium layer;

exposing the micro-via structure to a cleaning process to remove debris therefrom, wherein the cleaning process includes a dry fluorine-based plasma etch and a methanol-based wet clean; and

selectively removing the metal layer from the dielectric layer with a wet etch process.