ABSTRACT

SUB-QUARTER-MICRON MOSFET AND METHOD OF ITS MANUFACTURING

A method for forming a sub-quarter micron MOSFET having an LDD structure is described. An active area is provided in a semiconductor substrate separated from other active areas by isolation regions. Ions are implanted into the semiconductor substrate in the active area wherein a heavily doped region is formed adjacent to the surface of the semiconductor substrate and wherein a lightly doped region is formed underlying the heavily doped region. A first dielectric Layer is deposited overlying the semiconductor substrate in the active area. The first dielectric layer is etched away to form an opening to the semiconductor substrate. The semiconductor substrate within the opening is etched through to form a partial trench in the semiconductor substrate. Spacers are formed on the sidewalls of the first dielectric layer within the opening. A layer of conducting material is deposited over the first dielectric layer and the spacers and within the opening. The conducting material is etched to form a gate electrode to complete the fabrication of the integrated circuit device.

(FIGURE 2 IS SUGGESTED FOR PUBLICATION)