

(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property
Organization
International Bureau

(43) International Publication Date
26 September 2024 (26.09.2024)



(10) International Publication Number
WO 2024/196515 A1

(51) International Patent Classification:
G06F 13/42 (2006.01)

(21) International Application Number:
PCT/US2024/015567

(22) International Filing Date:
13 February 2024 (13.02.2024)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
18/187,259 21 March 2023 (21.03.2023) US

(71) Applicant: **QUALCOMM INCORPORATED** [US/US];
ATTN: International IP Administration, 5775 Morehouse
Drive, San Diego, California 92121-1714 (US).

(72) Inventors: **VUONG, Hung**; 5775 Morehouse Drive, San
Diego, California 92121-1714 (US). **BABU, Benish**; 5775
Morehouse Drive, San Diego, California 92121-1714 (US).

(74) Agent: **SMITH, Darren**; Norton Rose Fulbright US LLP,
2200 Ross Avenue, Suite 3600, Dallas, Texas 75201 (US).

(81) Designated States (*unless otherwise indicated, for every
kind of national protection available*): AE, AG, AL, AM,
AO, AT, AU, AZ, BA, BB, BG, BH, BN, BR, BW, BY, BZ,
CA, CH, CL, CN, CO, CR, CU, CV, CZ, DE, DJ, DK, DM,
DO, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT,
HN, HR, HU, ID, IL, IN, IQ, IR, IS, IT, JM, JO, JP, KE, KG,
KH, KN, KP, KR, KW, KZ, LA, LC, LK, LR, LS, LU, LY,
MA, MD, MG, MK, MN, MU, MW, MX, MY, MZ, NA,
NG, NI, NO, NZ, OM, PA, PE, PG, PH, PL, PT, QA, RO,
RS, RU, RW, SA, SC, SD, SE, SG, SK, SL, ST, SV, SY, TH,
TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, WS,
ZA, ZM, ZW.

(54) Title: PHYSICAL INTERFACE CONFIGURATION BUFFER IN A FLASH MEMORY SYSTEM

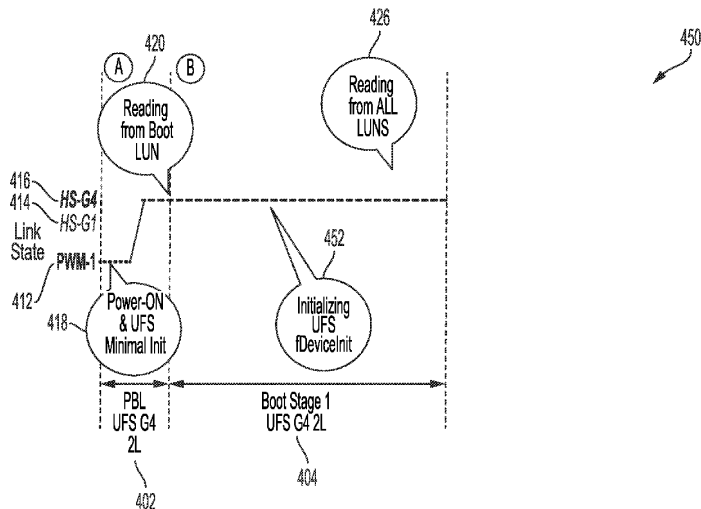


FIG. 4B

(57) **Abstract:** This disclosure provides systems, methods, and devices for memory systems that support updating a configuration of a physical layer interface (PHY) using information stored in a buffer of a connected memory system. In a first aspect, a method of accessing data in a flash memory system includes initializing, by a memory controller of a host device, a PHY for connecting the host device to a memory system to operate at a first speed, receiving PHY configuration information for configuring the PHY to operate at a second speed, greater than the first speed, from a first buffer of the memory system, and adjusting, by the memory controller, a configuration of the PHY in accordance with the PHY configuration information to operate at the second speed. Other aspects and features are also claimed and described.

[Continued on next page]

(84) Designated States (*unless otherwise indicated, for every kind of regional protection available*): ARIPO (BW, CV, GH, GM, KE, LR, LS, MW, MZ, NA, RW, SC, SD, SL, ST, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, RU, TJ, TM), European (AL, AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HR, HU, IE, IS, IT, LT, LU, LV, MC, ME, MK, MT, NL, NO, PL, PT, RO, RS, SE, SI, SK, SM, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, KM, ML, MR, NE, SN, TD, TG).

Declarations under Rule 4.17:

- *as to applicant's entitlement to apply for and be granted a patent (Rule 4.17(ii))*
- *as to the applicant's entitlement to claim the priority of the earlier application (Rule 4.17(iii))*

Published:

- *with international search report (Art. 21(3))*