



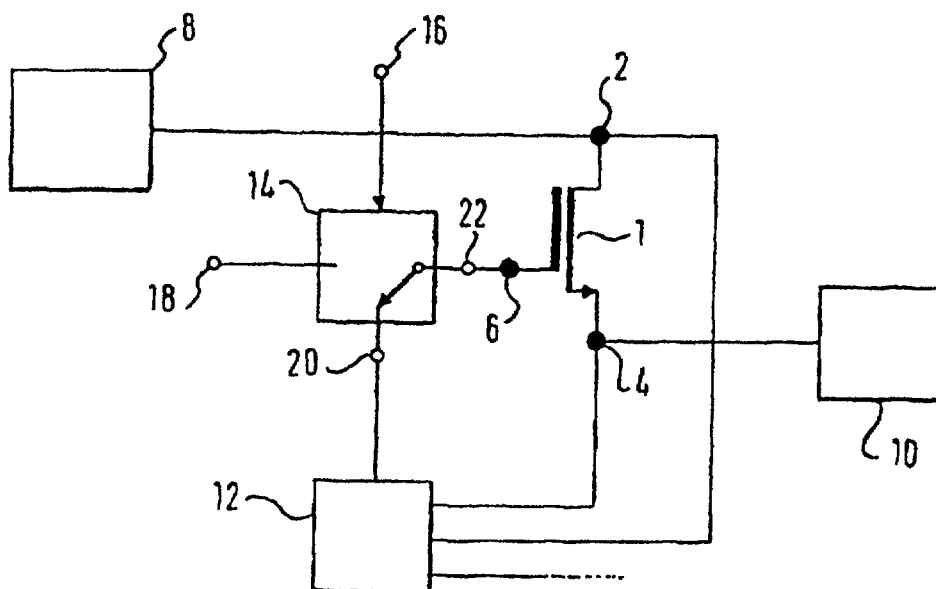
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(54) Title: FAILSAFE INTERFACE CIRCUIT



(57) Abstract

A failsafe interface circuit comprises at least one semiconductor switching circuit (1) with a first link terminal (2), a second link terminal (4) and a control terminal (6). To connect a first and second circuit (8, 10) attached to the first and second link terminal (2, 4), respectively, a potential difference between the control terminal (6) and one of the link terminals (2, 4) is raised above a predetermined threshold value. To avoid any flow of current from the second circuit (10) to the first circuit (8) or vice versa when the interface circuit is powered off, the maximum potential at the first and second link terminal (2, 4) is actively fed back to the control terminal (6) of the semiconductor switching circuit (1).