CLAIMS

1. An integrated circuit device, comprising:

an interposer structure and two or more active components carried by said interposer structure, and said interposer structure includes an interposer substrate including a certain semi-conductor material and a plurality of vias formed in the substrate;

wherein said two or more active components include at least two components, which are respectively constructed of at least two different semiconductor materials, carried by at least two different respective regions of the interposer structure, said two or more active components include at least one active component, whose semi-conductor materials are different than the certain semi-conductor material of the interposer substrate and have a coefficient of thermal expansion (CTE) different than a CTE of the certain semi-conductor material of the interposer substrate;

wherein said interposer structure includes at least two different respective arrangements of the vias in said at least two different respective regions of the interposer structure, at which said at least two components of the at least two different semiconductor materials are located;

wherein said vias having CTEs substantially different than the CTE of the interposer substrate; and

wherein configurations of said at least two different arrangements of the vias are different with respect to at least one parameter of the arrangements such that effective CTEs of the interposer structure, including the interposer substrate and the arrangements of vias at said at least two different respective regions, respectively match the CTEs of the semiconductor materials of the respective at least two components that are carried by the interposer structure at said at least two regions respectively, thereby providing that said interposer structure with said at least two active components of the at least two different semiconductor materials being mechanically stable under varying temperature conditions.

2. The integrated circuit device of claim 1 wherein said interposer structure is configured as an active interposer in which at least one of the two or more active components is implemented as an active component integrated with said interposer structure and thereby being carried by said interposer.

3. The integrated circuit device of claim 1 wherein said interposer structure is mechanically stable under extreme temperature conditions ranging between -65°C to 150°C.

4. The integrated circuit device of claim 1 wherein said components of at least two different semiconductor materials include at least two of the following semiconductor materials: Si, SiGe, SiC, GaAs, or GaN.

5. The integrated circuit device of claim 1 wherein said spaced-apart vias include conductive vias electrically connected with said two or more active components by at least one of the following: wire-bonding or flip-chip electrical connections.

6. The integrated circuit device of claim 5 wherein said interposer structure includes one or more Redistribution Layers (RDLs) furnished on at least a bottom surface of the interposer structure for providing wiring connections to the conductive vias of the interposer structure.

7. The integrated circuit device of claim 1 wherein said interposer structure includes silicon (Si) based interposer substrate with an arrangement of Copper (Cu) vias formed therein.

8. The integrated circuit device of claim 1, wherein the mechanical stability of the interposer structure allows carrying said active components of sizes up to about 25x25 mm.

9. The integrated circuit device of claim 1 , further comprising:

at least one metal cap that is furnished on said top surface of the interposer structure; and

wherein lateral dimensions, thickness, and material composition of said at least one metal cap are configured and to endure tensions and/or stresses affected between a boundary of the interposer structure and the at least one metal cap under the varying temperature conditions, thereby enforcing the structural integrity and mechanical stability of said interposer structure.

10. The integrated circuit device of claim 9 wherein said material composition of said at least one metal cap is similar to a material composition of vias formed in a substrate of the interposer structure.

11. The integrated circuit device of claim 1 wherein a bonding material used for furnishing said active components carried by the interposer structure is elastic for enduring stresses that may occur under said varying temperature conditions due to a difference in coefficients of thermal expansion between the active components and the interposer structure.

12. The integrated circuit device of claim 1 wherein the interposer structure is configured in at least one of the following configurations providing improved heat evacuation from the active components mounted thereon:

(a) said interposer substrate includes a material having relatively high thermal conductivity; and

(b) at least some of the vias are formed from a material having relatively high thermal conductivity and wherein locations and lateral dimensions of at least some of the vias are selected in accordance with locations and characteristic sizes of at least some of the pattern features within at least one active component which are associated with substantial heat emission, thereby providing sufficient thermal coupling between the at least some vias and said features allowing diffusion of heat therefrom during operation under extreme temperatures conditions.

13. The integrated circuit device of claim 12 wherein said at least one active component is a signal amplifier component associated with substantial heat emission.

14. The integrated circuit device of claim 1 , further comprising:

at least one metal cap that is furnished on said top surface of the interposer structure and encapsulates at least one active component of said two or more active components;

wherein said at least one active component is configured to operate with high frequency signals; and

wherein said at least one metal cap is configured to define a cavity providing a sufficient gap between said at least one active component and other dielectric materials of said integrated circuit device such that electrical impedance of said at least one active component is substantially not affected by said other dielectric materials thereby facilitating proper operation of said one active component.

15. The integrated circuit device of claim 14, wherein said at least one active component encapsulated by the metal cap is a high frequency component operating with high frequency signals, and wherein electrical connection in between certain vias in a substrate of said interposer structure and said high frequency component are configured as RF connections utilizing balanced RF lines.

16. The integrated circuit device of claim 1 , further comprising:

at least one metal cap that is furnished on said top surface of the interposer structure and encapsulates at least one active component of said two or more active components;

a vent opening defined in the metal cap for preventing pressure build up in a cavity between the metal cap and said interposer structure under the varying temperature conditions; and

a mold layer covering the top surface of the interposer structure with said at least one metal cap;

wherein said metal cap thereby provides a near hermetically sealed packaging of said at least one active component that is suitable for operating said at least one active component under said varying temperature conditions and under various humidity conditions.

17. A method for manufacturing an integrated circuit device, the method comprising:

providing an interposer substrate of a certain semi-conductor material; and

implementing one or more arrangements of spaced apart vias in the interposer substrate to generate an interposer structure including at least the interposer substrate and the vias;

wherein said arrangements of said vias include at least one arrangement of vias is located at a certain region of said interposer structure at which an active component of semi-conductor material different than said certain semi-conductor material of the interposer substrate is to be carried by the interposer structure;wherein the vias of said at least one arrangement having CTEs substantially different than the CTE of the interposer substrate; and

wherein at least one parameter of said at least one arrangement of vias is selected such that effective coefficient of thermal expansion (CTE) of the interposer structure including the interposer substrate and the arrangement of vias at said certain region, match CTE of the semi-conductor material of said active component; said at least one parameter including at least one of the following: diameters of the vias; pitches of the vias in said arrangements of vias; materials of said vias; or fraction of a surface area covered by the vias.

18. The method according to claim 17 wherein the interposer substrate carries at least one additional active component that is made of a semi-conductor material similar to said certain semiconductor material of the interposer substrate and wherein the at least one of the following:

a) said interposer structure is a passive interposer and the method comprises providing and mounting said at least one additional active component on the interposer structure;
b) said interposer structure is an active interposer including at least one of the active components implemented thereon.

19. The method according to claim 17, further comprising configuring at least one of the locations and dimensions of one or more of said vias to provide heat evacuation from one or more features of at least one said active component that are associated with substantial heat emission.

20. The method according to claim 17, further comprising:

providing said at least one active component of said semi-conductor material different than said certain semi-conductor material of the interposer substrate; and

mounting said at least one active component at said region of the interposer structure.

21. The integrated circuit device of claim 1 wherein said at least one parameter includes at least one of the following: diameters of the vias; pitches of the vias in said arrangements of vias; materials of said vias; or fraction of a surface area covered by the vias.

22. An integrated circuit device, comprising:

an interposer structure comprising an interposer substrate of a certain semi-conductor material, and a plurality of vias formed in the interposer substrate; and

an active component formed with a semi-conductor material different than said certain semi-conductor material of the interposer substrate and being carried at a certain region of said interposer structure;

wherein a coefficient of thermal expansion (CTE) of the semi-conductor material of the active component is different than a CTE of the interposer substrate; and

wherein said certain region of the interposer structure, at which said active component being carried, comprises a spaced apart arrangement of one or more of said vias whereby CTEs of said vias are substantially different than the CTE of the interposer substrate, and wherein at least one parameter of said spaced apart arrangement is configured such that effective the CTE of the interposer structure including the interposer substrate and the spaced apart arrangement of said vias in said certain region, matches said CTE of the semi-conductor material of the active component being carried at said certain region,

thereby enabling the interposer structure and the active component carried thereby toremain mechanically stable under varying temperature condition despite a CTE mismatch between the interposer substrate and the active component.

23. The integrated circuit device, of claim 22 wherein said at least one parameter includes at least one of the following: diameters of the vias; pitches of the vias in said arrangements of vias; materials of said vias; or fraction of a surface area covered by the vias.

24. The integrated circuit device of claim 1 wherein said at least one parameter comprises at least one of the following: (i) diameters of the vias, (ii) pitches of the vias in said arrangements of vias, (iii) materials of said vias, or (iv) fraction of a surface area covered by the vias; thereby providing different effective coefficients of thermal expansion (CTEs) of the interposer structure at said at least two different respective regions that are matching the CTEs of the semiconductor materials of the respective components in said at least two regions.