ULTRA-THIN STACKED GATE DIELECTRIC STRUCTURE

ABSTRACT

An embodiment of the instant invention is a method of forming a transistor which includes a gate dielectric (layer 112) which is situated between a gate structure (structure 114) and a semiconductor substrate (substrate 110), the method comprising the steps of: growing [step 206] a nitrogen-containing layer (layer 118) on the substrate; depositing [step 208] a first oxygen-containing layer (layer 116) on the first nitrogen-containing layer; growing [step 210] a second oxygen-containing layer (layer 120) between the substrate and the first nitrogen-containing layer; and wherein the steps of growing the nitrogen-containing layer, depositing the first oxygen-containing layer, and growing the second oxygen-containing layer are all performed in a single processing chamber. Preferably, the nitrogen-containing layer is comprised of N_2O; the first oxygen-containing layer is comprised of DCS/N_2O; and the second oxygen-containing layer is comprised of SiO_2. The step of growing the second oxygen-containing layer is, preferably, performed after the steps of growing the nitrogen-containing layer and the depositing of the first oxygen-containing layer.

Figure 1