## CLAIMS

What is claimed is:

1. An apparatus comprising:

switch controller circuitry to control a conduction state of a first switch and a second switch in a DC to DC converter; and

dead time logic circuitry to determine an estimated dead time interval between a turn off of the first switch and a turn on of the second switch, the first switch and the second switch coupled at a switched node, wherein the estimated dead time interval is determined based, at least in part, on

a difference between an input voltage, Vin, and a switched voltage, Vsw, detected at the switched node just prior to turning off the first switch, wherein Vin and Vsw are differentially clocked by differential clocking circuitry in the apparatus;

a parasitic capacitance, Cpar, associated with the switched node, wherein Cpar is estimated based on the apparatus configuration or by delay adjustment logic circuitry in the apparatus; and

a maximum inductor current, $I_{L,max}$, the difference between Vin and Vsw representing the maximum inductor current, wherein $I_{L,max}$ is determined based on a digital code generated by dead time calculation circuitry in the apparatus,

wherein the dead time logic circuitry comprises the differential clocking circuitry and phase comparator circuitry, the differential clocking circuitry to receive the input voltage and the switched voltage as inputs and to provide a first clocked signal and a second clocked signal as outputs, a phase difference between the first clocked signal and the second clocked signal representing the difference between Vin and Vsw, the phase comparator circuitry to determine the phase difference.

2. The apparatus of claim 1, wherein the phase comparator circuitry comprises a first plurality of D flip flops and a second plurality of offset circuitries.

3. The apparatus of claim 1, wherein the dead time is determined as $T = Cpar*Vin/I_{L,max}$, and $I_{L,max}$ corresponds to the maximum inductor current just prior to the first switch turning off, $I_{L,max}$ estimated based, at least in part, on the difference between Vin and Vsw and the switch controller circuitry is to set a dead time to the estimate in a same PWM (pulse width modulation) cycle as the estimated dead time interval was determined.

4. The apparatus of claim 1, wherein an output of the phase comparator circuitry is a digital code corresponding to the phase difference.

5. The apparatus of claim 1, wherein the switch controller circuitry further comprises delay adjustment logic circuitry to determine whether the estimated dead time interval is greater than or less than an optimal dead time interval based, at least in part, on the switched voltage and based, at least in part, on a control input to the second switch.

6. The apparatus of claim 5, wherein the delay adjustment logic circuitry comprises a NOR gate to detect whether the estimated dead time interval is greater than the optimal dead time interval and an AND gate to detect whether the estimated time interval is less than the optimal dead time interval.

7. The apparatus of claim 2, wherein a respective delay time of at least some offset circuitries of the plurality of offset circuitries is a respective whole number multiple of a delay increment $\Delta t$.

8. The apparatus of claim 7, wherein the delay increment is related to a minimum resolution for the difference between Vin and Vsw.

9. A method comprising:

controlling, by switch controller circuitry, a conduction state of a first switch and a second switch in a DC to DC converter; and

determining, by dead time logic circuitry, an estimated dead time interval between a turn off of the first switch and a turn on of the second switch, the first switch and the second switch coupled at a switched node, the estimated dead time interval determined based, at least in part, on a difference between an input voltage, Vin, and a switched voltage, Vsw, detected at the switched node just prior to turning off the first switch, wherein Vin and Vsw are differentially clocked by differential clocking circuitry in an apparatus; a parasitic capacitance, Cpar, associated with the switched node, wherein Cpar is estimated based on the apparatus configuration or by delay adjustment logic circuitry in the apparatus; and a maximum inductor current, $I_{L,max}$, the difference between Vin and Vsw representing the maximum inductor current, wherein $I_{L,max}$ is determined based on a digital code generated by dead time calculation circuitry in the apparatus; and

receiving, by the differential clocking circuitry, the input voltage and the switched voltage as inputs; providing, by the differential clocking circuitry, a first clocked signal and a second clocked signal as outputs; and determining, by phase comparator circuitry, a phase difference between the first clocked signal and the second clocked signal, the phase difference representing the difference between Vin and Vsw.

10. The method of claim 9, wherein the phase comparator circuitry comprises a first plurality of D flip flops and a second plurality of offset circuitries.

11. The method of claim 9, further comprising setting, by the switch controller circuitry a dead time to the estimate in a same PWM (pulse width modulation) cycle as the estimated dead time interval was determined, the estimated dead time determined as T = Cpar*Vin/$I_{L,max}$, and $I_{L,max}$ corresponds to the maximum inductor current just prior to the first switch turning off, $I_{L,max}$ estimated based, at least in part, on the difference between Vin and Vsw.

12. The method of claim 9, wherein an output of the phase comparator circuitry is a digital code corresponding to the phase difference.

13. The method of claim 9, further comprising determining, by delay adjustment logic circuitry, whether the estimated dead time interval is greater than or less than an optimal dead time interval based, at least in part, on the switched voltage and based, at least in part, on a control input to the second switch.

14. The method of claim 13, further comprising detecting, by a NOR gate, whether the estimated dead time interval is greater than the optimal dead time interval and detecting, by an AND gate, whether the estimated time interval is less than the optimal dead time interval.

15. The method of claim 10, wherein a respective delay time of at least some offset circuitries of the plurality of offset circuitries is a respective whole number multiple of a delay increment $\Delta t$.

16. A system comprising:

DC to DC converter circuitry;

switch controller circuitry to control a conduction state of a first switch and a second switch in a DC to DC converter; and

dead time logic circuitry to determine an estimated dead time interval between a turn off of the first switch and a turn on of the second switch, the first switch and the second switch coupled at a switched node, the estimated dead time interval determined based, at least in part, on a difference between an input voltage, Vin, and a switched voltage, Vsw, detected at the switched node just prior to turning off the first switch, wherein Vin and Vsw are differentially clocked by differential clocking circuitry in the apparatus; a parasitic capacitance, Cpar, associated with the switched node, wherein Cpar is estimated based on the apparatus configuration or by delay

adjustment logic circuitry in the apparatus; and a maximum inductor current, $I_{L,max}$, the difference between Vin and Vsw representing the maximum inductor current, wherein $I_{L,max}$ is determined based on a digital code generated by dead time calculation circuitry in the apparatus,

wherein the dead time logic circuitry comprises the differential clocking circuitry and phase comparator circuitry, the differential clocking circuitry to receive the input voltage and the switched voltage as inputs and to provide a first clocked signal and a second clocked signal as outputs, a phase difference between the first clocked signal and the second clocked signal representing the difference between Vin and Vsw, the phase comparator circuitry to determine the phase difference.

17. The system of claim 16, wherein the phase comparator circuitry comprises a first plurality of D flip flops and a second plurality of offset circuitries.

18. The system of claim 16, wherein the dead time is determined as T = Cpar*Vin/$I_{L,max}$, and $I_{L,max}$ corresponds to the maximum inductor current just prior to the first switch turning off, $I_{L,max}$ estimated based, at least in part, on the difference between Vin and Vsw and the switch controller circuitry is to set a dead time to the estimate in a same PWM (pulse width modulation) cycle as the estimated dead time interval was determined.

19. The system of claim 16, wherein an output of the phase comparator circuitry is a digital code corresponding to the phase difference.

20. The system of claim 16, wherein the switch controller circuitry further comprises delay adjustment logic circuitry to determine whether the estimated dead time interval is greater than or less than an optimal dead time interval based, at least in part, on the switched voltage and based, at least in part, on a control input to the second switch.

21. The system of claim 20, wherein the delay adjustment logic circuitry comprises a NOR gate to detect whether the estimated dead time interval is greater than the optimal dead time interval and an AND gate to detect whether the estimated time interval is less than the optimal dead time interval.

22. The system of claim 17, wherein, a respective delay time of at least some offset circuitries of the plurality of offset circuitries is a respective whole number multiple of a delay increment $\Delta t$.