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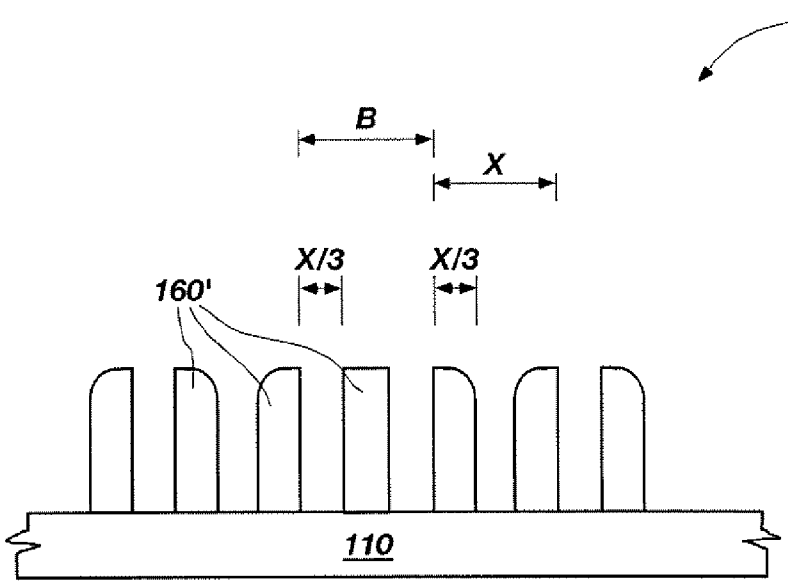
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(54) **Title:** METHODS TO REDUCE THE CRITICAL DIMENSION OF SEMICONDUCTOR DEVICES AND PARTIALLY FABRICATED SEMICONDUCTOR DEVICES HAVING REDUCED CRITICAL DIMENSIONS



(57) **Abstract:** A method of forming features on a target layer. The features have a critical dimension that is triple- or quadruple-reduced compared to the critical dimension of portions of a resist layer used as a mask. An intermediate layer is deposited over a target layer and the resist layer is formed over the intermediate layer. After patterning the resist layer, first spacers are formed on sidewalls of remaining portions of the resist layer, masking portions of the intermediate layer. Second spacers are formed on sidewalls of the portions of the intermediate layer. After removing the portions of the intermediate layer, the second spacers are used as a mask to form the features on the target layer. A partially fabricated integrated circuit device is also disclosed.

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