DIGITAL DEMODULATION CIRCUIT

BACKGROUND OF THE INVENTION

1. Field of the Invention

The present invention relates to a digital demodulator for demodulating signal waves modulated by digital signals, and also relates to AFC (Automatic Frequency Control) circuits, clock recovery circuits and bit error estimation circuits respectively used for that digital demodulator.

2. Prior Art

Digitization of communication has been studied and realized in the field of data transfer for communication on wires, such as telephone circuits, microwave communication or optical communication between base stations. Also, digitization of mobile communication for automobile telephones or portable telephones whose development has been delayed so far is studied extensively.

As the well-known method of modulating or demodulating digital signals, there can be mentioned the amplitude modulation for changing the amplitude of carrier waves corresponding to state of each digital signal and the so-called angle modulation for changing its phase or frequency.

In the field of digital mobile communication, generally, the angle modulation method which is not susceptible to amplitude distortion due to the signal transfer route is used.

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The angle modulation is now described in brief with respect to the so-called $\pi/4$ shift quadrature phase shift keying ($\pi/4$ shift QPSK) method which is excellent in withstandability to distortion and suitable for the mobile communication.

Fig. 16 is a block diagram showing fundamental construction of the $\pi/4$ shift QPSK system.

Serial/parallel converter 1 converts a row of binary digital data into 2-bit unit data (X, Y). The unit data is called one symbol used as one cycle of data processing. Differential coding circuit 2 produces a base band signal consisting of I and Q channels to which the information of (X, Y) is given respectively corresponding to the change (difference) in signals. The band of the base band signal is limited by low-pass filters (LPF) 3, 4. Thus, amplitude modulation is carried out by multiplying the in-phase and quadrature phase components of carrier wave ω_c by the band-limited base band signal respectively, and a modulation wave is then obtained by synthesizing both the products.

In case of the phase modulation by the above $\pi/4$ shift QPSK system, amplitude values "A", "-A" are assigned respectively to the binary signals "1", "0", and four signal-point data (I, Q) are given for one symbol to perform the quadrature phase shift keying. Namely, as shown by the signal-point arrangement with respect to I, Q in Fig. 17, the phase modulation is performed using the signal-point arrangement of QPSK designated by blackened

circles (●) and the corresponding $\pi/4$ shifted signal-point arrangement designated by normal circles (○) alternately at each symbol interval. Accordingly, each phase difference $\Delta\Phi$ between the two consecutive symbols always becomes odd times the shift of $\pi/4$ so that the relation between $\Delta\Phi$ and the input unit data (X, Y) can be expressed as shown in Fig. 17(b).

As the method of demodulating a modulation wave, the synchronous detection method and delay detection method are well-known. Theoretically, the synchronous detection method has excellent properties, but is likely to generate disadvantageously high-speed fading. Thus, the delay detection method is more preferred, in particular, in case of digital mobile communication where a sudden phase change often occurs.

In the delay detection method, a new modulation wave is detected based on the previous modulation wave delayed by a delay circuit provided with a predetermined delay time. Therefore, these modulation waves should be modulated by a signal processed by the differential coding as described above. In addition, the regeneration of the carrier wave becomes unnecessary. Accordingly, as compared to the synchronous detection method, the delay detection method can be constructed more simply and more suitable for the mobile communication.

For example, in case of the aforementioned $\pi/4$ shift QPSK, the phase difference $\Delta\Phi$ between any given two consecutive modulation waves is obtained by detecting the

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new modulation wave based on the phase of the previous modulation wave preceding by one symbol, and is then coded in accordance with the data of Fig. 17(b).

Fig. 18 is a block diagram showing one example of conventional digital demodulator for demodulating the $\pi/4$ shift QPSK modulation wave utilizing the delay detection method.

As shown in the same drawing, the phase modulation wave is converted into a base band signal consisting of I and Q channels respectively corresponding to a first signal having the same frequency as that of the carrier wave ω_c and a second signal shifted by $\pi/2$ from the first signal. Then, these I and Q signals are digitized by analog/digital converter (A/D) 7, 8 through low-pass filters 5, 6, respectively.

Thereafter, the digitized signals I and Q are decoded into X, Y based on the relation of Fig. 17(b) after detecting the difference of the signal-point arrangement to the signal preceding by one symbol, that is, the phase difference $\Delta\Phi$ through delay detection circuit 9.

From the delay detection circuit 9, the resultant detection signals are sent to data discrimination portions 11, 12 and clock recovery circuit 13, respectively. The clock recovery circuit 13 determines a timing point as will be described below, and supplies a timing clock signal based on that timing point to the data discrimination portions 11, 12 for each one symbol cycle. The data discrimination portions 11, 12 fix the fundamental data (X,

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Y) using the detection signal based on the timing clock signal. Thereafter, the fundamental data (X, Y) is demodulated by parallel/serial converter 14 into a row of binary data as before the modulation process.

Fig. 19 shows an eye pattern obtained by overlapping the detection signals derived from the X output terminal of the delay detection circuit 9. Generally, the signal level at point (timing point) 10 on which the eye for fixing the binary signal (X = 1 or 0) opens most widely is discriminated as the demodulation data for each symbol.

The most important in the above demodulation process is how to determine the timing point. Namely, the conventional clock recovery circuit determines the timing point to produce a timing clock signal. In that case, the so-called zero-cross detection method is generally known as a method of obtaining such a timing point. According to this method, the detection signal is taken out from one output terminal of the delay detection circuit 9 to detect the zero-cross point, at which the signal level crosses 0 (substantially the middle point between the two binary levels), designated by reference numeral 15 in Fig. 19. Then, the points 10 respectively shifted by 1/2 symbol cycle from the zero-cross point 15 are obtained and sent to the data discrimination portion 11, 12 as the timing point signal.

However, in case of such a clock recovery circuit for detecting the timing point using the zero-cross point as mentioned above, the point crossing 0 is distributed in

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a relatively wide range as denoted by Δt in the eye patten of Fig. 19. Therefore, it is difficult to accurately fix the zero-point. If the timing point is determined as the point shifted by 1/2 symbol from that inaccurate zero-cross point, the points at which the eye would be considered to open most widely shift from the most desired points, thereby causing increase of bit error occurrence. Therefore, in a general way, a plurality of zero-cross points must be read to fix their middle value as the real or accurate zero-cross point. However, such a method of fixing the zero-cross point takes much time.

Such inconvenience of this method becomes more noticeable in such a digitized system for radio communication which will be put into practice soon because this system requires frequent change of communication channels and fixing of the aforementioned timing point for each change of channels.

Japanese Patent Application for Disclosure HEI-3-205940 teaches a method in which such digital radio communication is considered first. Namely, in this method, the signal points I, Q of the base band signal to be obtained by a quasi-synchronous detection of the preceding modulation wave are determined respectively on the I-Q coordinate plane. If these signal points deviate from a predetermined signal point arrangement, synchronous correction is carried out by shifting each phase by changing the delay time of the detection circuit so as to correct these positions into originally estimated

positions. For example, if the detected signal point is located at a position designated by × in Fig. 20, the shift length is determined by estimating that the point × should be point P which is the nearest to the point × of those shown in Fig. 20.

However, in such a method, the possibility of wrong correction becomes considerably high for each one symbol detection if the deviation of the detected signal points from the predetermined point arrangement is too large to make the estimation reasonable. Therefore, it takes much time to complete such synchronous correction.

Fig. 21 is a block diagram in which AFC circuit 27 is added to the digital demodulator for demodulating the $\pi/4$ shift QPSK modulation wave as shown in Fig. 18. In that device, an intermediate frequency signal is produced by mixing the modulation wave with a reference frequency, and is then input into phase quantization circuit 22 through band-pass filter 20 and limiter 21. Thereafter, the quantized signal from the quantization circuit 22 is used to obtain phase difference based on the signal preceding by one symbol using delay detection circuit 23 having a delay time corresponding to one symbol cycle.

The so-obtained phase difference signal is decoded into digital signals X, Y by decoding circuit 24, and these signals X, Y are then fixed based on a timing clock signal from clock recovery circuit 25. Thus, a demodulation signal is obtained by converting these fixed signals into a series of data by parallel/serial converter 26.

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In case of the $\pi/4$ shift QPSK modulation wave, the resultant phase point after the delay detection should be one of the four circles as shown in Fig. 22(a). However, when frequency drift occurs, the phase point takes either one of positions as designated by × in Fig. 22(b). Thus, the phase shift between the positions of Figs. 22(a) and 22(b) corresponds to the magnitude of frequency drift for one symbol.

Accordingly, the AFC circuit 27 is generally added to correct such frequency drift in the modulation wave. The degree of phase shift is estimated by counting the output of delay detection circuit 23 using up-down counter 28. Then, the count value is subjected to digital/analog conversion through filter 29. Thereafter, the frequency of VCXO 30 for generating the aforementioned reference frequency is so changed that the position of the phase point can coincide with either one of the circles as shown in Fig. 22.

However, even in such an improved system, it is also possible that the phase point which should correctly take the position of circle A emerges at the position × near the wrong position B as shown in Fig. 23 due to considerably large frequency drift. As a result, the AFC circuit 27 carries out wrong correction judging that the position B is the aimed phase point. Therefore, the possibility of obtaining wrong demodulation data still remains high.

Further, in case of mobile communication, base

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stations are generally placed in fixed areas respectively, and each mobile station performs communication through these base stations. For example, as shown in Fig. 24, mobile station 35 selects one station in the best circuit state to perform communication from base stations A, B and C located near the mobile station.

In this case, as the means for judging whether or not the communication circuit is in a good state, there is a method of comparing the electric field strength of the wave to be transmitted from each base station or a method of measuring the bit error rate (BER) capable of detecting the circuit state including noises or the like factors as well as the synchronous state of the demodulator. Generally, either one or combination of these two methods is used for that purpose.

As a generally-known method of measuring the bit error rate, there can be mentioned a method as shown in Fig. 25(a) in which a series of data (N bits) for measuring a specific bit error rate are inserted in advance at a predetermined interval in a series of information data formed by digitizing information, such as voice or the like elements, on the transmission side, and the bit error rate (n/N) is calculated by detecting the number of bits (n) wrongly received from the series of data for measuring the bit error rate when the demodulation is performed on the reception side. It is also possible to use a method as shown in Fig. 25(b) in which a parity bit is inserted in each group consisting of a plurality of bits (8 bits in the

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drawing) as a series of information data so as to estimate the bit error rate by the parity check on the reception side.

However, in such a method of measuring the bit error rate, the series of data or parity bit for measuring the bit error rate must be inserted in the series of information data, thereby degrading the communication efficiency. In the former method, in particular, transmission of a series of information data must be discontinued during transmission of the series of data for measuring the bit error rate.

The present invention was made to solve the problems in the clock recovery circuit, AFC circuit and bit error rate estimation means used in the aforementioned conventional digital demodulator and demodulation circuit.

The first object of the present invention is to provide a clock recovery circuit capable of producing desired demodulation signals and a digital demodulator including the clock recovery circuit.

The second object of the present invention is to provide a bit error rate estimation means which does not require any insertion of a specific series of data other than information data on the transmission side and can suppress the degradation of transmission efficiency to a minimum.

The third object of the present invention is to provide an AFC circuit capable of performing well-directed and suitable correction even in case of considerably large

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frequency drift.

SUMMARY OF THE INVENTION

To achieve the first object, the present invention provides a clock recovery circuit of the digital demodulator for detecting a modulation wave by predetermined detection means, comprising correlation detection means for sampling a signal in the demodulation process for each unit data cycle (symbol cycle) at a plurality of sampling points fixed in advance and detecting correlations between two adjacent sampling points; and correlation judgement means for comparing the correlations detected by the correlation detection means and deciding a pair of sampling points providing the largest correlation and producing a timing clock signal based on the judgement of the pair of sampling points providing the largest correlation.

Alternatively, the clock recovery circuit to achieve the first object may comprise correlation detection means for sampling a signal in the demodulation process for each unit data cycle (symbol cycle) at a plurality of sampling points fixed in advance and detecting correlations between two adjacent sampling points; correlation judgement means for comparing the correlations detected by the correlation detection means, deciding a pair of sampling points providing the largest correlation and another pair of sampling points providing the next largest correlation and producing a timing clock signal based on the judgement; and

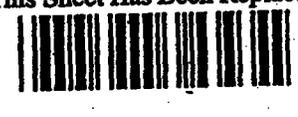
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phase shift means for shifting the phase of the digital signal so as to equalize the correlations of the two pairs of sampling points.

To achieve the second object, the present invention provides a bit error estimation means of the digital demodulator for demodulating a modulation wave detected by predetermined detection means, which samples a signal in the demodulation process for each unit data cycle (symbol cycle) at a plurality of sampling points fixed in advance and detects correlations between two adjacent sampling points so as to estimate the bit error rate based on the distribution of the detected correlations.

To achieve the third object, the present invention provides an AFC circuit of the digital demodulator for demodulating a modulation wave detected by predetermined detection means, comprising a bit error rate estimation means for sampling a signal in the demodulation process for each unit data cycle (symbol cycle) at a plurality of sampling points fixed in advance and detecting correlations between two adjacent sampling points so as to estimate the bit error rate based on the distribution of the detected correlations; a bit error rate measuring device for measuring each bit error rate based on a series of bit error rate measuring data inserted in the modulation wave at a predetermined interval, thereby correcting the frequency drift of the modulation wave by comparing the two bit error rates.

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BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a block diagram showing one example of the construction in which an embodiment of the clock recovery circuit of this invention is applied to a digital demodulator.

Fig. 2 is a block diagram showing one example of the construction of the correlation detection circuit.

Fig. 3 shows input-output characteristics of an XOR gate.

Fig. 4 is a block diagram showing a second embodiment of the digital demodulator according to the present invention.

Figs. 5(a) and 5(b) show the operation of a phase quantization circuit, respectively.

Fig. 6 is a block diagram showing another embodiment of the digital demodulator device according to the present invention.

Fig. 7 is an eye pattern of a detection signal in the demodulation process.

Fig. 8 shows one example of fixing the sampling points.

Figs. 9(a) and 9(b) show the relation between the bit error rate and E_b/N_o and between that rate and sampling points, respectively.

Fig. 10 shows distribution of correlation values over the respective sampling points.

Fig. 11 is a block diagram showing construction in which one embodiment of the bit error rate estimation means

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related to this invention is applied to the digital demodulator.

Fig. 12 is a block diagram showing one example of construction of the correlation detection circuit.

Fig. 13 is a graph showing results of simulation for the bit error rate measurement.

Fig. 14 is a block diagram showing construction in which one embodiment of the AFC circuit related to this invention is applied to the digital demodulator.

Fig. 15 shows one example of construction of the bit error rate estimation means.

Fig. 16 is a block diagram showing a standard construction of the $\pi/4$ shift QPSK modulator.

Fig. 17(a) and 17(b) show a $\pi/4$ shift QPSK demodulation method, respectively.

Fig. 18 is a block diagram showing a standard construction of the conventional demodulator.

Fig. 19 is an eye pattern of a detection signal.

Fig. 20 shows conventional phase shift estimation means.

Fig. 21 is a block diagram showing a $\pi/4$ shift QPSK modulator.

Fig. 22(a) and 22(b) show a change of the phase point to be caused by frequency drift, respectively.

Fig. 23 shows a relatively large-scale change of the phase point caused by frequency drift.

Fig. 24 schematically shows a mobile communication system.

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Fig. 25 shows a conventional method of measuring the bit error rate.

Fig. 26 shows an example of fixing the sampling points.

DETAILED DESCRIPTION OF THE PRESENT INVENTION

Hereinafter, several embodiments related to this invention will be described in detail with reference to the drawings.

As is seen by the eye pattern in Fig. 19, at timing point 10 on which the eye opens most widely, the level of detection signal becomes a or -a (X = 1 or 0) at which it is focused with a relatively high density, and is kept at substantially the same level in the vicinity of point 10. Contrary, in the vicinity of point 15 or location farther from the timing point 10, the probability of discordance in that level becomes high.

Namely, by fixing a plurality of sampling points with respect to a detection signal for one symbol cycle and sampling the signal level at each sampling point so as to determine the correlation between the signal levels at each adjacent pair of the sampling points, the correlation becomes large in the vicinity of the timing point where the signal levels are substantially the same, while becomes small in the area where those levels of two sampling points are distinctly different. In other words, the correlation is relatively large at point 10 in Fig. 19, while small at point 15.

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One important aspect of this invention is to obtain a desired demodulation signal based on such comparison between the correlation values for detecting the timing point.

Specifically, as shown in Fig. 26, a pair of sampling points (to be estimated in this case as P4 and P5 or P5 and P6) are obtained to fix the timing point as either one of them, by sampling signal levels at predetermined sampling points (8 points for one symbol) for each one symbol cycle, detecting and comparing the correlations on those sampling data between each adjacent pair of P1 and P2, P2 and P3, ..., respectively, then determining the pair of sampling points to make the correlation the largest.

Fig. 1 is a block diagram showing construction in which one embodiment of a clock recovery circuit related to this invention is applied to a digital demodulator. In Fig. 1, like reference numerals denote like portions in Fig. 18, respectively.

Clock recovery circuit 40 according to this invention comprises correlation detection circuit 41 and correlation judgement circuit 42. The correlation detection circuit 41 samples respective levels of detection signals X, Y from delay detection circuit 9 at a plurality of sampling points fixed in advance for each one symbol cycle. Further, the circuit 41 detects correlation between signals sampled respectively at each adjacent pair of the sampling points as a set, adds the detected correlations in sets of the sampling points with respect to X and Y, and then supplies

the results to correlation judgement circuit 42 after accumulating them by a certain number of symbols.

Fig. 2 is a block diagram showing one example of construction of the correlation detection circuit 41. In the same drawing, delay circuits 43, 44 commonly have delay time τ which corresponds to the interval of the sampling points. Detection signals X, Y are input directly to each terminal of XOR (exclusive OR) gates 45, 46 and to the respective other terminals thereof through the delay circuits 43, 44 so as to detect the correlation to the sampling point located just before.

Thereafter, both the correlation data are added, and the result is then supplied to counter 48 after distributed at cycle τ by multiplexer 47. The counter 48 accumulates correlation data corresponding to a predetermined number of symbols.

The correlation judgement circuit 42 compares the accumulated correlation data to detect the pair of sampling point providing the largest correlation. Then, the circuit 42 judges one of the sampling points as timing point, and produces a timing clock signal based on the timing point.

As is well known, the XOR gates generally have input-output characteristics as shown in Fig. 3. Therefore, "0" is outputted when the correlation is relatively large (or the input levels are substantially identical), while "1" is outputted when small (or the input levels are not identical). Accordingly, the closer to 0 the numeral values accumulated in the counter become, the larger

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correlation the sampling point provides. Thus, the correlation judgement circuit 42 is constructed to obtain the minimum value of a plurality of input data derived from the previous stage.

Further, the detection signals X, Y outputted from delay detection circuit 9 are sent to data discrimination portions 11, 12, respectively. These data discrimination portions 11, 12 decode the detection signals X, Y based on the timing clock produced by the correlation judgement circuit 42. Thereafter, the decoded signals are demodulated into a series of data by parallel/serial converter 14.

Namely, by constructing the clock recovery circuit 40 as described above, it becomes possible to detect the distribution of correlation for each one symbol and fix a timing point based on that distribution.

In more detail, while the timing point has been estimated in the prior art based on such an instable point as zero-crossing point, the present invention can directly decide that point as a relatively stable timing point on which the eye pattern opens most widely. Therefore, such a decision of this invention is not subjected to a rapid phase shift due to fading or the like factors. It is also possible to fix a proper timing point in a short time even in case of a relatively large phase shift.

Fig. 4 is a block diagram showing construction of a second embodiment of the digital demodulator related to this invention, which demodulates a phase modulation wave

converted into an intermediate frequency (IF).

The amplitude of a phase demodulation wave is controlled by limiter circuit 50, and its phase is then quantized by phase quantization circuit 51.

Then, phase difference $\Delta\Phi$ is obtained as a quantization signal based on the difference between the phase-quantized signal and the previous signal preceding by one symbol adjusted by delay circuit 52 having a delay time of one symbol cycle.

For example, if the IF frequency is 450 kHz and the one symbol cycle (frequency) is 21 kHz, and a 12.6 MHz - pulse signal and another 168 kHz pulse signal produced from the 12.6 MHz signal by 1/75 division using divider 54 are inputted to phase quantization circuit 51 through clock 53 and divider 54 respectively, the phase modulation wave is divided into eight elements per one symbol by the pulse signal from divider 54, and each element is quantized corresponding to each phase by the pulse signal from clock 53.

In this case, the phase of each element is expressed by 0 to 27 signal pulses from the frequency ratio between IF and the pulse signal of clock 53 so that the phase difference $\Delta\Phi$ is outputted also in the form quantized by those 0 to 27 signal pulses. Thus, the relation between the phase difference $\Delta\Phi$ and the number of pulses can be expressed as shown in Fig. 5(a) in which a coordinate system is divided into 28 sections.

Namely, decoding circuit 55 determines a quadrant

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corresponding to each element inputted therein based on Fig. 5(a) by the number of pulses of the element, and decides the phase difference $\Delta\Phi$ based on Fig. 5(b) so as to decode the element into digital signals X, Y in accordance with the relation shown in Fig. 16(b). Since each of the digital signals X, Y is composed of a series of eight data per one symbol cycle, it is parallelized by serial/parallel converter 56, 57 and then latched by latch circuit 58, 59 for each one symbol cycle.

Then, each adjacent pair of bits in the outputs from the respective latch circuits 58, 59 are inputted as a set into each corresponding XOR gate to detect the correlation. Thereafter, the detected data are added in sets of the bits with respect to X and Y and then accumulated in counters by a predetermined number of symbols. Then, correlation judgement circuit 60 which received the data of counters judges the set minimizing the data or the points maximizing the correlation, and produces a timing clock signal based on those points.

Phase shifter 64 shifts the timing of latching data in latch circuits 58, 59 based on the timing clock signal so that the pair of sampling points judged by the correlation judgement circuit 60 correspond to the fourth and fifth counters.

In that way, the signals drawn out from the fifth bits of output terminals in the respective latch circuits 58, 59 become signals X, Y at the timing point, respectively. Then, they are demodulated into a series of data by

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parallel/serial converter 62.

In Fig. 4, reference numeral 63 denotes a divider for supplying one symbol cycle as the latch timing. Divider 61 further divides that symbol cycle to supply the number of count symbols for counters.

Fig. 6 shows a modified example of the embodiment shown in Fig. 4. In this case, the outputs of the fourth and fifth counters are sent to correction amount detection portion 70, and phase shifter 71 and correction delay circuit 72 shift the phase of a signal in the demodulation process based on that detection portion 70 so as to equalize the output values of both the counters.

This method of sampling such decoded digital signals in a predetermined manner and then detecting correlations between data adjacent one another is highly effective in case of obtaining a timing point or the like case. Since this method directly determines that point as a point at which the eye pattern opens most widely, it is not likely to be affected by noise near the zero-crossing point. In addition, since the timing point is renewed every time the modulation wave is demodulated by a plurality of symbols, this inventive system can rapidly follow the phase shift to be caused by fading.

Next, the bit error rate estimation means for use in the demodulator related to this invention will be described.

Fig. 7 schematically shows an eye pattern to be obtained by overlapping several times the detection signals

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in the demodulation process of the digital demodulator. In the same drawing, the signal level at point (timing point) 73 at which the eye pattern opens most widely is discriminated as the demodulation data for each symbol.

Generally, the bit error rate is evaluated by measuring it in a synchronous state or at a timing point. Fig. 9(a) shows a result of measuring the bit error rate in the event that a predetermined number of sampling points (eight points per one symbol) are fixed for each one symbol cycle as shown in Fig. 8, and demodulation is performed for each sampling point. In Fig. 9(a), the horizontal axis shows the ratio between density No of noise power spectrum and signal energy Eb per one bit, and the vertical axis shows the logarithm of the bit error rate.

In the same drawing, reference numeral 90 is a curve obtained at timing point P5, 91 at P4 or P6, and 92 at P3 or P7. It should be understood that the bit error rate will rise with the sampling point getting away from the timing point, while fall with decrease of noise (or increase of E_b/N_o).

If the difference of bit error rate ΔBER at each of three points α, β and γ is measured with respect to curves 90 and 91 in Fig. 9(a), the relation of $\Delta BER_\alpha > \Delta BER_\beta > \Delta BER_\gamma$ will be obtained. Though there can not be seen definite difference between these ΔBERs in the drawing, there is, in fact, a relatively large difference between these error rate values because they are expressed

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respectively as logarithms in the same drawing.

As is also apparently seen from Fig. 9(b) showing the relation between each sampling point and the bit error rate with respect to ΔBER_α, ΔBER_β and ΔBER_γ correspond well to the bit error rates BER_α, BER_β and BER_γ at the timing point, respectively. Therefore, by measuring ΔBERs, it becomes possible to obtain the bit error rate at the timing point.

On the other hand, in case of the timing point 73 shown in Fig. 7 at which the eye pattern opens most widely, the level of detection signal becomes a or -a where it converges at a relatively high density, and is kept at substantially the same level near that point 73. However, the probability of discordance in the level of detection signals becomes high in the area far from the timing point 73 and near the zero-crossing point 74.

When the correlation between each adjacent pair of the sampling points as fixed in Fig. 8 is examined, there can be obtained a curve as shown in Fig. 10 very similar to the curve of Fig. 9(b), showing the fact that the correlation value becomes large near the timing point 73 (P5) where the signal level is kept substantially the same, while becomes small when the signal levels of two sampling points are distinctly different.

Accordingly, considering the fact that both the correlation and the bit error rate show a similar distribution to the sampling points, the present invention

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is constructed to fix the predetermined number of sampling points for a certain signal in the demodulation process and estimate the bit error rate at the timing point by detecting the correlation.

Specifically, the signal levels at the sampling points as fixed in Fig. 7 are sampled, and the correlation of the sampled data between each adjacent pair of sampling points P1 and P2, P2 and P3, ·····, are detected successively, then the pair of sampling points which maximize the correlation and another pair adjacent that pair showing the larger correlation (P4 and P5, and P5 and P6 in Fig. 8) are determined. Further, synchronization is performed to make those pairs of sampling points take the same value. Then, the sampling point (P5 in the same drawing) belonging to both the pairs is fixed as the timing point.

Since the correlation value of such a pair of sampling points in a synchronized state corresponds to the aforementioned ΔBER, the bit error rate can be estimated using the correlation value by a calculation based on statistic values giving the relation between correlation values and ΔBERs obtained in advance by measurement and the relation between ΔBERs and the bit error rate at the timing point.

Figs. 11 and 12 respectively show construction in which the bit error rate estimation means related to this invention is applied to a digital demodulator. In the same drawings, like parts in Figs. 1 and 2 are designated by

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like reference numerals, respectively.

In the construction shown in Figs. 11 and 12, counter 4 of correlation detection circuit 41 outputs data to bit error estimation circuit 95. Namely, when synchronized as shown in Fig. 10, sampling point P5 becomes the timing point, and the output of counter 4 expresses the correlation between sampling points P4 and P5. Since the output data corresponds to the aforementioned ΔBER, the bit error rate at the timing point can be estimated by the bit error rate estimation means 95 through a predetermined calculation on that correlation value from the counter 4. Thus, based on that estimated bit error rate, the control system of the demodulator selects a radio wave the most suitable to the current circuit condition from a plurality of base stations.

In this case, as the bit error rate device 95, any means may be used if it can perform conversion based on statistic values for giving relations between a correlation value measured in advance and ΔBER and between ΔBER and the timing point. That is, a logic circuit may be constructed based on the aforementioned statistic values, or numerical operations by a microcomputer or the like means may be used.

Fig. 13 is a graph showing results obtained from a simulation of bit error rate measurement. Marks expressed by circles (○) respectively show measurement results from a conventional method comprising adding a predetermined noise to a series of modulated data and then dividing the

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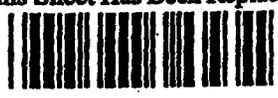
number of bit errors when demodulated by the demodulation circuit by the number of all the bits. The other marks expressed by blackened circles (●) respectively show the results obtained by using the bit error rate estimation means according to this invention under the same condition. As is clearly seen from the same drawing, the estimation is fully reliable in practical use because both the above results are substantially the same.

Next, the AFC circuit for use in the demodulator related to this invention will be described.

As described above, this circuit corrects frequency drift in a modulation wave based on comparison between an estimation value from the bit error rate estimation means and a value measured by a known bit error rate measuring device for measuring a bit error rate based on a series of data specifically used for the bit error rate measurement inserted in the modulation wave at a predetermined interval. Fig. 14 shows construction in which one embodiment of the AFC circuit related to this invention is applied to the digital demodulator. In the same drawing, like reference parts in Fig. 21 are designated by like reference numerals, respectively.

Phase quantization circuit 22 divides a signal into eight elements per one symbol and quantizes each element corresponding to each phase. Using delay detection circuit 8 having a delay time corresponding to one symbol cycle, phase difference for each element is obtained by detecting difference from the signal preceding by one symbol.

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Decoding circuit 9 produces decoded digital signals X, Y respectively based on the phase difference of each element.

Based on the decoded signals, the bit error rate estimation means 95 estimates a bit error rate and produces a timing clock signal to decide data of X, Y.

Fig. 15 shows a circuit construction on the periphery of bit error rate estimation means 95. Similar to the aforementioned case, sampling point P5 of the bit error rate estimation means is designated as the timing point, and the output of counter 4 expresses the correlation between sampling points P4 and P5 and corresponds to $\Delta\bar{BER}$. Thus, the estimation means 95 can estimate the bit error rate at the timing point through a predetermined numerical operation on the correlation value from counter 4.

Also in this case, as the estimation means 95, any means may be used if it can perform conversion based on statistic values for giving relations between a correlation value measured in advance and ΔBER and between ΔBER and the timing point. That is, a logic circuit may be constructed based on the aforementioned statistic values, or numerical operations by a microcomputer or the like means may be used.

On the other hand, bit error rate estimation means 97 stores a series of data decided in advance for measuring bit error rates and measures bit error rates by extracting the aforementioned series of data for measuring bit error rates inserted in a modulation wave at a predetermined interval using a demodulated signal and comparing them with

the stored series of data.

Accordingly, the AFC circuit of this invention is constructed to compare a bit error rate estimation value with a measured value and supply to VCXO 30 the voltage necessary for minimizing both the values adding it to the output of conventional AFC circuit 27. Therefore, it becomes possible to detect and correct frequency drift not only on receiving the preamble signal but also for a period until the next preamble signal will reach.

Although this invention has been described only on the application to a digital demodulator of the type of performing base band delay detection to a phase modulation wave, it is not limited to such a type. Namely, it is possible to use any type of digital demodulator if it can be used in the system for modulating and demodulating digital signals. For example, this invention can also be applied to demodulator of the type of frequency modulation or of amplitude modulation.

In addition, the process from the modulation wave to decoding may be constructed by any known system. For example, in a synchronous detection type demodulator, this invention can be applied to complement the phase difference between the preamble signal and the next preamble signal.

In the above embodiments, an XOR gate has been used for detecting correlations. However, it is also possible to construct such means with an NXOR gate or the like circuit if it can discriminate the case in which the two input values are the same from the case in which they are

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different.

Also in the above embodiments, the timing point has been decided by detecting correlations of detected and decoded digital signals (X, Y). However, for example, in case of changing the system of Fig. 1 into the construction for performing A/D conversion to the signal having passed through LPF 5, 6 after delay detection, it also becomes possible to detect correlations of signals not digitized but subjected to delay detection. In that case, since the magnitude of correlations corresponds to that of results from the multiplication between sampling data for the respective sampling points, a multiplier may be used as the correlation detection means. Accordingly, it should be understood that it is also possible to detect correlations of base band signals (I, Q, $\Delta\Phi$) or the digitized signals thereof (multivalued digital signals) in the synchronous detection method.

Furthermore, the above embodiments have been constructed to estimate the bit error rate based on the correlation value of the two sampling points in the vicinity of the timing point with the number of sampling points fixed at eight per one symbol. It is also possible to increase or decrease the number of sampling points considering the precision or the like factors. In addition, it is also possible to estimate the bit error rate based on the distribution of correlation values of sampling points other than those at or near the timing point.

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As stated above, since the present invention makes it possible to detect the timing point in the demodulation process in a short time with the timing point corresponding to the point at which the eye pattern opens most widely, the occurrence of bit errors can be minimized against the phase shift due to noises or fading near the zero-crossing point.

Since the insertion of a specific signal in the modulation data becomes unnecessary, the bit error rate can be estimated without degrading the communication efficiency and any affection to the demodulation.

Additionally, it also becomes possible to make corrections at high speed and with high precision even in case of occurrence of relatively large frequency drift.

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CLAIMS:

1. A digital demodulator for demodulating a detection signal obtained by detecting a modulation wave using predetermined detection means based on a timing clock signal, comprising:

correlation detection means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of the sampling points;

correlation judgement means for comparing the correlations detected by the correlation detection means, judging the pair of sampling points which maximize the correlation and another pair of sampling points providing the next largest correlation, and producing a timing clock signal based on the judgement; and

phase shift means for shifting the phase of the signal in the demodulation process so as to equalize the correlations of the two pairs of sampling points.

2. A digital demodulator for demodulating a detection signal obtained by detecting a modulation wave using predetermined detection means based on a timing clock signal, comprising:

correlation detection means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of

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the sampling points;

correlation judgement means for comparing the correlations detected by the correlation detection means, judging the pair of sampling points which maximize the correlation and one of the two pairs of sampling points adjacent that correlation maximizing pair and providing the next largest correlation, and producing a timing clock signal at the sampling point belonging to both the pairs of sampling points; and

phase shift means for shifting the phase of the signal in the demodulation process so as to equalize the correlations of the two pairs of sampling points.

3. A digital demodulator according to claim 1 or 2, wherein the signal in the demodulation process is a detection signal obtained by detecting a modulation wave using predetermined detection means, and the sampling cycle of the correlation detection means is shifted to produce the timing clock signal correspond to predetermined one of the sampling points, thereby obtaining a demodulation signal from data sampled at the one of sampling points.

4. A digital demodulator according to claim 1 or 2, wherein the signal in the demodulation process is a base band signal, and the sampling cycle of the correlation detection means is shifted to produce the timing clock signal correspond to predetermined one of the sampling points, thereby obtaining a demodulation signal by detecting data sampled at the one of sampling points.

5. A digital demodulator for demodulating a

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detection signal obtained by detecting a modulation wave using predetermined detection means into a digital signal based on a timing clock signal produced by a clock recovery circuit, wherein the clock recovery circuit comprises:

correlation detection means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of the sampling points; and

correlation judgement means for comparing the correlations detected by the correlation detection means and judging the pair of sampling points which maximize the correlation; whereby:

the correlation judgement means can produce a timing clock signal based on the judgement.

6. A digital demodulator for obtaining a digital signal by detecting a modulation wave using predetermined detection means, comprising:

correlation detection means for sampling a detection signal output from detection means at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of the sampling points;

correlation judgement means for comparing the correlations detected by the correlation detection means and judging the pair of sampling points which maximize the correlation; and

shift means for shifting the sampling cycle of the

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correlation detection means so that the sampling data of either one of the pair of sampling points providing the maximum correlation is output at one of the sampling points fixed in advance based on the output of the correlation judgement means, whereby the detection signal can be output as a demodulation signal at the one of sampling points.

7. A digital demodulator for obtaining a digital signal by detecting a modulation wave using predetermined detection means, comprising:

correlation detection means for sampling a base band signal at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of the sampling points;

correlation judgement means for comparing the correlations detected by the correlation detection means and judging the pair of sampling points which maximize the correlation; and

shift means for shifting the sampling cycle of the correlation detection means so that the sampling data of either one of the pair of sampling points providing the maximum correlation is output at one of the sampling points fixed in advance based on the output of the correlation judgement means, whereby a demodulation signal can be obtained by detecting the base band signal output at the one of sampling points.

8. A digital demodulator according to claims 5 to 7, further comprising correlation accumulation means for

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accumulating the respective outputs from the correlation detection means for a plurality of symbol cycles, whereby the correlation judgement means can detect the pair of sampling points providing the maximum correlation data of those accumulated in the correlation accumulation means.

9. An AFC circuit used for a digital demodulator for detecting a modulation wave using predetermined detection means and demodulating the modulation wave, comprising:

a bit error rate estimation means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle), detecting correlations between each adjacent pair of the sampling points, and estimating a bit error rate based on the distribution of the detected correlations; and a bit error rate measuring device for measuring a bit error rate based on a series of data inserted in the modulation wave at a predetermined interval for measuring the bit error rate, whereby the frequency drift can be corrected by comparing both the bit error rates.

10. An AFC circuit according to claim 9, wherein the bit error rate estimation means samples a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle), detects correlations between each adjacent pair of the sampling points, and estimates the bit error rate based on the difference of at least two of the correlations.

11. A bit error rate estimation means used for a

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digital demodulator for detecting a modulation wave using predetermined detection means and demodulating the modulation wave, wherein:

the bit error rate estimation means samples a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle), detects correlations between each adjacent pair of the sampling points, and estimates a bit error rate based on the distribution of the detected correlations.

12. A bit error rate estimation means used for a digital demodulator for detecting a modulation wave using predetermined detection means and demodulating the modulation wave, wherein:

the bit error rate estimation means samples a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle), detects correlations between each adjacent pair of the sampling points, and estimates a bit error rate based on the difference of at least two of the correlations.

13. A clock recovery circuit used for a digital demodulator for detecting a modulation wave using predetermined detection means, comprising:

correlation detection means for sampling a signal in the demodulation process at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and detecting correlations between each adjacent pair of the sampling points; and

correlation judgement means for comparing the

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correlations detected by the correlation detection means and judging the pair of sampling points which maximize the correlation, whereby:

the correlation judgement means can produce a timing clock signal based on the judgement.

14. A clock recovery circuit used for a digital demodulator for sampling a detection signal obtained by detecting a modulation wave using predetermined detection means at a plurality of sampling points fixed in advance for each unit data cycle (symbol cycle) and shifting the sampling cycle to produce the timing clock signal correspond to predetermined one of the sampling points, thereby to produce a demodulation signal from the data sampled at the predetermined one of sampling points, comprising:

correlation detection means for detecting correlations between the sampling data of each adjacent pair of the sampling points; and

correlation judgement means for comparing the correlations detected by the correlation detection means and judging the pair of sampling points which maximize the correlation, whereby:

a timing clock signal can be produced at the sampling point providing the maximum correlation based on the judgement of the correlation judgement means.

15. A clock recovery circuit used for a digital demodulator for sampling a base band signal at a plurality of sampling points fixed in advance for each unit data

cycle (symbol cycle) and shifting the sampling cycle to produce a timing clock signal correspond to predetermined one of the sampling points, thereby to produce a demodulation signal by detecting the data sampled at the predetermined one of sampling points, comprising:

correlation detection means for detecting correlations between the sampling data of each adjacent pair of the sampling points; and

correlation judgement means for comparing the correlations detected by the correlation detection means and judging the pair of sampling points which maximize the correlation, whereby: a timing clock signal can be produced at the sampling point providing the maximum correlation based on the judgement of the correlation judgement means.

16. A clock recovery circuit according to claims 13 to 15, further comprising correlation accumulation means for accumulating correlation data for a plurality of symbol cycles to the respective outputs from the correlation detection means, whereby the correlation judgement means can detect the pair of sampling points providing the maximum correlation data of those accumulated in the correlation accumulation means.

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