

The invention is based on a circuit arrangement for automatically adjusting the quiescent current in a transformerless transistorised push pull output stage at whose output a load impedance is connected to a datum potential and including at least one sensing element for measuring the quiescent current flowing in the push pull output stage wherein there is provided in each branch of the push pull output stage a respective sensing element from each of which a voltage measured against the datum potential can be tapped off, which voltages are each connected to a respective input of a differential amplifier stage whose output is connected to the one input of a comparator circuit whose other input is at a reference potential, and that the output of the comparator circuit controls an electronic switch in a manner such that it charges an electrical store whose charging voltage regulates the quiescent current of the push pull output stage via a regulating transistor in such a way that the voltage value which is proportional to the quiescent current and which is measured by the sensing elements is equal to the reference potential. A circuit of this type is known from the DE-A 36 32 076. See also the quiescent current regulation in accordance with the US-A-4 207 475.

The circuit arrangement described in the first patent application has an automatic quiescent current regulation that is still partially frequency dependent.

The object of the invention is to remove this frequency dependence. This object is achieved by the invention defined in claim 1. Further advantageous embodiments of the invention are specified in the appendant claims.

The invention will be described hereinafter with the help of the drawing.

Figure 1 shows a circuit arrangement relating to the invention

Figure 2 shows voltage diagrams for explaining the effect of the invention.

To start with, the circuit described in DE-A 36 32 076, upon which the invention is based, will be discussed once more whereby however, only the essential parts of the Figure were adopted. The circuit arrangement is concerned with the construction of a known push pull output stage including the complementary output transistors 1 and 2 which have their emitters interconnected and whose collectors are respectively connected to the operating voltage potentials $+UB_1$ and $-UB_1$. The

load impedance 3, e.g. in the form of a loudspeaker, is connected to the output of the push pull output stage. The other end of the load impedance is connected to a datum potential e.g. earth. For the purpose of adjusting the quiescent current flowing in the push pull output stage, there serves a transistor 6 which is connected between the bases of the output transistors 1 and 2. The input signal UE, which controls the push pull output stage 1, 2 via the pre-amplifier 8 and the driver transistor 9, is supplied via the terminal 7. Voltages measured against the datum potential can be tapped off from the resistors 4 and 5. The voltage tapped off from the resistor 4, which is produced by the quiescent current and the load current flowing through the load impedance 3 that is superimposed thereon, is supplied to the non-inverting input of a differential amplifier stage 10 and the voltage tapped off from the resistor 5 is supplied to the inverting input of the differential amplifier stage 10. A signal occurs at the output of the differential amplifier stage 10 as is marked in the Figure. It is composed of the value UR, which corresponds to the quiescent current and of the value US which corresponds to the signal current.

Due to the supply of the negative signal portion to the inverting input of the differential amplifier stage 10, this appears phase rotated by 180° at the output. Since the supply voltage UB2 for the differential amplifier stage 10 is usually smaller than the supply voltage UB1 for the push pull output stage, the signal voltage supplied to the differential amplifier stage 10 has to be reduced by a division factor which corresponds to the ratio of the resistance values of the resistors ($R_{11} + R_{12}$). The differential amplifier stage 10 has an amplification factor $V = R_{12}/R_{11}$. The output voltage is led to the one input of a comparator circuit 13 to whose other input reference potential U_{ref} is applied which is formed with the help of the voltage divider consisting of the resistors 14 and 15 connected to the operating voltage source UB2. If the voltage value applied to the plus input of the comparator 13 falls below the reference potential U_{ref} applied to the minus input, then the output of the comparator 13 goes to the datum potential. The comparator 13 has an open collector output which adopts either the datum potential or the operating voltage UB2. When the output falls to the datum potential, an electronic switch in the form of a transistor 16 becomes conductive so that the operating voltage UB2 charges an electrical store in the form of a capacitor 18 via the resistor 17. The store influences the transistor 6 via a regulating transistor 19 in such a way that the quiescent current rises until such time as the voltage value supplied to the plus input of the comparator 13 corresponds to the reference potential U_{ref} . The reference potential U_{ref} is

set in such a way that it corresponds to the voltage drop across the resistors 4 and 5 which is proportional to the desired quiescent current through the push pull output stage. When this voltage value is reached, the transistor 16 is blocked by the potential occurring at the output of the comparator 13. Due to the circuit, a charging of the capacitor 18 only occurs during the zero crossings of the input signal UE at times when the actual quiescent current is flowing.

There are output transistors which, when modulated by signals of higher frequency and when subjected to large load currents, conduct a shunt current through the output stage if their cut-off frequency is too low. They are then too sluggish for the crossover-like switching so that these additional shunt currents can flow. The circuit for the automatic regulation of the quiescent current described hereinabove interprets these shunt currents as quiescent current so that they try to change these until the total current again corresponds to the prescribed reference value. Thereby however, the quiescent current required is too small so that transfer distortions can occur for high frequencies and large load currents. In order to avoid this event, one could select the quiescent current to be basically larger by the factor of 3 - 4 and would thereby achieve a safety margin from the transfer distortions. However, this would considerably increase the quiescent dissipation. That also means a greater heat loss which, in its turn, would have to be dissipated by larger heat sinks.

For the elimination of the frequency dependent quiescent current regulation which delivers too small a quiescent current above about 8 kHz, a phase rotating member is connected to one, e.g. the non-inverting input of the differential amplifier 10. In the Figure, this is for example a capacitor 20 connected between the input and the datum potential. The resistor 11 having a magnitude of e.g. 20 kOhm and the capacitor 20 having a magnitude of e.g. 10 pF displace the phase of the input signal by ca one degree. Due to this tiny phase displacement, the common mode rejection at high frequencies is deliberately degraded. Without the phase rotating member, there occurs at the output of the differential amplifier 10 the voltage in accordance with Figure 2a. The quiescent current is automatically adjusted such that the negative peaks of the voltage correspond to the reference value of the comparator 13. Due to the poor common mode rejection as a result of the deliberately introduced phase displacement of the one input signal to the differential amplifier 10, there results the curve in accordance with Figure 2b. One can see that this curve lies partly below the zero axis. The automatic quiescent current

regulation endeavours, contingent upon the circuit, to always adjust itself to the reference value. However, the circuit temporarily sees a voltage value which is too low and correspondingly increases the quantity of charge for the capacitor 18. Instead of a capacitor, an inductance having a magnitude of ca 1 mH can also be placed in series with the resistor 11 in the input lead of the differential amplifier 10 with a similar effect.



Claims

1. Circuit arrangement for automatically adjusting the quiescent current in a transformerless transistorised push pull output stage (1, 2) at whose output a load impedance (3) is connected to a datum potential and including at least one sensing element (4, 5) for measuring the quiescent current flowing in the push pull output stage wherein there is provided in each branch of the push pull output stage a respective sensing element (4, 5) from each of which a voltage measured against the datum potential can be tapped off, which voltages are each connected to a respective input of a differential amplifier stage (10) whose output is connected to the one input of a comparator circuit (13) whose other input is at a reference potential, and that the output of the comparator circuit (13) controls an electronic switch (16) in a manner such that it charges an electrical store (18) whose charging voltage regulates the quiescent current of the push pull output stage (1, 2) via a regulating transistor (19) in such a way that the voltage value which is proportional to the quiescent current and which is measured by the sensing elements (4, 5) is equal to the reference potential, characterised in that, a phase rotating element (20) is connected to one of the two inputs of the differential amplifier (10) whereby the output voltage of the differential amplifier stage (10) is reduced at higher frequencies and the quiescent current is boosted for the compensation of the shunt currents flowing in the output stage transistors (1, 2).
2. Circuit arrangement in accordance with Claim 1, characterised in that, a capacitor (20) is connected to the datum potential at the inverting or non-inverting input of the differential amplifier (10).
3. Circuit arrangement in accordance with Claim 2, characterised in that, the capacitor is in the order of magnitude of 10 pF.
4. Circuit arrangement in accordance with Claim 1, characterised in that, an inductance is connected in the lead to the inverting or non-inverting input of the differential amplifier (10).
5. Circuit arrangement in accordance with Claim 4, characterised in that, the value of the inductance has a magnitude of 1 mH.