(12) INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(19) World Intellectual Property Organization
International Bureau

(43) International Publication Date
20 September 2007 (20.09.2007)

PCT

(10) International Publication Number
WO 2007/104799 A1

(51) International Patent Classification:
H01L 21/48 (2006.01)

(21) International Application Number:
PCT/EP2007/052497

(22) International Filing Date: 16 March 2007 (16.03.2007)

(25) Filing Language: English

(26) Publication Language: English

(30) Priority Data:
MI2006A000478 16 March 2006 (16.03.2006) IT

(71) Applicants *(for all designated States except US)*: **ELES SEMICONDUCTOR EQUIPMENT S.P.A.** [IT/IT]; Fraz. Pian di Porto, Zona Ind. le Bodoglie, 148/1/Z, I-06059 Todi (IT). **RISE tECHNOLOGY S.R.L.** [IT/IT]; Via Orazio, 8/b, I-00040 Pomezia (IT).

(72) Inventor; and

(75) Inventor/Applicant *(for US only)*: **BALUCANI, Marco** [IT/IT]; Univeristà di Roma La Sapienza, Dip. Elettronica, Via Eudossiana, 18, I-00184 Roma (IT).

(74) Agents: **PEZZOLI, Ennio** et al.; Via Settembrini, 40, I-20124 Milano (IT).

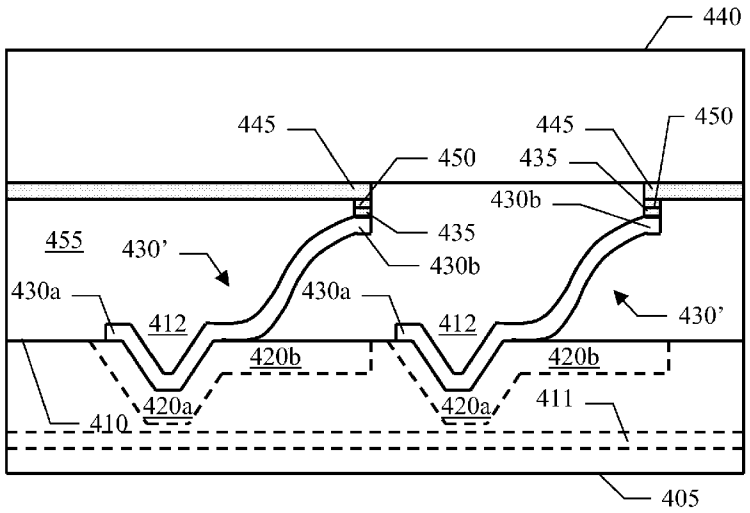
(81) Designated States *(unless otherwise indicated, for every kind of national protection available)*: AE, AG, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BW, BY, BZ, CA, CH, CN, CO, CR, CU, CZ, DE, DK, DM, DZ, EC, EE, EG, ES, FI, GB, GD, GE, GH, GM, GT, HN, HR, HU, ID, IL, IN, IS, JP, KE, KG, KM, KN, KP, KR, KZ, LA, LC, LK, LR, LS, LT, LU, LY, MA, MD, MG, MK, MN, MW, MX, MY, MZ, NA, NG, NI, NO, NZ, OM, PG, PH, PL, PT, RO, RS, RU, SC, SD, SE, SG, SK, SL, SM, SV, SY, TJ, TM, TN, TR, TT, TZ, UA, UG, US, UZ, VC, VN, ZA, ZM, ZW.

(84) Designated States *(unless otherwise indicated, for every kind of regional protection available)*: ARIPO (BW, GH, GM, KE, LS, MW, MZ, NA, SD, SL, SZ, TZ, UG, ZM, ZW), Eurasian (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European (AT, BE, BG, CH, CY, CZ, DE, DK, EE, ES, FI, FR, GB, GR, HU, IE, IS, IT, LT, LU, LV, MC, MT, NL, PL, PT, RO, SE, SI, SK, TR), OAPI (BF, BJ, CF, CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD, TG).

Published:
— *with international search report*
— *before the expiration of the time limit for amending the claims and to be republished in the event of receipt of amendments*

[Continued on next page]

(54) **Title:** INTERCONNECTION OF ELECTRONIC DEVICES WITH RAISED LEADS



(57) **Abstract:** A process of manufacturing an interconnection element (160; 160') for contacting electronic devices is proposed. The process starts with the step of forming a plurality of leads (130) on a main surface (110) of a first substrate (105); each lead has a first end (130a) and a second end (130b). The second end of each lead is coupled with a second substrate (140). The second substrate and the first substrate are then spaced apart, so as to extend the leads (130') between the first substrate and the second substrate. The process also includes the step of treating the main surface before forming the leads to control an adhesion of the leads on the main surface.

WO 2007/104799 A1

For two-letter codes and other abbreviations, refer to the "Guidance Notes on Codes and Abbreviations" appearing at the beginning of each regular issue of the PCT Gazette.