

Description

The present invention relates to a reactance control circuit, and more particularly to a reactance control circuit for use in a variable frequency oscillator.

An example of a typical conventional variable frequency oscillator is known from US-A-4 745 375 and shown in Fig. 1, and comprises a differential amplifier 2, a DC amplifier 3, a variable reactance circuit 4, and an oscillator 5. The oscillating frequency generated by the oscillator 5 is determined by an oscillating frequency of the oscillator 5 and the value of reactance of the reactance circuit 4. The reactance circuit 4 is made up of a capacitor C1, a resistor R5, and differential amplifiers 6 and 7, respectively coupled with the oscillator 5 in a negative feedback and a positive feedback fashion. Since the negative feedback loop has the effect of decreasing the output of the oscillator 5, and the positive feedback loop increases the same, the reactance value of the variable reactance circuit 4 can be varied in accordance with the ratio (I_3/I_4) of the value of a current I_3 flowing through the differential transistor circuit 6 and that of a current I_4 flowing through the differential transistor circuit 7. When the current I_3 is greater than the current I_4 , the output of the oscillator 5 is decreased by the negative feedback loop of the differential transistor circuit 6, with the result that the reactance value C of the variable reactance circuit 4 increases. When on the other hand, the current I_3 is less than the current I_4 , the output of the oscillator 5 is increased by the positive feedback loop of the differential transistor circuit 7, and thus the reactance value C of circuit 4 decreases.

The current ratio I_3/I_4 is determined by the differential amplifier 2 and the DC amplifier 3. In the differential amplifier 2, currents I_1 and I_2 are determined by the difference in the level of an input voltage V_{in} and a reference voltage V_{ref1} , amplified by the DC amplifier 3, and supplied in the form of currents I_3 and I_4 to the differential transistor circuits 6 and 7.

When there is zero difference in the level of the input voltage V_{in} and the reference voltage V_{ref1} , the currents I_3 and I_4 are then equal, in which case the negative feedback operation by the differential transistor circuit 6 and the positive feedback operation by the differential transistor circuit 7 cancel each other out. Therefore, the reactance value of the variable reactance circuit 4 is determined solely by capacitor C1 and the oscillator 5, independent upon the currents I_3 and I_4 , and the reactance value is equal to a reference reactance C_{ref} . When the reactance value is equal to the reference reactance C_{ref} , the variable frequency oscillator generates an output signal V_{out} of a free running frequency F_{ref} .

The DC amplifier 3 of the variable frequency oscillator shown in Fig. 1 uses NPN transistors Q1 and Q2. However, the geometrics and operating characteristics of such transistors are frequently nonuni-

form, this being attributable to the process used to manufacture them. Thus, when there is zero difference in the level of the input voltage V_{in} and the reference voltage V_{ref1} , and hence the current I_1 is equal to the current I_2 , the reactance value C of the reactance circuit 4 may not be equal to the reference reactance C_{ref} , for the reason that, even if the currents I_1 and I_2 applied to the bases of the transistors Q1 and Q2 are equal to each other, the currents I_3 and I_4 passing through the transistors Q1 and Q2 may not be equal if the operating characteristics and geometrics of these transistors differ from each other. Consequently, if the reactance value C of the variable reactance circuit 4 is not equal to the reference reactance value C_{ref} , the free running frequency F_{ref} of the variable frequency oscillator will differ from its designed value.

Accordingly, an object of the present invention is to provide a reactance control circuit which provides a desired reference reactance value C_{ref} even if the transistors of the DC amplifier thereof have different geometrics and operating characteristics.

To achieve the above object, there is provided a reactance control circuit comprising: a variable reactance circuit having first and second differential transistor circuits, the reactance of the variable reactance circuit being determined by the currents flowing to the first and second differential transistors; a differential amplifier for producing first and second currents in accordance with an input voltage; and a DC amplifier circuit for amplifying the first and second currents derived from the differential amplifier, and for supplying the amplified currents to the variable reactance circuit in order to control the currents flowing to the first and second differential transistor circuits. The DC amplifier circuit includes first and second input terminals for receiving first and second currents output from the differential amplifier circuit, first and second output terminals for supplying third and fourth currents to the variable reactance circuit, a first transistor, having a collector coupled with the first output terminal, an emitter coupled with a predetermined potential supplying terminal, and a base, a second transistor, having a collector coupled with the second output terminal, an emitter coupled with the predetermined potential supplying terminal, and a base, and base potential control means. When the first and second currents differ from each other, the base potential control means supplies different potentials to the bases of the first and second transistors so that third and fourth currents corresponding to the first and second currents flow through the first and second transistors, respectively. When the first and second currents are equal to each other, the base potential control means supplies a predetermined low potential to the bases of the first and second transistors, so that the third and fourth currents flowing to the first and second transistors are both reduced.

Therefore, even if the first and the second transistors differ in their geometrics and operating characteristics, any difference in the third and fourth currents will be very small. As a result, the reference reactance of the variable reactance circuit of the present invention is unaffected by differences in geometrics and operating characteristics of the first and the second transistors; thus, in this invention, the desired reference reactance can be assured.

This invention can be more fully understood from the following detailed description when taken in conjunction with the accompanying drawings, in which:

Fig. 1 is a circuit diagram showing a variable frequency oscillator using a conventional reactance control circuit;

Fig. 2 is a circuit diagram showing a variable frequency oscillator using a reactance control circuit which is a first embodiment of the present invention;

Fig. 3 is a graph showing an operating characteristic of the reactance control circuit of Fig. 2; and

Fig. 4 is a circuit diagram showing a variable frequency oscillator using a reactance control circuit which is a second embodiment of the present invention.

A variable frequency oscillator using a reactance control circuit which is a first embodiment of the present invention will now be described with reference to Fig. 2.

The variable frequency oscillator according to this embodiment comprises a differential amplifier 12, a variable reactance circuit 14, an oscillating circuit 16, and a DC amplifier 20.

The differential amplifier 12 is made up of a resistor R8, PNP transistors Q11 and Q12, and a low-pass filter (LPF) 11. An input voltage V_{in} is smoothed by low-pass filter 11 and is supplied to the base of the PNP transistor Q11. The base of the PNP transistor Q12, on the other hand, is coupled for reception of a reference voltage V_{ref1} . The value of a difference in the level of the input voltage V_{in} and the reference voltage V_{ref1} determines the levels of currents I1 and I2 produced by the differential amplifier 12. For example, when there is zero difference in these voltages, the currents I1 and I2 are equal.

The oscillating circuit 16 is made up of an oscillator 161 and a ceramic resonator 162, and its oscillating frequency is determined by the resonance frequency of the ceramic resonator 162 and the reactance value of the variable reactance circuit 14.

The variable reactance circuit 14 is made up of a capacitor C1, resistors R3 to R5, a first differential transistor circuit 141 including NPN transistor Q5 and Q6, a second differential transistor circuit 142 including NPN transistors Q7 and Q8, and a current mirror circuit 143 including PNP transistors Q9 and Q10 and resistors R6 and R7. An emitter common to the NPN transistors Q5 and Q6 in the first differential transis-

tor circuit 141, is connected to a current output terminal C of the DC amplifier 20, by way of the resistor R3, and an emitter common to the transistors Q7 and Q8 in the differential transistor circuit 142 is connected, by way of the resistor R4, to a current output terminal D of the DC amplifier 20. The current mirror circuit 143 serves as a load circuit of the first and second differential transistor circuits 141 and 142 and is connected to these circuits.

The bases of the transistors Q6 and Q7 receive a reference voltage V_{ref2} , and the bases of the transistors Q5 and Q8 are coupled for reception of a potential at the series connecting node of the capacitor C1 and the resistor R5. The differential transistor circuits 141 and 142 are coupled with the oscillator 16 in a negative feedback and a positive feedback fashion, respectively. The negative feedback loop decreases the output of the oscillator 16, whereas the positive feedback loop increases the same.

In the circuit arranged thus, the reactance of the variable reactance circuit 14 is varied in accordance with the ratio (I3/I4) of a current I3 flowing through the differential transistor circuit 141 and a current I4 flowing through the differential transistor circuit 142. More specifically, when $I3 > I4$, the negative feedback loop decreases the output of the oscillator 16, with the result that the reactance C of the variable reactance circuit 14 is high. Conversely, when $I3 < I4$, the positive feedback loop increases the output of the oscillator 16, and thus the reactance C is low.

For simplicity, let us suppose two extreme cases. In the first case, the DC amplifier 20 generates the current I3 but not the current I4. In contrast, in the second case, the DC amplifier 20 generates the current I4 but not the current I3. In the first case, the reactance C of the variable reactance circuit 14, when viewed from the ceramic resonator 162, is expressed as

$$C = (1 + g_m R_5) C_1 \quad (1)$$

In the second case, the reactance C of the variable reactance circuit 14 is expressed as

$$C = (1 - g_m R_5) C_1 \quad (2)$$

In the above equations, g_m denotes the mutual conductance of each of the transistors Q5 to Q8.

It is apparent from the above explanation that the reactance C of the variable reactance circuit 14 (parallel capacitance of the ceramic resonator 162) is controlled by the ratio (I3/I4) of the currents I3 and I4, and determines the oscillating frequency of the oscillating circuit 16.

The DC amplifier 20 functions to amplify the output currents I1 and I2 of the differential amplifier 12, and to feed the amplified currents as the currents I3 and I4 to the variable reactance circuit 14. The DC amplifier 20 is made up of NPN transistors Q1 and Q2 for producing the currents I3 and I4, and a control circuit 21 for providing base potentials for transistors Q1 and Q2. The control circuit 21 is made up of NPN tran-

sistors Q3 and Q4, and resistors R1, R2, R11, and R12.

The transistor Q1 is connected at the collector to the current output terminal C for outputting the current I3, and at the emitter to a ground terminal. The transistor Q2 is connected at the collector to the current output terminal D for outputting the current I4, and at the emitter to a ground terminal. The transistors Q1 and Q2 as designed to have the same geometrics, the base of the transistor Q1 being connected to the collector of the transistor Q3, whose emitter is connected to a ground terminal, and the base of the transistor Q2 being connected to the collector of the transistor Q4, whose emitter is also connected to a ground terminal. The bases of the transistors Q3 and Q4 are interconnected. The resistor R11 is located between the input node A for receiving the current I1 from the differential amplifier 12 and the collector of the transistor Q3, and the resistor R12 is located between the input node B for receiving the current I2 from the amplifier 12 and the collector of the transistor Q4. The resistors R1 and R2 are located between the input nodes A and B, respectively, and the base common to the transistors Q3 and Q4. The resistors R1 and R2 are equal in resistance, as are resistors R3 and R4.

When $I_1 = I_2$ in the DC amplifier 20, the potential at a connection point (node A) of the resistors R1 and R11 is substantially equal to that at a connection point (node B) of the resistors R2 and R11. As a result, only a small amount of current flows between the nodes A and B through the resistors R1 and R2, and thus the current I1 flows into the resistor R11, while the current I2 flows into the resistor R12. Assuming that the resistance value of each of the resistors R11 and R12 is R, and the current value of each of the currents I1 and I2 is I, then the base potential of each transistor (Q1 or Q2) is smaller, by RI, than the potential at the corresponding node (A or B). Since the current flowing between the nodes A and B through the resistors R1 and R2 is almost zero, a potential at the base common to the transistors Q3 and Q4 is substantially equal to the potential at the node A (= node B).

Under this condition, the base-emitter voltage VBE1 of each of the transistors Q1 and Q2 is by RI smaller than that VBE2 of each of the transistors Q3 and Q4. Assuming that a current value of each current I3 and I4 is Iout, and a thermoelectromotive force of each transistor Q1 to Q4 is $V_T = KT/q$ (where K = Boltzman constant, T = absolute temperature, q = electric charge of electron), a current gain Iout/I of the DC amplifier 20 when $I_1 = I_2$, is expressed by

$$I_{out}/I = \exp[-RI/V_T] \quad (3)$$

The above formula teaches that as the current I from the differential amplifier 12 increases, the current gain Iout/I of the DC amplifier 20 exponentially decreases. Therefore, when $I_1 = I_2$, the output currents I3 and I4 of the DC amplifier 20 are both de-

creased to be extremely small.

Where the currents I3 and I4 are both small, the currents flowing into the transistors Q5 to Q8 in the variable reactance circuit 14 are small. Accordingly, the mutual conductance "gm" of each transistor Q5 to Q8 is also small. This fact implies that the term "gm × R5" in each of the equations (1) and (2) is small, and hence that even if the currents I3 and I4 are somewhat different, the reactance of the variable reactance circuit 14 is little changed by such a difference, and is kept at a value approximately equal to the reference reactance Cref.

Fig. 3 shows a graphical representation of a relationship of the reactance C of the variable reactance circuit 14 vs. difference factor (as given by $\frac{I_3 - I_4}{I_4}$)

of the currents I3 and I4. In the figure, a line L1 indicates the relationship of the circuit of Fig. 2, and a line L2, that of the prior circuit of Fig. 1. To plot the graph, in the circuit of Fig. 2, C1 = 20 pF, R5 = 2.7 kilo ohms, I1 = I2 = 100 uA, and R11 = R12 = 600 ohms. As seen from the graph, in the Fig. 2 circuit according to the invention, the reactance C of the reactance circuit 14 is kept at an almost constant value (here, 20 pF) irrespective of the difference factor. The reason for this is that when $I_1 = I_2$, the output currents I1 and I2 of the DC amplifier 20 are both controlled to be very small.

The description that follows is an operation of the DC amplifier 20 when the current I1 is not equal to that of the current I2.

In the description, it is assumed that $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$. Under this condition, since the base potentials of the transistors Q3 and Q4 are equal to each other, the collector current of the transistor Q3 flowing through the resistor R11 is equal to that of the transistor Q4 flowing through the resistor R12. Specifically, of the current $I + \Delta I$ flowing from the differential amplifier 12 into the node A, the current component ΔI flows into the node B through the resistors R1 and R2, and the current component I flows through the resistor R11 as the collector current of the transistor Q3. Accordingly, the current ΔI from the node A and the current $I - \Delta I$ from the differential amplifier 12 flow into the node B. Therefore, the current value flowing into the resistor R12 in the form of the collector current of the transistor Q4 is equal to I ($= I - \Delta I + \Delta I$). As a result, the collector current of the transistor Q3 flowing through the resistor R11 is equal to that of the transistor Q4 flowing through the resistor R12.

The current ΔI flows from the node A to the node B through the resistors R1 and R2, to produce a potential difference $(R1 + R2) \times \Delta I$ between the nodes A and B. The voltage generated across each of the resistors R11 and R12 is RI. Therefore, a potential difference $(R1 + R2) \times \Delta I$ is caused between the bases of the transistors Q1 and Q2. Thus, when $I_1 \neq I_2$, the DC amplifier 20 amplifies the currents I1 and I2, and produces the currents I3 and I4.

As seen from the foregoing description, in the DC amplifier 20, when $I_1 = I_2$, the values of the currents I_3 and I_4 is controlled to be small. When $I_1 \neq I_2$, the potential difference $(R_1 + R_2) \times \Delta I$ is caused between the bases of the transistors Q1 and Q2 and therefore the satisfactorily large currents I_3 and I_4 are produced.

Fig. 4 is a circuit diagram showing a variable frequency oscillator using a reactance control circuit, which is a second embodiment of the present invention. In this embodiment, a DC amplifier 30 is used in place of the DC amplifier 20 in the first embodiment of Fig. 2. The DC amplifier 30 is made up of NPN transistors Q1 and Q2, and a control circuit 31 for controlling the base potentials of those transistors. The control circuit 31 is made up of resistors R1 and R2, and NPN transistors Q30 and Q40. An emitter area of each of the NPN transistors Q30 and Q40 is larger than that of each of the NPN transistors Q1 and Q2. In this instance, the former is three times as large as the latter.

In the DC amplifier 30, when the currents I_1 and I_2 derived from the differential amplifier 12 are equal to each other, $I_1 = I_2$, a potential at the node A is approximately equal to that at the node B. Accordingly, little current flows between the nodes A and B through the resistors R1 and R2. Under this condition, the potential at the base common to the transistors Q30 and Q40 may be considered to be equal to the potential at the node A (= node B). The base potential of each of the transistors Q1 and Q2 is likewise equal to the potential at the node A (= node B). Accordingly, the base-emitter voltage V_{BE1} of each of the transistors Q1 and Q2 is equal to that V_{BE2} of each of the transistors Q30 and Q40. Since the emitter area of each transistor Q1 and Q2 is $1/3$ as large as that of each transistor Q30 and Q40, the current flowing into each transistor Q1 and Q2 is $1/3$ that flowing into each transistor Q30 and Q40. When the currents I_1 and I_2 derived from the differential amplifier 12 are equal to each other, the output currents I_3 and I_4 of the DC amplifier 30 are both controlled to be small.

When $I_1 \neq I_2$, for example, $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$, the current ΔI flows from the node A to the node B through the resistors R1 and R2. Therefore, a potential difference $(R_1 + R_2) \times \Delta I$ is caused between the nodes A and B. When the currents $I_1 \neq I_2$, the DC amplifier 30 amplifies the currents I_1 and I_2 and produces currents I_3 and I_4 .

Also in the DC amplifier 30, when $I_1 = I_2$, the values of the currents I_3 and I_4 are controlled to be small. When $I_1 \neq I_2$, the potential difference $(R_1 + R_2) \times \Delta I$ is caused between the bases of the transistors Q1 and Q2 and therefore the satisfactorily large currents I_3 and I_4 are produced.

As described above, in the DC amplifier 20 or 30, when $I_1 = I_2$, the currents flowing to the transistors Q1 and Q2 may be reduced. Therefore, when $I_1 = I_2$,

the currents flowing into the differential transistor circuits 141 and 142 in the variable reactance circuit 14 are both small. Therefore, if the transistors Q1 and Q2 are different in geometrics and operating characteristic, a difference between the current flowing to the differential transistor circuit 141 and the current flowing to the differential transistor circuit 142 is very small. For this reason, the reference reactance C_{ref} of the variable reactance circuit 14 is free from the difference of the geometrics and the operating characteristics of the transistors Q1 and Q2. Therefore, a desired reference reactance C_{ref} may be secured.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A reactance control circuit comprising:
 - a variable reactance circuit (14) having first and second differential transistor circuits (141, 142), a reactance of said variable reactance circuit being determined by the currents flowing to said first and second differential transistors (141, 142); and
 - a differential amplifier (12) for producing first and second currents (I_1 , I_2) in accordance with an input voltage (V_{in}); characterized by comprising:
 - a DC amplifier circuit (20; 30) for amplifying the first and second currents (I_1 , I_2) derived from said differential amplifier (12), and for supplying the amplified currents to said variable reactance circuit (14) in order to control the currents flowing to said first and second differential transistor circuits (141, 142);
 - said DC amplifier circuit (20; 30) including first and second input terminals (A, B) for receiving first and second currents (I_1 , I_2) output from said differential amplifier circuit (12), respectively,
 - first and second terminals (C, D) for supplying the third and fourth currents (I_3 , I_4) to said variable reactance circuit (14), respectively,
 - a first transistor (Q1), having a collector coupled with said first output terminal (C), an emitter coupled with a predetermined potential supplying terminal (Gnd), and a base,
 - a second transistor (Q2), having a collector coupled with said second output terminal (D), an emitter coupled with said predetermined potential supplying terminal (Gnd), and a base, and
 - base potential control means for, when said first and second currents (I_1 , I_2) differ from each other, supplying different potentials to the bases of said first and second transistors (Q1, Q2) so that third and fourth currents (I_3 , I_4)



As seen from the foregoing description, in the DC amplifier 20, when $I_1 = I_2$, the values of the currents I_3 and I_4 is controlled to be small. When $I_1 \neq I_2$, the potential difference $(R_1 + R_2) \times \Delta I$ is caused between the bases of the transistors Q1 and Q2 and therefore the satisfactorily large currents I_3 and I_4 are produced.

Fig. 4 is a circuit diagram showing a variable frequency oscillator using a reactance control circuit, which is a second embodiment of the present invention. In this embodiment, a DC amplifier 30 is used in place of the DC amplifier 20 in the first embodiment of Fig. 2. The DC amplifier 30 is made up of NPN transistors Q1 and Q2, and a control circuit 31 for controlling the base potentials of those transistors. The control circuit 31 is made up of resistors R1 and R2, and NPN transistors Q30 and Q40. An emitter area of each of the NPN transistors Q30 and Q40 is larger than that of each of the NPN transistors Q1 and Q2. In this instance, the former is three times as large as the latter.

In the DC amplifier 30, when the currents I_1 and I_2 derived from the differential amplifier 12 are equal to each other, $I_1 = I_2$, a potential at the node A is approximately equal to that at the node B. Accordingly, little current flows between the nodes A and B through the resistors R1 and R2. Under this condition, the potential at the base common to the transistors Q30 and Q40 may be considered to be equal to the potential at the node A (= node B). The base potential of each of the transistors Q1 and Q2 is likewise equal to the potential at the node A (= node B). Accordingly, the base-emitter voltage V_{BE1} of each of the transistors Q1 and Q2 is equal to that V_{BE2} of each of the transistors Q30 and Q40. Since the emitter area of each transistor Q1 and Q2 is $1/3$ as large as that of each transistor Q30 and Q40, the current flowing into each transistor Q1 and Q2 is $1/3$ that flowing into each transistor Q30 and Q40. When the currents I_1 and I_2 derived from the differential amplifier 12 are equal to each other, the output currents I_3 and I_4 of the DC amplifier 30 are both controlled to be small.

When $I_1 \neq I_2$, for example, $I_1 = I + \Delta I$ and $I_2 = I - \Delta I$, the current ΔI flows from the node A to the node B through the resistors R1 and R2. Therefore, a potential difference $(R_1 + R_2) \times \Delta I$ is caused between the nodes A and B. When the currents $I_1 \neq I_2$, the DC amplifier 30 amplifies the currents I_1 and I_2 and produces currents I_3 and I_4 .

Also in the DC amplifier 30, when $I_1 = I_2$, the values of the currents I_3 and I_4 are controlled to be small. When $I_1 \neq I_2$, the potential difference $(R_1 + R_2) \times \Delta I$ is caused between the bases of the transistors Q1 and Q2 and therefore the satisfactorily large currents I_3 and I_4 are produced.

As described above, in the DC amplifier 20 or 30, when $I_1 = I_2$, the currents flowing to the transistors Q1 and Q2 may be reduced. Therefore, when $I_1 = I_2$,

the currents flowing into the differential transistor circuits 141 and 142 in the variable reactance circuit 14 are both small. Therefore, if the transistors Q1 and Q2 are different in geometrics and operating characteristic, a difference between the current flowing to the differential transistor circuit 141 and the current flowing to the differential transistor circuit 142 is very small. For this reason, the reference reactance C_{ref} of the variable reactance circuit 14 is free from the difference of the geometrics and the operating characteristics of the transistors Q1 and Q2. Therefore, a desired reference reactance C_{ref} may be secured.

Reference signs in the claims are intended for better understanding and shall not limit the scope.

Claims

1. A reactance control circuit comprising:
 - a variable reactance circuit (14) having first and second differential transistor circuits (141, 142), a reactance of said variable reactance circuit being determined by the currents flowing to said first and second differential transistors (141, 142); and
 - a differential amplifier (12) for producing first and second currents (I_1 , I_2) in accordance with an input voltage (V_{in}); characterized by comprising:
 - a DC amplifier circuit (20; 30) for amplifying the first and second currents (I_1 , I_2) derived from said differential amplifier (12), and for supplying the amplified currents to said variable reactance circuit (14) in order to control the currents flowing to said first and second differential transistor circuits (141, 142);
 - said DC amplifier circuit (20; 30) including first and second input terminals (A, B) for receiving first and second currents (I_1 , I_2) output from said differential amplifier circuit (12), respectively,
 - first and second terminals (C, D) for supplying the third and fourth currents (I_3 , I_4) to said variable reactance circuit (14), respectively,
 - a first transistor (Q1), having a collector coupled with said first output terminal (C), an emitter coupled with a predetermined potential supplying terminal (Gnd), and a base,
 - a second transistor (Q2), having a collector coupled with said second output terminal (D), an emitter coupled with said predetermined potential supplying terminal (Gnd), and a base, and
 - base potential control means for, when said first and second currents (I_1 , I_2) differ from each other, supplying different potentials to the bases of said first and second transistors (Q1, Q2) so that third and fourth currents (I_3 , I_4)



corresponding to said first and second currents (I1, I2) flow through said first and second transistors (Q1, Q2), respectively,

when the first and second currents (I1, I2) are equal to each other, supplying a predetermined low potential to the bases of the first and second transistor (Q1, Q2) so that the third and fourth currents (I3, I4) flowing to the first and second transistor (Q1, Q2) are both reduced.

2. The reactance control circuit according to claim 1, characterized in that said base potential control means (21) includes a third transistor (Q3), having a collector connecting to the base of said first transistor (Q1), an emitter coupled with said predetermined potential supplying terminal (Gnd), and a base, a fourth transistor (Q4), having a collector connected to the base of said second transistor (Q2), an emitter coupled with said predetermined potential supplying terminal (Gnd), and a base interconnected with the base of said third transistor (Q3), a first impedance element (R1), located between said first input terminal (A) and the base common to said third and fourth transistors (Q3, Q4), a second impedance element (R2), located between said second input terminal (B) and the base common to said third and fourth transistors (Q3, Q4), a third impedance element (R11), located between said first input terminal (A) and the base of said first transistor (Q1), and a fourth impedance element (R12), located between said second input terminal (B) and the base of said second transistor (Q2).
3. The reactance control circuit according to claim 2, characterized in that said first and second impedance elements (R1, R2) have equal resistance values.
4. The reactance control circuit according to claim 2, characterized in that said third and fourth impedance elements (R11, R12) have equal resistance values.
5. The reactance control circuit according to claim 2, characterized in that said first to fourth transistors (Q1, Q2, Q3, Q4) have equal geometrics.
6. The reactance control circuit according to claim 1, characterized in that said base potential control means (31) includes a third transistor (Q30), having a collector coupled with the base of said first transistor (Q1), an emitter having an area N times as large as an emitter area of said first transistor (Q1) coupled with said predetermined potential supplying terminal (Gnd), and a base, a fourth transistor (Q40), having a collector coupled with

the base of said second transistor (Q2), an emitter having an area N times as large as an emitter area of said second transistor (Q2) coupled with said predetermined potential supply terminal (Gnd), and a base coupled with the base of said third transistor (Q30), a first impedance element (R1), located between said first input terminal (A) and the base common to said third and fourth transistors (Q30, Q40), and a second impedance element (R2), located between said second input terminal (B) and the base common to said third and fourth transistors (Q30, Q40).

7. The reactance control circuit according to claim 6, characterized in that said first and second impedance elements (R1, R2) have equal resistance values.
8. The reactance control circuit according to claim 6, characterized in that said first and second transistors (Q1, Q2) have equal geometrics.

Patentansprüche

1. Reaktanzsteuerschaltung, welche umfaßt:
eine Schaltung mit variabler Reaktanz (14) mit ersten und zweiten Differentialtransistorschaltungen (141, 142), wobei eine Reaktanz der Schaltung mit variabler Reaktanz bestimmt ist durch die Ströme, die an die ersten und zweiten Differentialtransistoren (141, 142) fließen; und einen Differentialverstärker (12) zum Erzeugen erster und zweiter Ströme (I1, I2) in Übereinstimmung mit einer Eingabespannung (Vin);
gekennzeichnet durch
eine DC-Verstärkerschaltung (20; 30) zum Verstärken der ersten und zweiten Ströme (I1, I2), die sich ableiten aus dem Differentialverstärker (12); und zum Zuführen der verstärkten Ströme an die Schaltung mit variabler Reaktanz (14) zum Steuern der Ströme, die an die ersten und zweiten Differentialtransistorschaltungen (141, 142) fließen;
wobei die DC-Verstärkerschaltung (20; 30) beinhaltet:
erste und zweite Eingabeanschlüsse (A,B) zum Empfangen erster und zweiter Ströme (I1, I2), ausgegeben von der Differentialverstärkerschaltung (12);
erste und zweite Anschlüsse (C, D) zum Zuführen der dritten und vierten Ströme (I3, I4) an die Schaltung mit variabler Reaktanz (14);
einen ersten Transistor (Q1) mit einem Kollektor, der verbunden ist mit dem ersten Ausgabeanschluß (C), einem Emmitter, der verbunden ist mit einem Zuführungsanschluß für ein vorbestimm-



- tes Potential (Gnd), und einer Basis;
einen zweiten Transistors (Q2) mit einem Kollektor, der verbunden ist mit dem zweiten Ausgabeanschluß (D), einem Emitter, der verbunden ist mit dem Zuführungsanschluß für das vorbestimmte Potential (Gnd), und einer Basis; und eine Basispotential-Steuereinrichtung zum Zuführen verschiedener Potentiale an die Basen der ersten und zweiten Transistoren (Q1, Q2), wenn die ersten und zweiten Ströme (I1, I2) voneinander verschieden sind, so daß dritte und vierte Ströme (I3, I4) entsprechend den ersten und zweiten Strömen (I1, I2) durch die ersten und zweiten Transistoren (Q1, Q2) jeweils fließen, und wenn die ersten und zweiten Ströme (I1, I2) gleich einander sind, zum Zuführen eines vorbestimmten Niedrigpotentials an die Basis des ersten und zweiten Transistors (Q1, Q2), so daß die dritten und vierten Ströme (I3, I4), die zu den ersten und zweiten Transistoren (Q1, Q2) fließen, beide reduziert sind.
2. Reaktanzsteuerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Basispotential-Steuereinrichtung (21) einen dritten Transistor (Q3) beinhaltet mit einem Kollektor, der verbunden ist mit der Basis des ersten Transistors (Q1), einem Emitter, der verbunden ist mit dem Zuführungsanschluß für das vorbestimmte Potential (Gnd), und einer Basis, einen vierten Transistor (Q4) mit einem Kollektor, der verbunden ist mit der Basis des zweiten Transistors (Q2), einem Emitter, der verbunden ist mit dem Zuführungsanschluß für das vorbestimmte Potential (Gnd), und einer Basis, die verbunden ist mit der Basis des dritten Transistors (Q3), ein erstes Impedanzelement (R1), angesiedelt zwischen dem ersten Eingabeanschluß (A) und der Basis, die gemeinsam ist den dritten und vierten Transistor (Q3, Q4), ein zweites Impedanzelement (R2), angesiedelt zwischen dem zweiten Eingabeanschluß (B) und der Basis, die gemeinsam ist dem dritten und vierten Transistor (Q3, Q4), ein drittes Impedanzelement (R11), angesiedelt zwischen dem ersten Eingabeanschluß (A) und der Basis des ersten Transistors (Q1), und ein viertes Impedanzelement (R12), angesiedelt zwischen dem zweiten Eingabeanschluß (B) und der Basis des zweiten Transistors (Q2).
 3. Reaktanzsteuerschaltung nach Anspruch 2, dadurch gekennzeichnet, daß die ersten und zweiten Impedanzelemente (R1, R2) gleiche Widerstandswerte haben.
 4. Reaktanzsteuerschaltung nach Anspruch 2, dadurch gekennzeichnet, daß die dritten und vierten Impedanzelemente (R11, R12) gleiche Wider-

standswerte haben.

5. Reaktanzsteuerschaltung nach Anspruch 2, dadurch gekennzeichnet, daß die ersten bis vierten Transistoren (Q1, Q2, Q3, Q4) gleiche Geometrien haben.
6. Reaktanzsteuerschaltung nach Anspruch 1, dadurch gekennzeichnet, daß die Basispotential-Steuereinrichtung (31), einen dritten Transistor (Q30) beinhaltet, mit einem Kollektor, der verbunden ist mit der Basis des ersten Transistors (Q1), einem Emitter mit einer Fläche, die N mal so groß ist wie ein Emitterbereich des ersten Transistors (Q1), der verbunden ist mit dem Zuführungsanschluß für das vorbestimmte Potential (Gnd), und einer Basis, einen vierten Transistor (Q40) mit einem Kollektor, der verbunden ist mit einer Basis des zweiten Transistors (Q2), einem Emitter mit einem Bereich, der N mal so groß ist wie ein Emitterbereich des zweiten Transistors (Q2), der verbunden ist mit dem Zuführungsanschluß für das vorbestimmte Potential (Gnd), und einer Basis, die verbunden ist mit der Basis des dritten Transistors (Q30), ein erstes Impedanzelement (R1), angesiedelt zwischen dem ersten Eingabeanschluß (A) und der Basis, die gemeinsam ist dem dritten und vierten Transistor (Q30, Q40), und ein zweites Impedanzelement (R2), angesiedelt zwischen dem zweiten Eingabeanschluß (B) und der Basis, die gemeinsam ist für den dritten und vierten Transistor (Q30, Q40).
7. Reaktanzsteuerschaltung nach Anspruch 6, dadurch gekennzeichnet, daß die ersten und zweiten Impedanzelemente (R1, R2) gleiche Widerstandswerte haben.
8. Reaktanzsteuerschaltung nach Anspruch 6, dadurch gekennzeichnet, daß die ersten und zweiten Transistoren (Q1, Q2) gleiche Geometrien haben.

Revendications

1. Circuit de commande de réactance comprenant :
un circuit de réactance variable (14) ayant des premier et second circuits différentiels de transistor (141, 142), une réactance dudit circuit de réactance variable étant déterminée par les courants passant dans lesdits premier et second transistors différentiels (141, 142) ; et
un amplificateur différentiel (12) pour produire des premier et second courants (I1, I2) selon une tension d'entrée (Vin) ; caractérisé en ce qu'il comprend :
un circuit amplificateur de courant continu



(20 ; 30) pour amplifier les premier et second courants (I1, I2) dérivés dudit amplificateur différentiel (12), et pour fournir les courants amplifiés audit circuit de réactance variable (14) afin de commander les courants passant dans lesdits premier et second circuits différentiels de transistor (141, 142) ;

ledit circuit amplificateur de courant continu (20, 30) comprenant :

des première et seconde bornes d'entrée (A, B) pour recevoir respectivement, des premier et second courants (I1, I2) fournis par ledit circuit amplificateur différentiel (12),

des première et seconde bornes (C, D) pour fournir respectivement, les troisième et quatrième courants (I3, I4) audit circuit de résistance variable (14),

un premier transistor (Q1), ayant un collecteur couplé à ladite première borne de sortie (C), un émetteur couplé à une borne de fourniture de potentiel prédéterminé (Gnd) et une base,

un second transistor (Q2), ayant un collecteur couplé à ladite seconde borne de sortie (D), un émetteur couplé à ladite borne de fourniture de potentiel prédéterminé (Gnd), et une base, et

un dispositif de commande de potentiel de base pour, lorsque lesdits premier et second courants (I1, I2) diffèrent l'un de l'autre, fournir différents potentiels aux bases desdits premier et second transistors (Q1 et Q2) pour que des troisième et quatrième courants (I3, I4) correspondant auxdits premier et second courants (I1, I2) passent respectivement à travers lesdits premier et second transistors (Q1, Q2),

lorsque les premier et second courants (I1, I2) sont égaux l'un à l'autre, fournir un potentiel de niveau bas prédéterminé aux bases des premier et second transistors (Q1, Q2) pour que les troisième et quatrième courants (I3, I4) passant dans les premier et second transistors (Q1, Q2) soient tous les deux réduits.

2. Circuit de commande de réactance selon la revendication 1, caractérisé en ce que ledit dispositif de commande de potentiel de base (21) comprend un troisième transistor (Q3), ayant un collecteur reliant la base dudit premier transistor (Q1), un émetteur couplé à ladite borne de fourniture de potentiel prédéterminé (Gnd), et une base, un quatrième transistor (Q4), ayant un collecteur relié à la base dudit second transistor (Q2), un émetteur couplé à ladite borne de fourniture de potentiel prédéterminé (Gnd), et une base interconnectée à la base dudit troisième transistor (Q3), un premier élément d'impédance (R1), situé entre ladite première borne d'entrée (A) et la borne commune auxdits troisième et quatrième transistors (Q3, Q4), un second élé-

ment d'impédance (R2), situé entre ladite seconde borne d'entrée (B) et la base commune auxdits troisième et quatrième transistors (Q3, Q4), un troisième élément d'impédance (R11), situé entre ladite première borne d'entrée (A) et la base dudit premier transistor (Q1), et un quatrième élément d'impédance (R12) situé entre ladite seconde borne d'entrée (B) et la base dudit second transistor (Q2).

3. Circuit de commande de réactance selon la revendication 2, caractérisé en ce que lesdits premier et second éléments d'impédance (R1, R2) ont des valeurs de résistances égales.

4. Circuit de commande de réactance selon la revendication 2, caractérisé en ce que lesdits troisième et quatrième éléments d'impédance (R11, R12) ont des valeurs de résistance égales.

5. Circuit de commande de réactance selon la revendication 2, caractérisé en ce que lesdits premier au quatrième transistors (Q1, Q2, Q3, Q4) ont des géométries égales.

6. Circuit de commande de réactance selon la revendication 1, caractérisé en ce que ledit dispositif de commande de potentiel de base (31) comprend un troisième transistor (Q30) ayant un collecteur couplé à la base dudit premier transistor (Q1), un émetteur ayant une zone N fois plus grande qu'une zone d'émetteur dudit premier transistor (Q1) couplé à ladite borne de fourniture de potentiel prédéterminé (Gnd), et une base, un quatrième transistor (Q40), ayant un collecteur couplé à la base dudit second transistor (Q2), un émetteur ayant une surface N fois plus grande qu'une surface d'émetteur dudit second transistor (Q2) couplé à ladite borne de fourniture de potentiel prédéterminé (Gnd), et une base couplée à la base dudit troisième transistor (Q30), un premier élément d'impédance (R1), situé entre ladite première borne d'entrée (A) et la base commune auxdits troisième et quatrième transistors (Q30, Q40), et un second élément d'impédance (R2) situé entre ladite seconde borne d'entrée (B) et la base commune auxdits troisième et quatrième transistors (Q30, Q40).

7. Circuit de commande de réactance selon la revendication 6, caractérisé en ce que lesdits premier et second éléments d'impédance (R1, R2) ont des valeurs de résistances égales.

8. Circuit de commande de réactance selon la revendication 6, caractérisé en ce que lesdits premier et second transistors (Q1, Q2) ont des géométries égales.