

(19) World Intellectual Property Organization
International Bureau



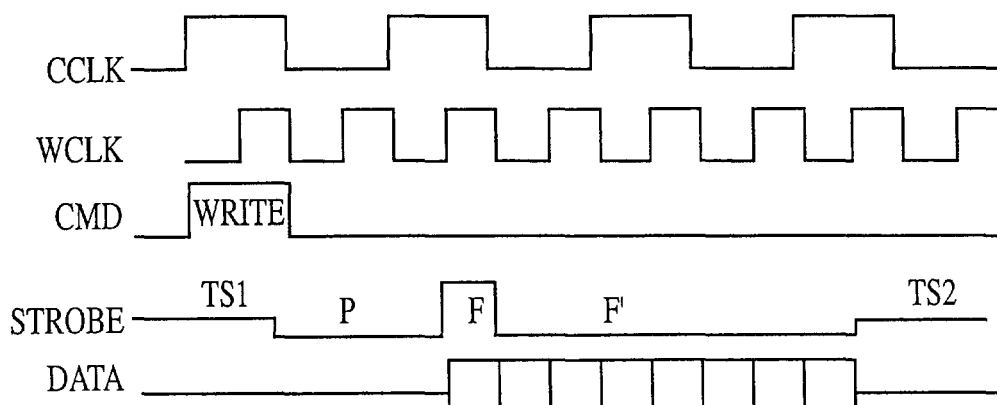
(43) International Publication Date
28 February 2002 (28.02.2002)

PCT

(10) International Publication Number
WO 02/17323 A2

- (51) International Patent Classification⁷: **G11C 7/00**
- (21) International Application Number: PCT/US01/25957
- (22) International Filing Date: 21 August 2001 (21.08.2001)
- (25) Filing Language: English
- (26) Publication Language: English
- (30) Priority Data:
09/641,516 21 August 2000 (21.08.2000) US
- (71) Applicant: **MICRON TECHNOLOGY, INC.** [US/US];
8000 S. Federal Way, Boise, ID 83707-0006 (US).
- (72) Inventors: **KEETH, Brent**; 5077 N. Fifeshire Place,
Boise, ID 83713 (US). **JOHNSON, Brian**; 5977 E.
Gateway Dr., Boise, ID 83716 (US).
- (74) Agent: **MINUTOLI, Gianni**; Dickstein Shapiro Morin &
Oshinsky LLP, 2101 L Street NW, Washington, DC 20037-
1526 (US).
- (81) Designated States (*national*): AE, AG, AL, AM, AT, AU,
AZ, BA, BB, BG, BR, BY, BZ, CA, CH, CN, CO, CR, CU,
CZ, DE, DK, DM, DZ, EC, EE, ES, FI, GB, GD, GE, GH,
GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC,
LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW,
MX, MZ, NO, NZ, PH, PL, PT, RO, RU, SD, SE, SG, SI,
SK, SL, TJ, TM, TR, TT, TZ, UA, UG, UZ, VN, YU, ZA,
ZW.
- (84) Designated States (*regional*): ARIPO patent (GH, GM,
KE, LS, MW, MZ, SD, SL, SZ, TZ, UG, ZW), Eurasian
patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European
patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE,
IT, LU, MC, NL, PT, SE, TR), OAPI patent (BF, BJ, CF,
CG, CI, CM, GA, GN, GQ, GW, ML, MR, NE, SN, TD,
TG).
- Published:**
— *without international search report and to be republished
upon receipt of that report*
- For two-letter codes and other abbreviations, refer to the "Guid-
ance Notes on Codes and Abbreviations" appearing at the begin-
ning of each regular issue of the PCT Gazette.*

(54) Title: SYNCHRONIZED WRITE DATA ON A HIGH SPEED MEMORY BUS



(57) **Abstract:** Some synchronous semiconductor memory devices accept a command clock which is buffered and a write clock which is unbuffered. Write command are synchronized to the command clock while the associated write data is synchronized to the write clock. Due to the use of the buffer, an arbitrary phase shift can exist between the command and write clocks. The presence of the phase shift between the two clocks makes it difficult to determine when a memory device should accept write data associated a write command. A synchronous memory device in accordance with the present invention utilizes the unbuffered strobe signal which is normally tristated during writes as a flag to mark the start of write data. A preamble signal may be asserted on the strobe signal line prior to asserting the flag signal in order to simplify flag detection.