

METHOD AND RELATED CIRCUIT FOR PROVIDING SUPPLEMENTAL DIELECTRIC MATERIAL

BACKGROUND

Relevant Field

[0001] The present disclosure relates to transistors. In particular, the present disclosure relates to transistor devices and methods of manufacturer using a supplemental dielectric layer.

Description of Related Art

[0002] Field-effect transistors (“FETs”) are transistors that utilize an electric field to control or modify current flowing between a source terminal and a drain terminal. The electric field is generated by a voltage applied to a gate terminal of the FET. FETs use electrons and/or holes as charge carriers to achieve this effect. FETs can be predominantly majority-charge-carrier devices or minority-charge-carrier devices. The voltage applied to the gate of the FET creates an active channel through which the charge carriers flow from the source terminal to the drain terminal. The non-linear impedance through this channel can be varied by applying different voltages to the gate terminal relative to the source and/or drain terminals. However, these characteristics are ephemeral because as soon as the voltage is no longer applied, the FET quickly returns to its original, resting state.

[0003] Ferroelectric field-effect transistors (“FeFETs”) are FETs that include a ferroelectric material. Ferroelectric materials are materials that have electric polarization (or polarization density). The electric field polarization of the ferroelectric material can be used to create an active channel within the FeFET. By utilizing this property of the ferroelectric material, the electric field polarization in the ferroelectric material may be used to retain the FeFET’s state in the absence of any electrical bias. That is, the FeFET can retain information in the ferroelectric material without having any external power applied to it. This feature makes FeFETs suitable for non-volatile memory applications that involve discrete or continuous values.

[0004] SUMMARY

[0005] The method of making an integrated circuit device involves forming a dielectric layer, creating an active layer on top of the dielectric layer, and then forming a supplemental dielectric layer on the dielectric layer. In one embodiment of the method, the supplemental dielectric layer can deposit dielectric material substantially without depositing the active layer. In another

embodiment of the method, an electrode is formed prior to forming the dielectric layer. In one embodiment of the method, the electrode used can be a gate electrode. Additionally, the method may also involve forming adjacent dielectric material adjacent to the electrode. In one embodiment of the method, forming the active layer involves etching away a portion of the active layer.

[0006] In another embodiment, the method also involves applying an active mask to etch away a non-active layer portion, thereby forming the active layer, and using the active mask to deposit the supplemental dielectric layer on the dielectric layer. In one embodiment of the method, an active mask is applied to deposit the active layer, followed by the application of a supplemental dielectric mask to deposit the supplemental dielectric layer on the dielectric layer. In another embodiment of the method, an opposite-active mask is used to deposit the supplemental dielectric layer on the dielectric layer. In one embodiment, the method involves forming the integrated circuit on a back-end-of-the-line. Additionally, in another embodiment, the active layer of the method can be made of ferroelectric material.

[0007] In another aspect, an integrated circuit is disclosed that consists of several layers, including a first electrode, a dielectric layer placed on top of the first electrode, an active layer on the dielectric layer, and a supplemental layer adjacent to the active layer. Optionally, the integrated circuit may also feature a metal connection, with the first electrode being situated on this metal connection. In one embodiment of the integrated circuit, there is an adjacent dielectric material disposed next to the metal connection, along with another supplemental layer that is placed on top of the adjacent dielectric material. Additionally, the integrated circuit may feature a second electrode disposed on the first portion of the active layer and a third electrode disposed on the second portion of the active layer. In one embodiment, the integrated circuit features a first electrode as a gate electrode and a second electrode as a drain electrode. Additionally, this integrated circuit may also include a first metal connector coupled to the first electrode, a second metal connector coupled to the second electrode, and a third metal connector coupled to the third electrode as optional features. The integrated circuit, as described in one embodiment, further comprises an adjacent dielectric that is disposed adjacent to the first electrode. The integrated circuit comprises a first electrode for providing a gate, a dielectric layer for insulation disposed on the first electrode, an active layer for a ferroelectric effect disposed on the dielectric layer, and a supplemental layer for additional insulation. Furthermore, the integrated circuit may optionally include a second electrode for providing a drain, which is disposed on a first portion of the active layer, and a third electrode for providing a source, which is disposed on a second portion of the active layer.

BRIEF DESCRIPTION OF THE DRAWINGS

[0008] These and other aspects will become more apparent from the following detailed description of the various embodiments of the present disclosure with reference to the drawings wherein:

[0009] Fig. 1 shows a block diagram of an artificial intelligence accelerator that utilizes FeFET memory in accordance with an embodiment of the present disclosure;

[0010] Fig. 2 shows a diagram of a memory cell utilizing a FeFET transistor in accordance with an embodiment of the present disclosure;

[0011] Fig. 3 illustrates operating characteristics of the FeFET of Fig. 2 when used to store binary states in accordance with an embodiment of the present disclosure;

[0012] Fig. 4 illustrates operating characteristics of the FeFET of Fig. 2 when used to store a continuous value, such as a weight of a neuromorphic cell, in accordance with an embodiment of the present disclosure; and

[0013] Fig. 5 shows a memory array utilizing FeFET transistors in accordance with an embodiment of the present disclosure; and

[0014] Figs. 6A-6D show several drawings of a transistor, such as a FeFET, to illustrate a manufacturing method of utilizing a supplemental dielectric layer in accordance with an embodiment of the present disclosure.

DETAILED DESCRIPTION

[0015] Fig. 1 shows a block diagram of an Artificial Intelligence (“AI”) accelerator 100 that utilizes FeFET memory 112 in accordance with an embodiment of the present disclosure. The AI accelerator 100 may be implemented on a semiconductor device, a custom integrate circuit, an application-specific integrated circuit (“ASIC”), a graphics processing unit (“GPU”), a field-programmable gate array (“FPGA”), any device known to one of ordinary skill in the art, or some combination thereof. The AI accelerator 100 includes a processing element (“PE”) array 102 that performs the majority of AI computation. The PE array 102 performs the AI computations using a plurality of processing elements 110. These processing elements 110 may form a manycore processor where each processing element 110 performs AI calculations in parallel with the other processing elements 110. Additionally or alternatively, the processing elements 110 may include an arithmetic logic unit, a neuromorphic computation element, a processor, a multicore processor,

a manycore processor, a reduced instruction set computer (“RISC”) processor, and/or other computation device known to one of ordinary skill in the relevant art.

[0016] The processing elements 110 may each be part of a neuromorphic circuit; for example, the processing elements 110 may each form a portion of an artificial neural network where each accompanying memory 112 is an analog memory configured to act as parameters for artificial neurons (e.g., weights), in some specific embodiments. Each processing element 110 and its respective memory 112 may form an in-memory processing architecture, e.g., to enable efficient and parallel execution of multiply-accumulate operations, in yet additional embodiments.

[0017] The memories 112 are implemented using FeFETs described in further detail below. The memories 112 may store binary data and/or may store analog data in some specific embodiments. Additionally or alternatively, the memories 112 may store a combination of binary and analog data in some embodiments.

[0018] The AI accelerator 100 may also include a shared memory 108. Computations computed by the PE array 102 may be stored and/or instructed by information stored on a shared memory 104 internal to the AI accelerator and/or shared memory 108 stored off of the AI accelerator 100. The shared memory 104 and/or the shared memory 108 may utilize the FeFET memory cells as described herein. The AI accelerator 100 also includes a Network-on-Chip 106 for communicating with other devices, e.g., via TCP/IP, Ethernet, Wifi, etc.

[0019] Fig. 2 shows a diagram of a memory cell 200 utilizing a FeFET 202 in accordance with an embodiment of the present disclosure. The memory cell 200 also includes a program-signal circuit 206 and a sense circuit 204. The program-signal circuit 206 may apply one or more positive-voltage pulse signals or negative-voltage pulse signals to program the FeFET 202. The FeFET 202 includes a drain 210, a source 212, and a gate 208. However, because of the symmetry of the FeFET 202, the operation of the drain 210 and source 212 may be reversed.

[0020] The FeFET 202 may be powered by a Vread voltage that is relative to a voltage SL. The Vread voltage may be a ground, may be a fixed voltage, may be a programmable voltage, may be a variable voltage, may be coupled to a ground or a voltage source via another transistor (not shown), etc. Similarly, the SL reference may be a ground, may be a fixed voltage, may be a programmable voltage, may be a variable voltage, may be coupled to a ground or a voltage source via another transistor (not shown), etc. For example, the voltage Vread and the voltage SL may be predetermined values to enable a fixed voltage between the drain 210 and the source 212, for example, intermittently or continuously, etc. In other embodiments, the voltage Vread and the

voltage SL may be set to enable a constant current from the drain 210 to the source 212, for example intermittently or continuously, etc.

[0021] The voltages applied to the gate 208 of the FeFET 202 by the program-signal circuit 206 can cause the ferroelectric material in the FeFET 202 to form an electric polarization. The ferroelectric polarization can remain (or substantially remains) long after the voltage applied to the gate 208 of the FeFET 202 is removed if the voltage was of sufficient magnitude and duration to change the state of the ferroelectric material. This is a result of a stable electric polarization in the ferroelectric material. The ferroelectric material is an insulator in which the electric polarization induced by an applied electric field from a voltage applied to the gate 208 remains after removal of that voltage.

[0022] Positive voltage biases (or pulses) from the program-signal circuit 206 applied to the gate 208 of the FeFET 202 results in a reduction in the threshold voltage of the FeFET 202 and brings the channel of the FeFET 202 into accumulation mode. And negative voltage bias (or pulses) from the program-signal circuit 206 applied to the gate 208 of the FeFET 202 results in an increase in the threshold voltage of the FeFET 202 and brings the channel of the FeFET 202 into depletion mode. The first state may correspond to a 0-value and the second state may correspond to a 1-value, or visa-versa.

[0023] Referring to Figs. 2-3: Fig. 3 illustrates operating characteristics of the FeFET 202 of Fig. 2 in a graph 300 when used to store binary states in accordance with an embodiment of the present disclosure. The graph 300 shows an axis 302 that shows a current, I_{ds} , that is the current from the drain 210, through the FeFET 202, and through the source 212 to ground. The current I_{ds} passes through a channel of the FeFET 202 where the channel has characteristics based upon the polarization of the ferroelectric material. The graph 300 also includes an axis 304 that shows the voltage at the gate 208 of Fig. 2. The V_g values applied to the gate 208 may be within a range of voltages to determine the state of the FeFET without significantly disturbing the ferroelectric material's polarization.

[0024] Fig. 3 illustrates the relationship between the I_{ds} and V_g based upon the state of the FeFET 202 in accordance with an embodiment of the present disclosure. A first curve 306 shows the FeFET 202 in a first state because it has a first threshold voltage 308. A second curve 308 shows the FeFET 202 in a second state because it has a second threshold voltage 312. The states of the FeFET 202 may be programmed by the program-signal circuit 206 to change the electric polarization of the ferroelectric material in the FeFET 202. These states may be detected by the

sense circuit 302. In some embodiments, no V_g voltage needs to be applied to the FeFET 202 to determine the state; however, in other embodiments, a sufficient voltage needs to be applied to the gate 208 to determine the state of the FeFET, but without programming the FeFET 202.

[0025] Referring to Figs. 2 and 4: Fig. 4 illustrates operating characteristics of the FeFET 202 of Fig. 2 in a graph 400 when the FeFET 202 is used to store a continuous value, such as a weight of a neuromorphic cell, in accordance with an embodiment of the present disclosure.

[0026] The graph 400 shows an axis 402 for a current I_{ds} . I_{ds} is the current from the drain 210 through the FeFET 202 and through the source 212 to ground. The current I_{ds} passes through a channel of the FeFET 202 where the channel has characteristics based upon the polarization of the ferroelectric material. The graph 400 also includes an axis 404 that shows the voltage at the gate 208 of Fig. 2. The V_g values applied to the gate 208 may be within a range of voltages to determine the state of the FeFET without significantly disturbing the ferroelectric material's polarization.

[0027] Fig. 4 illustrates the relationship between the I_{ds} and V_g based upon the polarization of the FeFET 202 in accordance with an embodiment of the present disclosure. As the polarization changes, the characteristic curve shifts as indicated by arrow 408. These shifting curves cause the threshold voltages 406 to shift as well. These values may be mapped to a weight of an artificial neural network. For example, an arithmetic logic unit may read these values for computation within a processing element of Fig. 1. In some embodiments, the memory is used as in-memory-computing, and along with other analog circuit, can perform the calculations of an artificial neural net in accordance with the mapped value corresponding to a weight of a neural network cell, e.g., neuron. During a neural network training phase, the AI accelerator 100 may use the program-signal circuit 206 to change the electric polarization of the ferroelectric material in the FeFET 202 to correspond to a neuron weight. These threshold voltages 406 may be detected by the sense circuit 204. In some embodiments, no V_g voltage needs to be applied to the FeFET 202 to determine its state; however, in other embodiments, a voltage is applied to the gate 208.

[0028] Fig. 5 shows a memory array 500 utilizing FeFET transistors 514 in accordance with an embodiment of the present disclosure. The FeFET transistors 514 each have a polarization state. An interface circuit (not shown) can select one of the word lines 502, 504, or 506, to activate a column of FeFET transistors 514. These activated FeFETs 514 coupled to the activated word line, e.g., 504, causes each of the bit lines 508, 510, 512 to output the state (or value) that corresponds to the ferroelectric's electric polarization in each respective one of the FeFETs 514. One of ordinary skill in the art will appreciate that the array of FeFETs 514 can be increased to have a target memory

size. Additionally, one of ordinary skill in the relevant art will appreciate that programming circuitry may be added to the memory array 500.

[0029] The FeFET transistors 512 may be powered by a voltage from the bit lines 502, 504, 506 that is relative to the voltages SL. The SL references may be a ground, may be a fixed voltage, may be a programmable voltage, may be a variable voltage, may be coupled to a ground or a voltage source via another transistor (not shown), etc.

[0030] Figs. 6A-6D show several drawings of a transistor, such as a FeFET, to illustrate a manufacturing method of utilizing a supplemental dielectric layer in accordance with an embodiment of the present disclosure.

[0031] The transistor 600 may be a MOSFET and/or FeFET. The transistor 600 may be formed on the Back End of the Line (BEOL) to enhance the memory footprint within a chip and enable improved data transfer and calculation capabilities. The transistor 600 includes a conductive connection 602 that may be linked to a lower level and be connected to a gate electrode 622. The gate electrode 622 may have a gate width below 100nm and may utilize the patterned back-gate and/or dual-gate BEOL FET or FeFET device architectures. Surrounding the conductive connection 604 is a dielectric layer 604 that provides insulation. Additionally, another dielectric layer 606 may be applied further enhances insulation properties. The gate electrode 622 is enveloped by another dielectric layer 608, while a dielectric layer 610 covers the gate electrode 622. An active layer 612 may be disposed on the dielectric layer 610. The active layer 612 may be made of a ferroelectric material.

[0032] Because there is always a risk of short between the source electrode 616 or drain electrode 617 to the gate electrode 622, additional steps may follow after forming the active layer as shown in Fig. 6A. Thus, to effectively increase the thickness of the dielectric layer 610 of Fig. 6A in specific areas, namely above the back gate and below the Source/Drain contact outside of the active area more dielectric material may be added.

[0033] The supplemental dielectric layer 614 can mitigate the reduction in dielectric thickness in MOSFET and FeFET devices in the BEOL caused by any etching steps performed after application of the active layer 612. By increasing the thickness of the dielectric layer above the back gate and below the Source/Drain contact outside the active area, the proposed approach helps prevent potential shorts and reliability issues. Furthermore, it efficiently utilizes existing masks, repurposing the Active mask whenever possible and minimizing the need for additional masks unless alignment concerns arise.

[0034] Once the active layer has been patterned as shown in Fig. 6A, a following process that is an etching process is used that can inadvertently reduce the thickness of the dielectric layer 610. Consequently, this can yield a thin dielectric layer primarily in the regions outside the active area 612. Thus, as shown in Fig. 6B, a supplemental dielectric layer 614 may be added. In cases where the "Active mask" is initially created to define the active area and expose the remaining surface for the subsequent etching step, the same mask can be utilized for adding the supplemental dielectric layer 614. This allows for the comprehensive coverage of the active region and provides a conducive environment for the deposition of an additional dielectric layer.

[0035] In other embodiments, e.g., if there are concerns surrounding misalignments or if the primary purpose of the active mask is solely to create an open active area for the channel layer deposition, there are two other embodiments of the method that can be employed: The first method may use "Opposite active" lithography that serves as a viable option to deposit the supplemental dielectric layer 614. This technique can facilitate alignment with the active area, effectively circumventing misalignment concerns that may arise during the process. Another embodiment involves the generation of a completely new mask exclusively designed for this particular step. This may reduce the risk of misalignment issues and complications that may occur in relation to the active area during subsequent stages of the process. After successfully depositing the supplemental dielectric layer 614 in the designated areas, the remaining steps of the standard BEOL FET process can be followed, for example.

[0036] After this, as shown in Fig. 6C, on top of the active layer 612 and the supplemental dielectric layer 614, a source electrode 616 and a drain electrode 617 are positioned. As shown in Fig. 6D, the source electrode 616 and drain electrode 617 are then surrounded by a dielectric layer 618 that also separates the source electrode 616 from the drain electrode 617. A conductive connection 620 links to the source electrode 616 and a separate conductive connection 621 couples to the drain electrode 617 so that additional circuitry may be placed in layers above the transistor 600.

[0037] Various alternatives and modifications can be devised by those skilled in the art without departing from the disclosure. Accordingly, the present disclosure is intended to embrace all such alternatives, modifications and variances. Additionally, while several embodiments of the present disclosure have been shown in the drawings and/or discussed herein, it is not intended that the disclosure be limited thereto, as it is intended that the disclosure be as broad in scope as the art will allow and that the specification be read likewise. Therefore, the above description should not

be construed as limiting, but merely as exemplifications of particular embodiments. And, those skilled in the art will envision other modifications within the scope and spirit of the claims appended hereto. Other elements, steps, methods and techniques that are insubstantially different from those described above and/or in the appended claims are also intended to be within the scope of the disclosure.

[0038] The embodiments shown in the drawings are presented only to demonstrate certain examples of the disclosure. And, the drawings described are only illustrative and are non-limiting. In the drawings, for illustrative purposes, the size of some of the elements may be exaggerated and not drawn to a particular scale. Additionally, elements shown within the drawings that have the same numbers may be identical elements or may be similar elements, depending on the context.

[0039] Where the term "comprising" is used in the present description and claims, it does not exclude other elements or steps. Where an indefinite or definite article is used when referring to a singular noun, e.g., "a," "an," or "the," this includes a plural of that noun unless something otherwise is specifically stated. Hence, the term "comprising" should not be interpreted as being restricted to the items listed thereafter; it does not exclude other elements or steps, and so the scope of the expression "a device comprising items A and B" should not be limited to devices consisting only of components A and B. This expression signifies that, with respect to the present disclosure, the only relevant components of the device are A and B.

[0040] Furthermore, the terms "first," "second," "third," and the like, whether used in the description or in the claims, are provided for distinguishing between similar elements and not necessarily for describing a sequential or chronological order. It is to be understood that the terms so used are interchangeable under appropriate circumstances (unless clearly disclosed otherwise) and that the embodiments of the disclosure described herein are capable of operation in other sequences and/or arrangements than are described or illustrated herein.

What is claimed is:

1. A method of making an integrated circuit device, the method comprising:
forming a dielectric layer;
forming an active layer on the dielectric layer; and
forming a supplemental dielectric layer on the dielectric layer.
2. The method according to claim 1, wherein the supplemental dielectric layer deposits dielectric material substantially without depositing the active layer.
3. The method according to claim 1, the method further comprising:
prior to forming the dielectric layer, forming an electrode.
4. The method according to claim 3, wherein the electrode is a gate electrode.
5. The method according to claim 3, the method further comprising
forming adjacent dielectric material adjacent to the electrode.
6. The method according to claim 1, wherein the act of forming the active layer includes etching away a portion of the active layer.
7. The method according to claim 1, the method further comprising:
applying an active mask to etch away a non-active layer portion to thereby form the active layer; and
applying the active mask to deposit the supplemental dielectric layer on the dielectric layer.

8. The method according to claim 1, the method further comprising:
applying an active mask to deposit the active layer; and
applying a supplemental dielectric mask to deposit the supplemental dielectric layer on the dielectric layer.
9. The method according to claim 1, the method further comprising:
applying an opposite-active mask to deposit the supplemental dielectric layer on the dielectric layer.
10. The method according to claim 1, wherein the integrated circuit is formed on a back-end-of-the-line.
11. The method according to claim 1, wherein the active layer is a ferroelectric material.
12. An integrated circuit, comprising:
a first electrode;
a dielectric layer disposed on the first electrode;
an active layer disposed on the dielectric layer; and
a supplemental layer disposed adjacent to the active layer.
13. The integrated circuit according to claim 12, further comprising a metal connection, wherein the first electrode is disposed on the metal connection.
14. The integrated circuit according to claim 13, further comprising:
adjacent dielectric material disposed adjacent to the metal connection; and

another supplemental layer disposed on the adjacent dielectric material.

15. The integrated circuit according to claim 12, further comprising:
a second electrode disposed on a first portion of the active layer; and
a third electrode disposed on a second portion of the active layer.
16. The integrated circuit according to claim 15, wherein the first electrode is a gate electrode and the second electrode is a drain electrode.
17. The integrated circuit according to claim 15, further comprising:
a first metal connector coupled to the first electrode;
a second metal connector coupled to the second electrode; and
a third metal connector coupled to the third electrode.
18. The integrated circuit according to claim 12, further comprising an adjacent dielectric disposed adjacent to the first electrode.
19. An integrated circuit, comprising:
a first electrode means for providing a gate;
a dielectric layer means for providing insulation, the dielectric means disposed on the first electrode means;
an active layer means for providing a ferroelectric effect, the active layer disposed on the dielectric layer means; and
a supplemental layer means for providing supplemental insulation.
20. The integrated circuit according to claim 19, further comprising:
a second electrode means for providing a drain, the second electrode means disposed on a first portion of the active layer means; and

a third electrode means for providing a source, the third electrode means disposed on a second portion of the active layer means.