

## CLAIMS

What is claimed is

1. An apparatus for catalyst influenced chemical etching, comprising:
  - a process chamber to house a semiconductor wafer;
  - one or more actuators configured to control environmental properties within the process chamber;
  - a control system to control rate of etching of the semiconductor wafer by adjusting the one or more environmental properties via the one or more actuators;
  - a light source to illuminate one or both sides of the semiconductor wafer; and
  - a rinsing station to remove the etchant.
2. The apparatus as recited in claim 1, wherein environmental properties include temperature, vapor pressure, electric field, etchant concentration, etchant composition and illumination.
3. The apparatus as recited in claim 1, wherein the rinsing station is the same as the process chamber.
4. The apparatus as recited in claim 1, further comprising a plurality of sensors to detect the etch state.
5. The apparatus as recited in claim 4, wherein the etch state comprises one or more of the following: an etch depth, a material porosity, number of alternating layers etched, electrical conductivity of doped semiconducting material in contact with an etchant, optical properties of features, and electrical properties of features measured during and/or after the etching process.
6. The apparatus in claim 1, further comprising a send ahead wafer that is processed through the equipment and an offline metrology system to sense etch state of the send ahead wafer.

7. The apparatus of claim 6, wherein the offline metrology estimates process excursions noticed in the send ahead wafer.
8. The apparatus in claim 1, wherein the process chamber comprises a sapphire window on one or both sides of the semiconductor wafer.
9. The apparatus in claim 1, wherein the process chamber comprises one or more optic fiber cables on one or both sides of the semiconductor wafer.
10. The apparatus in claim 2, wherein the sapphire window transmits illumination from a light source to the back of the substrate to create an ohmic contact.
11. The apparatus in claim 1, wherein the process chamber comprises an electrode on one or both sides of the semiconductor wafer.
12. The apparatus in claim 11, wherein the electrodes are designed to allow transmission of light to the one or both sides of the semiconductor wafer.
13. The apparatus in claim 1, wherein the light source is a lamp with tunable wavelength and intensity.
14. The apparatus in claim 1, wherein the electrolyte on the back of the electrode comprises one or more of the following: hydrogen peroxide, PVA, PLA, sulphuric acid, ammonium sulphate, or water.
15. The apparatus in claim 5, wherein the etch state is determined in-situ using optical metrology on the front and on the back of the wafer.
16. The apparatus in claim 15, wherein the images acquired using visible wavelengths on the front of the wafer and IR wavelengths on the back of the wafer can be used to create 3D images of the etch front at any stage of the etch process.
17. The apparatus in claim 16, wherein the images are taken as snapshots at regular time intervals, with the times intervals ranging from 1ms to 1 minute.
18. A method for improving reliability of catalyst influenced chemical etching, the method comprising:

providing a semiconducting material;

patterning a catalyst layer on a surface of the semiconducting material, wherein the pattern comprising one or more lithographic links; and

exposing the patterned layer to an etchant such that the lithographic links in the patterned catalyst layer enhance etchant diffusion during etch of high aspect ratio structures.

19. The method as recited in claim 18, wherein the material is one of the following:

single crystal bulk silicon wafer, a layer of polysilicon of thickness greater than 100nm deposited on a substrate, a layer of amorphous silicon of thickness greater than 100nm deposited on a substrate, an SOI (silicon on insulator) wafer, or a layer of epitaxial silicon of thickness greater than 100nm on a substrate.

20. The method as recited in claim 18, wherein the material comprises alternating layers of semiconductor materials of varying doping levels and dopants, highly doped silicon and lightly doped silicon, undoped silicon and doped silicon or germanium, Silicon and  $\text{Si}_x\text{Ge}_{1-x}$ , differently doped silicon and/or  $\text{Si}_x\text{Ge}_{1-x}$ , differently doped silicon and/or Ge, or Si and Ge.

21. The method as recited in claim 18, wherein the etchant comprises at least two of the following:

fluoride species containing chemicals HF or  $\text{NH}_4\text{F}$ ;

oxidants  $\text{H}_2\text{O}_2$ ,  $\text{KMnO}_4$ , or dissolved oxygen;

alcohols ethanol, isopropyl alcohol, or ethylene glycol; or

protic, aprotic, polar and non-polar solvents including DI water, or dimethyl sulfoxide (DMSO).

22. The method of claim 18, wherein the semiconducting material can be Ge, GaAs, GaN, Si, SiC, SiGe, InGaAs, and other Group IV, III-V, II-V elements or compounds.

23. The method of claim 18, wherein the catalyst layer comprises one or more of the following: Au, Pt, Pd, Ru, Ag, Cu, Ni, W, TiN, TaN,  $\text{RuO}_2$ ,  $\text{IrO}_2$ , or Graphene.