POLISHING APPARATUS AND METHOD FOR FORMING AN INTEGRATED CIRCUIT

Abstract of the Disclosure

In one embodiment, a dielectric layer (144, 156) overlying a semiconductor substrate (28) is uniformly polished. During polishing, the perimeter (32) of the semiconductor substrate (28) overlies a peripheral region (16, 48, 66, 86, 120) of a polishing pad (6, 42, 60, 80, 100) and an edge portion (36) of the front surface of semiconductor substrate (28) is not in contact with the front surface (18, 50, 68, 88, 122) of the polishing pad (6, 42, 60, 80, 100), in the peripheral region (16, 48, 66, 86, 120). As a result, the polishing rate at the edge portion (36) of the semiconductor substrate (28) is reduced, and the semiconductor substrate (28) is polished with improved center to edge uniformity. Since the semiconductor substrate (28) is polished with improved center to edge uniformity, die yield is increased because die located within the edge portion (36) of the semiconductor substrate (28) are not over polished.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)