PACKAGING MODULE AND ELECTRONIC DEVICE

ABSTRACT

This application provides a packaging module and an electronic device. The packaging module includes a substrate layer disposed in a stacking manner, and a plurality of chip layers stacked on the substrate layer. The substrate layer serves as a supporting structure to support the plurality of chip layers. The plurality of chip layers include a top chip layer, and the top chip layer is a chip layer furthest from the substrate layer in the plurality of chip layers. The top chip layer includes a first chip, a connection surface of the first chip faces the substrate layer, and the connection surface of the first chip is conductively connected to a chip of an adjacent chip layer by using a first conductor. In the foregoing technical solution, all chips are supported by one substrate (the substrate layer), to reduce a quantity of used substrates, and further reduce a thickness of the packaging module. In addition, the connection surface of the first chip faces the substrate layer, so that the first conductor connected to the first chip and another chip does not occupy additional space, to reduce the thickness of the packaging module, and facilitate miniaturization of the packaging module.

Fig. 3