Claims

What is claimed:

1. A method of making a semiconductor device, comprising:

providing a semiconductor die including a first conductive layer formed on a surface of the semiconductor die;

forming a first insulating layer over the surface of the semiconductor die;

depositing an encapsulant over the semiconductor die with a surface of the encapsulant coplanar with the surface of the semiconductor die;

forming a second insulating layer over the surface of the encapsulant and over the first insulating layer and extending to contact the first conductive layer;

forming an interconnect site outside a footprint of the semiconductor die by removing a portion of the second insulating layer within the interconnect site over the encapsulant to form an opening extending to the surface of the encapsulant while leaving a portion of the second insulating layer in an interior region of the interconnect site; and

forming a second conductive layer over the interconnect site to contact the portion of the second insulating layer and extending into the opening to contact the surface of the encapsulant.

2. The method of claim 1, further including forming a bump over the second conductive layer.

3. The method of claim 1, wherein the opening includes a ring shape around the portion of the second insulating layer in the interior region of the interconnect site.

4. The method of claim 1, wherein the opening includes a plurality of vias disposed around a perimeter of the interconnect site.

5. The method of claim 1, further including forming a third conductive layer over the interconnect site.

6. The method of claim 1, further including forming a third insulating layer over the second insulating layer.

7. A method of making a semiconductor device, comprising:

providing a semiconductor die;

depositing an encapsulant over the semiconductor die with a surface of the encapsulant coplanar with a surface of the semiconductor die;

forming a first insulating layer over the surface of the encapsulant;

forming an interconnect site outside a footprint of the semiconductor die by removing a portion of the first insulating layer within the interconnect site over the encapsulant to form an opening extending to the surface of the encapsulant while leaving a portion of the first insulating layer in an interior region of the interconnect site; and

forming a first conductive layer over the interconnect site to contact the portion of the first insulating layer and extending into the opening to contact the surface of the encapsulant.

8. The method of claim 7, further including forming an interconnect structure over the first conductive layer.

9. The method of claim 8, wherein the interconnect structure includes a bump.

10. The method of claim 7, wherein the opening includes a ring shape around the portion of the second insulating layer in the interior region of the interconnect site.

11. The method of claim 7, wherein the opening includes a plurality of vias disposed around a perimeter of the interconnect site.

12. The method of claim 7, further including forming a second insulating layer over the surface of the semiconductor die, wherein the first insulating layer extends over the second insulating layer to contact a second conductive layer on the semiconductor die.

13. The method of claim 7, further including forming a second insulating layer over the interconnect site.

14. A method of making a semiconductor device, comprising:

providing a semiconductor die;

depositing an encapsulant over the semiconductor die;

forming a first insulating layer over a surface of the encapsulant;

forming an interconnect site outside a footprint of the semiconductor die by removing a portion of the first insulating layer within the interconnect site over the encapsulant to form

an opening extending to the surface of the encapsulant while leaving a portion of the first insulating layer in an interior region of the interconnect site; and

forming a first conductive layer over the interconnect site to contact the portion of the first insulating layer and extending into the opening to contact the surface of the encapsulant.

15. The method of claim 14, further including forming an interconnect structure over the first conductive layer.

16. The method of claim 14, wherein the opening includes a ring shape around the portion of the second insulating layer in the interior region of the interconnect site.

17. The method of claim 14, wherein the opening includes a plurality of vias disposed around a perimeter of the interconnect site.

18. The method of claim 14, further including forming a second conductive layer over the interconnect site.

19. The method of claim 14, further including forming a second insulating layer over the semiconductor die, wherein the first insulating layer extends over the second insulating layer to contact a second conductive layer on the semiconductor die.

20. A semiconductor device, comprising:

a semiconductor die;

an encapsulant deposited over the semiconductor die;

a first insulating layer formed over a surface of the encapsulant;

an interconnect site located outside a footprint of the semiconductor die, wherein the interconnect structures includes an opening in the first insulating layer and a portion of the first insulating layer in an interior region of the interconnect site;

a first conductive layer formed over the interconnect site to contact the portion of the first insulating layer and extending into the opening to contact the surface of the encapsulant; and

forming a second insulating layer over the surface of the semiconductor die, wherein the first insulating layer extends over the second insulating layer to contact a second conductive layer on the semiconductor die.

21. The semiconductor device of claim 20, further including forming an interconnect structure over the first conductive layer.

22. The semiconductor device of claim 20, wherein the opening includes a ring shape around the portion of the second insulating layer in the interior region of the interconnect site.

23. The semiconductor device of claim 20, wherein the opening includes a plurality of vias disposed around a perimeter of the interconnect site.

24. The semiconductor device of claim 20, further including a second conductive layer formed over the interconnect site.