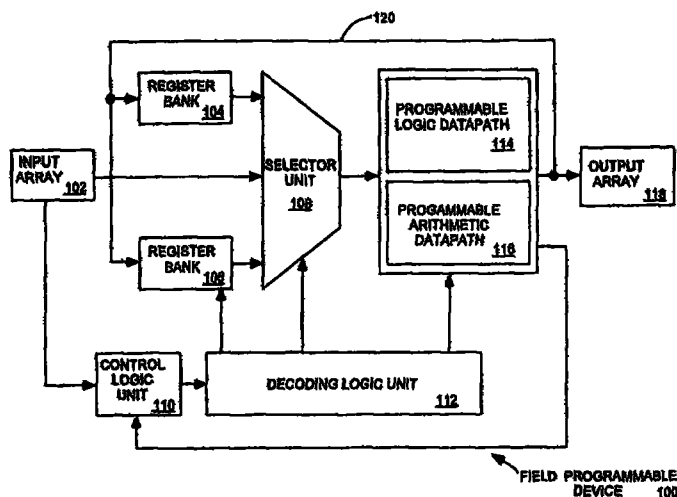




INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification ⁶: G06F 9/06, 9/22, 9/28	A1	(11) International Publication Number: WO 98/57252 (43) International Publication Date: 17 December 1998 (17.12.98)
(21) International Application Number: PCT/US98/11889 (22) International Filing Date: 9 June 1998 (09.06.98) (30) Priority Data: 08/874,817 13 June 1997 (13.06.97) US (71) Applicant (for all designated States except US): MALLEABLE MICROSYSTEMS, INC. [US/US]; 2131 Camino a los Cerros, Menlo Park, CA 94025 (US). (72) Inventor; and (75) Inventor/Applicant (for US only): ABBOTT, Curtis [US/US]; 2131 Camino a los Cerros, Menlo Park, CA 94025 (US). (74) Agents: DE VOS, Daniel, M. et al.; Blakely, Sokoloff, Taylor & Zafman LLP, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025 (US).		(81) Designated States: AL, AM, AT, AT (Utility model), AU (Petty patent), AZ, BA, BB, BG, BR, BY, CA, CH, CN, CU, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, GH, GM, GW, HU, ID, IL, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), SL, TJ, TM, TR, TT, UA, UG, US, UZ, VN, YU, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG). Published <i>With international search report.</i> <i>Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.</i>

(54) Title: PROGRAMMABLE LOGIC DATAPATH THAT MAY BE USED IN A FIELD PROGRAMMABLE DEVICE

**(57) Abstract**

A method and apparatus for providing a programmable logic datapath (114) that may be used in a field programmable device (100). According to one aspect of the invention, a programmable logic datapath (114) is provided that includes a plurality of logic elements to perform various (Boolean) logic operations. The programmable logic datapath (114) further includes circuitry to selectively route and select operand bits between the plurality of logic elements (operand bits is used hereinafter to refer to input bits, logic operation result bits, etc., that may be generated within the logic datapath (114)). In one embodiment, by providing control bits concurrently with operand bits to routing and selection (e.g., multiplexing) circuitry, the programmable logic datapath (114) of the invention can provide dynamic programmability to perform a number of logic operations on inputs of various lengths on a cycle-by-cycle basis.