

**ABSTRACT OF THE DISCLOSURE**  
**METHOD FOR FORMING A POLYCIDAL GATE ELECTRODE**

A method for forming within a Field Effect Transistor (FET) for use within an integrated circuit a polycide gate electrode. There is first provided a semiconductor substrate. Formed upon the semiconductor is a patterned polysilicon layer. Formed then upon the semiconductor substrate and the patterned polysilicon layer is a blanket insulator layer. The blanket insulator layer is then patterned through planarizing to form a patterned planarized insulator layer while simultaneously exposing the surface of the patterned polysilicon layer. Finally, there is formed upon the exposed surface of the patterned polysilicon layer a patterned metal silicide layer. The patterned metal silicide layer and the patterned polysilicon layer form a polycide gate electrode. The metal silicide layer within the polycide gate electrode is not susceptible to encroachment upon adjoining insulator spacers or source/drain regions within the Field Effect Transistor (FET) within which is formed the polycide gate electrode.

(FIGURE 1 IS SUGGESTED FOR PUBLICATION)