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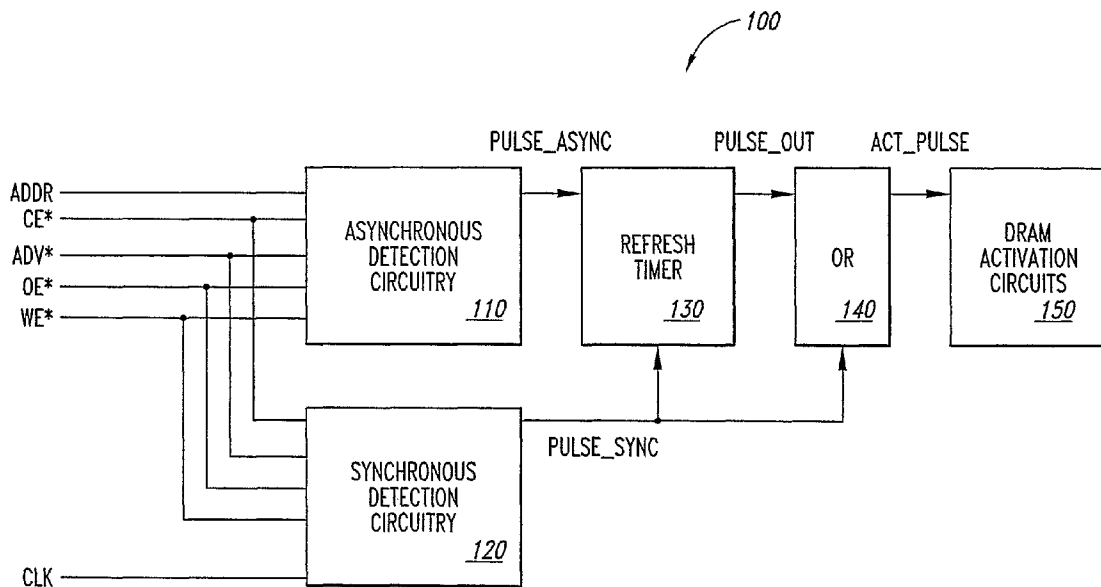
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(54) Title: DETECTION CIRCUIT FOR MIXED ASYNCHRONOUS AND SYNCHRONOUS MEMORY OPERATION



(57) Abstract: A memory access mode detection circuit and method for detecting and initiating memory access modes for a memory device. The memory access mode detection circuit receives the memory address signals, the control signals, and the clock signal and generates a first mode detection signal in response to receipt of the memory address signals or a first combination of control signals. A first mode initiation signal is generated a time delay subsequent to the detection signal to initiate the first mode memory access operation. In response to receipt of a second combination of control signals and an active clock signal, the memory access mode detection circuit further generates a second mode detection signal to initiate a second mode memory access operation and to suppress generation of the first mode detection signal, thereby canceling the first mode memory access operation.

WO 2004/070786 A2