A Method For Electrical Interconnection And An Interconnection Structure

FIELD OF INVENTION

The invention relates broadly to a method for electrical interconnection and an interconnection structure.

BACKGROUND

For micro/nano-devices and systems, performance of such micro/nano-devices and systems is increasingly related to interconnection and packaging due to decreasing bump sizes and pitches as well as increasing die sizes. In addition, heterogeneous integration of different technologies in a single chip is typically desirable. However, it will be appreciated that planar (two-dimensional) ICs are typically not suitable for such integration. It has been proposed that three-dimensional integrated circuits (3D ICs) and systems using short and vertical interlayer interconnections may significantly improve the performance of devices and reduce wire-limited chip areas. However, wiring or interconnection required for integrating or for packaging the micro/nano-devices and systems must typically scale at the same rate as the devices and systems in order to take advantage of improvements in size and speed.

Current interconnects are typically thin copper wires. At high current density, electromigration of copper atoms typically cause formation of voids and eventual separation of the interconnects. This typically leads to circuit failure of the semiconductor devices. Furthermore, electrical conductivity of copper interconnects at small scales typically degrades due to electron scattering at surfaces and grain boundaries. In addition, another problem may arise due to oxidation of metal at small scales.

In attempting to solve the above problems, the flip chip technique has been explored. The flip chip technique may provide advantages over typical interconnect techniques. These advantages include having the lowest inductance per lead, the highest frequency response speed as well as the lowest cross talk and simultaneous switching noise. However, using the interconnection method of flip chip in the integration and packaging industry, the issue of size becomes increasingly critical for interconnection and pitches. It has been recognised that as the interconnection dimensions and pitch sizes are reduced to very fine scales, the current flip chip interconnection material and technique are typically unable to meet design requirements.

Current flip chip interconnection material for electrical contacts are typically metal or metal-based solders. Following the reduction in size of interconnects, bumps and pitches, e.g. for nanodevices and nanosystems, using metal solder or metal-based solder are typically unreliable.

Thus, a need exists for a method for electrical interconnection and an interconnection structure to address at least one of the above problems.

SUMMARY

In accordance with a first aspect of the present invention, there is provided a a method for electrical interconnection, the method comprising, providing a first substantially vertical nano structure on a first substrate; strengthening the first nano structure; and forming a solder free electrical contact between the first nano structure and an electrical circuit of a second substrate.

The forming the solder free electrical contact may comprise the steps of forming a second substantially vertical nano structure on the second substrate; and engaging the first and second nano structures.

The engaging the first and second nano structures may comprise physically contacting the first and second nano structures.

The engaging the first and second nano structures may comprise inserting the first nano structure into the second nano structure.

The engaging the first and second nano structures may comprise inserting the first nano structure to contact a base of the second nano structure.

The forming the first and second nano structures may comprise the steps of depositing respective catalyst layers on the first and second substrates; performing patterning and lithography on the respective catalyst layers; and growing the first and second nano structures on the respective patterned catalyst layers.

The method may further comprise the step of metallizing the first and second nano structures.

The forming the solder free electrical contact may comprise the steps of strengthening the first nano structure; forming a contact pad on the second substrate; and forming the electrical contact between the strengthened first nano structure to the contact pad of the second substrate.

The forming the electrical contact to the contact pad of the second substrate may comprise thermal compression, thermosonic bonding, or both.

The step of strengthening the first nano structure may comprise forming a template for providing the first nano structure therein wherein the template is formed by depositing a layer of template material and performing patterning and lithography on the layer of template material.

The step of strengthening the first nano structure may comprise encapsulating the first nano structure using a polymer material and exposing a

contact surface of the encapsulated first nano structure prior to forming the electrical contact to the contact pad of the second substrate.

The method may further comprise depositing an intermediate electrically conducting layer on the first nano structure prior to forming the electrical contact.

The step of strengthening the first nano structure may comprise providing an electrically conducting stabiliser layer on the first nano structure.

The forming the first nano structure may comprise the steps of depositing a catalyst layer on the first substrate; performing patterning and lithography on the catalyst layer; and growing the first nano structure on the patterned catalyst layer.

The method may further comprise filling a gap between the first and second substrates using an electrically insolating material.

The electrically insolating material may be selected from a group consisting of polymeric underfill, polymer composite and adhesive.

In accordance with a second aspect of the present invention, there is provided an interconnection structure comprising: a strengthened first substantially vertical nano structure of a first substrate; and a solder free electrical contact between the first nano structure and an electrical circuit of the second substrate.

The solder free electrical contact may comprise a second substantially vertical nano structure of the second substrate in engagement with the first nano structure.

The first nano structure may be in physical contact with the second nano structure.

The first nano structure may be inserted into the second nano structure.

The first nano structure may be inserted into the second nano structure such that the first nano structure contacts a base of the second nano structure.

The interconnection structure may further comprise a first patterned catalyst layer between the first nano structure and the first substrate and a second patterned catalyst layer between the second nano structure and the second substrate.

The first nano structure and the second nano structure may be metallized.

The interconnection structure may comprise a strengthened first nano structure; a contact pad on the second substrate; and wherein the electrical contact is formed between the strengthened first nano structure and the contact pad of the second substrate.

The interconnection structure may comprise a template formed around the first nano structure.

The interconnection structure may comprise a polymer material encapsulating the first nano structure.

The interconnection structure may comprise an intermediate electrically conducting layer on the first nano structure.

The interconnection structure may comprise an electrically conducting stabiliser layer on the first nano structure.

The interconnection structure may further comprise a patterned catalyst layer between the first nano structure and the first substrate.

The interconnection structure may further comprise an electrically insolating material filling between the first and second substrates.

The electrically insolating material filling may be selected from a group consisting of polymeric underfill, polymer composite and adhesive.

BRIEF DESCRIPTION OF THE DRAWINGS

Embodiments of the invention will be better understood and readily apparent to one of ordinary skill in the art from the following written description, by way of example only, and in conjunction with the drawings, in which:

Figure 1(a) is a schematic diagram illustrating deposition of a catalyst layer on a first substrate.

Figure 1(b) is a schematic diagram illustrating lithography and patterning carried out on the catalyst layer of the first substrate.

Figure 1(c) is a schematic diagram illustrating growing of high density carbon nanotubes on the patterned catalyst layer of the first substrate.

Figure 1(d) is a schematic diagram illustrating deposition of a catalyst layer on a second substrate.

Figure 1(e) is a schematic diagram illustrating lithography and patterning carried out on the catalyst layer of the second substrate.

Figure 1(f) is a schematic diagram illustrating growing of high density carbon nanotubes on the patterned catalyst layer of the second substrate.

Figure 1(g)(1) is a schematic diagram illustrating contacting the respective carbon nanotubes of the first substrate and the second substrate using flip chip technique.

Figure 1(g)(2) is a schematic diagram illustrating inserting the carbon nanotubes of the first substrate into the carbon nanotubes of the second substrate using flip chip technique.

Figure 1(g)(3) is a schematic diagram illustrating inserting the carbon nanotubes of the first substrate into the carbon nanotubes of the second substrate using flip chip technique until the carbon nanotubes of the first substrate contact the patterned catalyst layer of the second substrate.

Figure 1(h) is a schematic diagram illustrating filling the gap between the contacted first and second substrates using a polymer.

Figure 2(a) is a schematic diagram illustrating deposition of a catalyst layer on a first substrate.

Figure 2(b) is a schematic diagram illustrating lithography and patterning carried out on the catalyst layer of the first substrate.

Figure 2(c) is a schematic diagram illustrating growing of high density carbon nanotubes on the patterned catalyst layer of the first substrate.

Figure 2(d) is a schematic diagram illustrating metallization of the high density carbon nanotubes of the first substrate.

Figure 2(e) is a schematic diagram illustrating deposition of a catalyst layer on a second substrate.

Figure 2(f) is a schematic diagram illustrating lithography and patterning carried out on the catalyst layer of the second substrate.

Figure 2(g) is a schematic diagram illustrating growing of high density carbon nanotubes on the patterned catalyst layer of the second substrate.

Figure 2(h) is a schematic diagram illustrating metallization of the high density carbon nanotubes of the second substrate.

Figure 2(i)(1) is a schematic diagram illustrating contacting the respective metallized carbon nanotubes of the first substrate and the second substrate using flip chip technique.

Figure 2(i)(2) is a schematic diagram illustrating inserting the metallized carbon nanotubes of the first substrate into the metallized carbon nanotubes of the second substrate using flip chip technique.

Figure 2(i)(3) is a schematic diagram illustrating inserting the metallized carbon nanotubes of the first substrate into the metallized carbon nanotubes of the second substrate using flip chip technique until the metallized carbon nanotubes of the first substrate contact the patterned catalyst layer of the second substrate.

Figure 2(j) is a schematic diagram illustrating filling the gap between the contacted first and second substrates using a polymer.

Figure 3(a) is a schematic diagram illustrating deposition of a catalyst layer and a template layer on a first substrate.

Figure 3(b) is a schematic diagram illustrating lithography and patterning carried out on the catalyst layer and the template layer of the first substrate.

Figure 3(c) is a schematic diagram illustrating formation of nanopores in the patterned template layer of the first substrate.

Figure 3(d) is a schematic diagram illustrating growing of carbon nanotubes in the nanopores.

Figure 3(e) is a schematic diagram illustrating deposition and patterning of a bonding metal layer on the carbon nanotubes in the nanopores.

Figure 3(f) is a schematic diagram illustrating a second substrate comprising metal contact pads.

Figure 3(g) is a schematic diagram illustrating bonding of the patterned bonding metal layer of the first substrate with the metal contact pads of the second substrate.

Figure 3(h) is a schematic diagram illustrating filling the gap between the contacted first and second substrates using a polymer.

Figure 4(a) is a schematic diagram illustrating deposition of a catalyst layer on a first substrate.

Figure 4(b) is a schematic diagram illustrating lithography and patterning carried out on the catalyst layer of the first substrate.

Figure 4(c) is a schematic diagram illustrating growing of high density carbon nanotubes on the patterned catalyst layer of the first substrate.

Figure 4(d) is a schematic diagram illustrating encapsulation of the carbon nanotubes of the first substrate.

Figure 4(e) is a schematic diagram illustrating exposing a surface of the encapsulated carbon nanotubes.

Figure 4(f) is a schematic diagram illustrating deposition and patterning of a bonding metal layer on the exposed carbon nanotubes.

Figure 4(g) is a schematic diagram illustrating a second substrate comprising metal contact pads.

Figure 4(h) is a schematic diagram illustrating bonding of the patterned bonding metal layer of the first substrate with the metal contact pads of the second substrate.

Figure 4(i) is a schematic diagram illustrating filling the gap between the contacted first and second substrates using a polymer.

Figure 5(a) is a schematic diagram illustrating deposition of a catalyst layer on a first substrate.

Figure 5(b) is a schematic diagram illustrating patterning of the catalyst layer of the first substrate.

Figure 5(c) is a schematic diagram illustrating growing of high density carbon nanotubes on the patterned catalyst layer of the first substrate.

Figure 5(d) is a schematic diagram illustrating formation of a bonding metal layer on the carbon nanotubes of the first substrate.

Figure 5(e) is a schematic diagram illustrating a second substrate comprising metal contact pads.

Figure 5(f) is a schematic diagram illustrating bonding of the patterned bonding metal layer of the first substrate with the metal contact pads of the second substrate.

Figure 5(g) is a schematic diagram illustrating filling the gap between the contacted first and second substrates using a polymer.

Figure 6 is a schematic flowchart illustrating a method for interconnection for semiconductor devices.

DETAILED DESCRIPTION

Example embodiments described provide a method for integrating and packaging high density devices and systems using carbon nanotubes. In the example

embodiments, a first substrate and a second substrate are aligned and electrically contacted using carbon nanotubes on one or both of the substrates. The alignment and contacting of the substrates are based on flip chip technique. The electrical contact between the first substrate and the second substrate is solder free in the example embodiments.

Figures 1(a) to (h) are schematic diagrams illustrating a process flow in a first example embodiment. Figure 1(a) illustrates a catalyst layer 102 deposited on a first substrate 104. The first substrate 104 comprises a circuit layer 106 and a dielectric/passivation layer 108. Figure 1(b) illustrates lithography and patterning carried out on the catalyst layer 102 of the first substrate 104. Figure 1(c) illustrates growing of high density carbon nanotubes e.g. 110 on the patterned catalyst layer 102 of the first substrate 104. Figure 1(d) illustrates a catalyst layer 112 deposited on a second substrate 114. The second substrate 114 comprises a circuit layer 116 and a dielectric/passivation layer 118. Figure 1(e) illustrates lithography and patterning carried out on the catalyst layer 112 of the second substrate 114. Figure 1(f) illustrates growing of high density carbon nanotubes e.g. 120 on the patterned catalyst layer 112 of the second substrate 114.

In this example embodiment, the first substrate 104 and the second substrate 114 are aligned and brought into electrical contact with each other using the respective carbon nanotubes e.g. 110 and e.g. 120. Figure 1(g)(1) illustrates a first method of making electrical contact. In this first method, the first substrate 104 and the second substrate 114 are brought into electrical contact using flip chip technique and by contacting the respective carbon nanotubes e.g. 110 and e.g. 120. Figure 1(g)(2) illustrates a second method of making electrical contact. In this second method, the first substrate 104 and the second substrate 114 are brought into electrical contact using flip chip technique and by inserting the carbon nanotubes e.g. 110 of the first substrate 104 into the carbon nanotubes e.g. 120 of the second substrate 114. Figure 1(g)(3) illustrates a third method of making electrical contact. In this third method, the first substrate 104 and the second substrate 114 are brought into electrical contact using flip chip technique and by inserting the carbon nanotubes e.g. 110 of the first substrate 104 into the carbon nanotubes e.g. 120 of the second substrate 114 such that the carbon nanotubes e.g.

110 of the first substrate 104 contact the patterned catalyst layer 112 of the second substrate 114.

Figure 1(h) illustrates filling the gap between the electrically contacted first substrate 104 and the second substrate 114 with a polymer 122.

In the described first example embodiment, the carbon nanotubes e.g. 110 and e.g. 120 are directly grown on the patterned catalyst pads on the first substrate 104 and the second substrate 114 using the deposition methods described above. The carbon nanotubes bundles e.g. 110 and e.g. 120 on the first substrate 104 and the second substrate 114 respectively are aligned and brought into contact using flip chip interconnection technique. As described using Figures 1(g)(1) to 1(g)(3), the aligned carbon nanotubes bundles e.g. 110 and e.g. 120 may remain in minimal contact, partially insert into each other or insert fully until one carbon nanotubes bundle e.g. 110 reaches the base of the other carbon nanotubes bundle e.g. 120 (ie. contacting the catalyst layer 112 of the second substrate). The gap between the first substrate 104 and the second substrate 114 is filled with polymer 122, such as underfill, and is then subjected to a curing process of the polymer 122. After curing, a compression stress is formed in the resulting package that compresses the carbon nanotubes bundles e.g. 110 and e.g. 120 together. Therefore, the electrical conductivity of the carbon nanotubes bundles e.g. 110 and e.g. 120 may advantageously be utilised in this example embodiment.

In this example embodiment, the catalyst metal pads formed by the patterned catalyst layers 102 and 112 comprise material such as Ni, Co, Fe, or alloys and composites containing one or more of these elements. The catalyst metal pads may be directly deposited and formed on single metal layer pads such as Cu and Al pads. Alternatively, a barrier or adhesion layer comprising single or multiple metallic layers may be deposited on Cu or Al material, followed by the deposition of the catalyst layer. The barrier or adhesion layer materials may comprise Au, Ti, W, Cr, Zr, V, Nb, Pb, Pt, Ta, Mo, Pd, and alloys of at least two metal elements. In the example embodiment, the thickness of the catalyst layers 102 and 112 is about 2 nm to 2 μm each. The catalyst layer and barrier or adhesion layer deposition methods can include physical vapour

deposition techniques such as sputtering, evaporation, laser ablation, and chemical vapour deposition techniques, flame fusion spraying as well as electroplating and electroless plating. Preferably, but not limiting to, physical vapour deposition techniques are employed due to the low deposition temperature and well controllable thin layer thickness. The deposition can be performed at room temperature. Patterning methods include, but are not limited to, optical lithography, extreme-ultraviolet (EUV) lithography, X-ray lithography, e-beam lithography, focus ion beam lithography, mechanical lithography, physical lithography and chemical lithography. The pad sizes may range from about 10 nm to about 100 μm.

In a second example embodiment, carbon nanotubes are metallized before being aligned and brought into contact. For the metallization, a metallic film of several nanometers thickness is deposited on the respective carbon nanotubes contact surfaces. After metallization of the carbon nanotubes, the two substrates are packaged using the approach described above.

Figures 2(a) to (j) are schematic diagrams illustrating a process flow in the second example embodiment. Figure 2(a) illustrates a catalyst layer 202 deposited on a first substrate 204. The first substrate 204 comprises a circuit layer 206 and a dielectric/passivation layer 208. Figure 2(b) illustrates lithography and patterning carried out on the catalyst layer 202 of the first substrate 204. Figure 2(c) illustrates growing of high density carbon nanotubes e.g. 210 on the patterned catalyst layer 202 of the first substrate 204. Figure 2(d) illustrates metallization of the carbon nanotubes e.g. 210 to form metallized carbon nanotubes e.g. 211. The metallization techniques can include physical vapour deposition techniques such as sputtering, evaporation, laser ablation, and chemical vapour deposition techniques, flame fusion spraying, sol-gel as well as electroplating and electroless plating. Preferably, physical vapour deposition, electroplating and electroless plating techniques are employed. Preferably, but not limiting to, Au, Cu and Ni are used as metallization material. The thickness of the metallization layer e.g. 211 is preferably about 1nm to 50 nm. Figure 2(e) illustrates a catalyst layer 212 deposited on a second substrate 214. The second substrate 214 comprises a circuit layer 216 and a dielectric/passivation layer 218. Figure 2(f) illustrates lithography and patterning carried out on the catalyst layer 212 of the second substrate

214. Figure 2(g) illustrates growing of high density carbon nanotubes e.g. 220 on the patterned catalyst layer 212 of the second substrate 214. Figure 2(h) illustrates metallization of the carbon nanotubes e.g. 220 to form metallized carbon nanotubes e.g. 222. The metallization techniques can be the same as described above with reference to metallization layer 211.

In this example embodiment, the first substrate 204 and the second substrate 214 are aligned and brought into electrical contact with each other using the respective metallized carbon nanotubes e.g. 211 and e.g. 222. Figure 2(i)(1) illustrates a first method of making electrical contact. In this first method, the first substrate 204 and the second substrate 214 are brought into electrical contact using flip chip technique and by contacting the respective metallized carbon nanotubes e.g. 211 and e.g. 222. Figure 2(i)(2) illustrates a second method of making electrical contact. In this second method, the first substrate 204 and the second substrate 214 are brought into electrical contact using flip chip technique and by inserting the metallized carbon nanotubes e.g. 211 of the first substrate 204 into the metallized carbon nanotubes e.g. 222 of the second substrate 214. Figure 2(i)(3) illustrates a third method of making electrical contact. In this third method, the first substrate 204 and the second substrate 214 are brought into electrical contact using flip chip technique and by inserting the metallized carbon nanotubes e.g. 211 of the first substrate 204 into the metallized carbon nanotubes e.g. 222 of the second substrate 214 such that the metallized carbon nanotubes e.g. 211 of the first substrate 204 contact the patterned catalyst layer 212 of the second substrate 214.

Figure 2(j) illustrates filling the gap between the electrically contacted first substrate 204 and the second substrate 214 with a polymer 224.

In the described second example embodiment, the metallized carbon nanotubes e.g. 211 and e.g. 222 are directly grown and metallized on the patterned catalyst pads on the first substrate 204 and the second substrate 214 using the deposition methods described above. The metallized carbon nanotubes bundles e.g. 211 and e.g. 222 on the first substrate 204 and the second substrate 214 respectively are aligned and brought into contact using flip chip interconnection technique. As described using Figures 2(i)(1)

to 2(i)(3), the aligned metallized carbon nanotubes bundles e.g. 211 and e.g. 222 may remain in minimal contact, partially insert into each other or insert fully until one metallized carbon nanotubes bundle e.g. 211 reaches the base of the other metallized carbon nanotubes bundle e.g. 222 (ie. contacting the catalyst layer 212 of the second substrate). The gap between the first substrate 204 and the second substrate 214 is filled with polymer 224, such as underfill, and is then subjected to a curing process of the polymer 224. After curing, a compression stress is formed in the resulting package that compresses the metallized carbon nanotubes bundles e.g. 211 and e.g. 222 together. Therefore, the electrical conductivity of the metallized carbon nanotubes bundles e.g. 211 and e.g. 222 may advantageously be utilised in this example embodiment.

In this example embodiment, the catalyst metal pads formed by the patterned catalyst layers 202 and 212 comprise material such as Ni, Co, Fe, or alloys and composites containing one or more of these elements. The catalyst metal pads may be directly deposited and formed on single metal layer pads such as Cu and Al pads. Alternatively, a barrier or adhesion layer comprising single or multiple metallic layers may be deposited on Cu or Al material, followed by the deposition of the catalyst layer. The barrier or adhesion layer materials may comprise Au, Ti, W, Cr, Zr, V, Nb, Pb, Pt, Ta, Mo, Pd, and alloys of at least two metal elements. In the example embodiment, the thickness of the catalyst layers 202 and 212 is about 2 nm to 2 μm each. The catalyst layer and barrier or adhesion layer deposition methods can include physical vapour deposition techniques such as sputtering, evaporation, laser ablation, and chemical vapour deposition techniques, flame fusion spraying as well as electroplating and electroless plating. Preferably, but not limiting to, physical vapour deposition techniques are employed due to the low deposition temperature and well controllable thin layer thickness. The deposition can be performed at room temperature. Patterning methods include, but are not limited to, optical lithography, extreme-ultraviolet (EUV) lithography, X-ray lithography, e-beam lithography, focus ion beam lithography, mechanical lithography, physical lithography and chemical lithography. The pad sizes may range from about 10 nm to about 100 μm.

Figures 3(a) to (h) are schematic diagrams illustrating a process flow in a third example embodiment. Figure 3(a) illustrates a catalyst layer 302 and a template layer

304 deposited on a first substrate 306. The first substrate 306 comprises a circuit layer 308 and a dielectric/passivation layer 310. Figure 3(b) illustrates lithography and patterning carried out on the catalyst layer 302 and the template layer 304 of the first substrate 306. Figure 3(c) illustrates forming nanopores e.g. 312 in the patterned template layer 304. The porous patterned template layer 314 may comprise alumina, alumina-based material, silica, silica-based material, titania, titania-based material, co-polymer material and/or at least two of the above material.

For alumina and alumina-based material template formation, one layer of aluminium is deposited first, followed by anodising of the aluminium layer and plasma cleaning or etching to thoroughly open the nanopores e.g. 312 until the nanopores e.g. 312 reach the patterned catalyst layer 302. For silica, silica-based material, titania and titania-based material templates, a sol gel process is used to obtain the nanopores e.g. 312. For silica, silica-based material, titania, titania-based material and co-polymer material templates, the nanopores e.g. 312 are obtained by removing one phase.

Figure 3(d) illustrates growing of carbon nanotubes e.g. 316 in the nanopores e.g. 312. Figure 3(e) illustrates deposition and patterning of a bonding metal layer 318 on the top surface of the carbon nanotubes e.g. 316 and the porous patterned template layer 314. Figure 3(f) illustrates a second substrate 320 comprising a dielectric/passivation layer 322, a circuit layer 324 and metal pads e.g. 326. Figure 3(g) illustrates bonding of the patterned bonding metal layer 318 of the first substrate 306 to the metal pads e.g. 326 of the second substrate 320. The bonding may be carried out using bonding techniques such as, but not limited to, thermal compression or thermosonic bonding techniques. Figure 3(h) illustrates filling the gap between the first substrate 306 and the second substrate 320 with a polymer 328.

In the described third example embodiment, an ordered nano-porous template layer 314 of e.g. alumina, silica or polymer is synthesized on the catalyst pads of the patterned catalyst layer 302. The thickness of the porous patterned template layer 314 may range from about 100 nm to about 100 μm. Once the through nanopores e.g. 312 with one end terminating on the catalyst pads of the patterned catalyst layer 302 are formed, the carbon nanotubes e.g. 316 are grown in the nanopores e.g. 312 using

techniques such as arc-discharge, pyrolysis of hydrocarbons, chemical vapor deposition, laser vaporization of graphite targets, solar carbon vaporization and electrolysis of carbon electrodes in molten ionic salts etc. The size of the nanopores e.g. 312 may range from about 2 nm to about 50 nm. In this example embodiment, the patterned template layer 314 is used for the growth of the aligned carbon nanotubes e.g. 316 and also used for enhancing the strength and rigidity of carbon nanotubes e.g. 316 as a whole together with the template 314. The patterned template layer 314 together with the carbon nanotubes e.g. 316 is used as an interconnecting bump that is robust enough for the bonding process. Prior to bonding, the bump top surface is coated with a bonding metal layer (see Figure 3(e)). The bonding metal layer may comprise material such as, but not limited to, the transition metals, Ni, Co, Cu, Au, Ti, W, Cr, Zn, Sn, Zr, Al, Mg, V, Nb, Pb, Ag, Pt, Ta, Mo, Pd, Ru, Cd, In, Ge, Bi and alloys of at least two metal elements. The coating may be carried out using methods such as, but not limited to, physical vapour deposition, sputtering, vapor evaporating, electroplating, electroless plating, chemical vapor deposition, flame fusion spraying and sol gel coating.

In this example embodiment, the bonding metal layer 318 may include a single layer metal or a multilayer metal. The metal pads e.g. 326 are deposited on the second substrate 320 using methods such as, but not limited to, physical vapour deposition, sputtering, vapor evaporating, electroplating, electroless plating, chemical vapor deposition, flame fusion spraying and sol gel coating. The bonding (see Figure 3(g)) may be thermocompression bonding in solid state at elevated temperatures under pressure or may be thermosonic bonding in solid state at elevated temperatures under pressure and ultrasonic power. It is preferable that the bonding is subjected to further annealing to strengthen the bonds.

In this example embodiment, the catalyst metal pads formed by the patterned catalyst layer 302 comprise material such as Ni, Co, Fe, or alloys and composites containing one or more of these elements. The catalyst metal pads may be directly deposited and formed on single metal layer pads such as Cu and Al pads. Alternatively, a barrier or adhesion layer comprising single or multiple metallic layers may be deposited on Cu or Al material, followed by the deposition of the catalyst layer. The barrier or adhesion layer materials may comprise Au, Ti, W, Cr, Zr, V, Nb, Pb, Pt, Ta,

Mo, Pd, and alloys of at least two metal elements. In the example embodiment, the thickness of the catalyst layer 302 is about 2 nm to 2 μm. The catalyst layer 302 and barrier or adhesion layer deposition methods can include physical vapour deposition techniques such as sputtering, evaporation, laser ablation, and chemical vapour deposition techniques, flame fusion spraying as well as electroplating and electroless plating. Preferably, but not limiting to, physical vapour deposition techniques are employed due to the low deposition temperature and well controllable thin layer thickness. The deposition can be performed at room temperature. Patterning methods include, but are not limited to, optical lithography, extreme-ultraviolet (EUV) lithography, X-ray lithography, e-beam lithography, focus ion beam lithography, mechanical lithography, physical lithography and chemical lithography. The pad sizes may range from about 10 nm to about 100 μm.

Figures 4(a) to (i) are schematic diagrams illustrating a process flow in a fourth example embodiment. Figure 4(a) illustrates a catalyst layer 402 deposited on a first substrate 404. The first substrate 404 comprises a circuit layer 406 and a dielectric/passivation layer 408. Figure 4(b) illustrates lithography and patterning carried out on the catalyst layer 402 of the first substrate 404. Figure 4(c) illustrates growing of carbon nanotubes e.g. 410 on the patterned catalyst layer 402 of the first substrate 404. Figure 4(d) illustrates encapsulation of the carbon nanotubes e.g. 410 using a polymer 412. Figure 4(e) illustrates exposing a surface of the encapsulated carbon nanotubes e.g. 410. This may be achieved by grinding and polishing of the encapsulated carbon nanotubes e.g. 410 until the carbon nanotubes e.g. 410 are exposed (indicated at numeral 414). Figure 4(f) illustrates deposition and patterning of a bonding metal layer 416 on the top surface of the carbon nanotubes e.g. 410. Figure 4(g) illustrates a second substrate 418 comprising a dielectric/passivation layer 420, a circuit layer 422 and metal pads e.g. 424. Figure 4(h) illustrates bonding of the patterned bonding metal layer 416 of the first substrate 404 with the metal pads e.g. 424 of the second substrate 418. The bonding may be carried out using bonding techniques such as, but not limited to, thermal compression or thermosonic bonding techniques. Figure 4(i) illustrates filling the gap between the first substrate 402 and the second substrate 418 with the polymer 412.

In the described fourth example embodiment, the carbon nanotubes e.g. 410 are directly grown on the patterned catalyst pads of the catalyst layer 402 using the deposition methods described above, followed by encapsulation using the polymer 412. The polymer may be a polymeric underfill, a polymer composite or an adhesive. After the encapsulation, the polymer 412 is cured. The encapsulated surface is ground and polished until the carbon nanotubes e.g. 410 are exposed (see numeral 414). The individual bundles of exposed carbon nanotubes e.g. 410 are used as bumps and are fixed and mechanically enhanced by the polymer 412. Thus, the carbon nanotubes e.g. 410 in the example embodiment are robust enough for the bonding process.

In this example embodiment, the bonding metal layer 416 may comprise transition metals, Al, In, Ti, Sn, Pb and Bi and alloys of at least two metal elements. The bonding metal layer 416 may be deposited using methods such as, but not limited to, physical vapour deposition, sputtering, vapor evaporating, electroplating, electroless plating, chemical vapor deposition, flame fusion spraying and sol gel coating In this example embodiment, the bonding metal layer 416 may include a single layer metal or a multilayer metal. The metal pads e.g. 424 are deposited on the second substrate 418 using methods such as, but not limited to, physical vapour deposition, sputtering, vapor evaporating, electroplating, electroless plating, chemical vapor deposition, flame fusion spraying and sol gel coating. The bonding (see Figure 4(h)) may be thermocompression bonding in solid state at elevated temperatures under pressure or may be thermosonic bonding in solid state at elevated temperatures under pressure and ultrasonic power. It is preferable that the bonding is subjected to further annealing to strengthen the bonds.

In this example embodiment, the catalyst metal pads formed by the patterned catalyst layer 402 comprise material such as Ni, Co, Fe, or alloys and composites containing one or more of these elements. The catalyst metal pads may be directly deposited and formed on single metal layer pads such as Cu and Al pads. Alternatively, a barrier or adhesion layer comprising single or multiple metallic layers may be deposited on Cu or Al material, followed by the deposition of the catalyst layer. The barrier or adhesion layer materials may comprise Au, Ti, W, Cr, Zr, V, Nb, Pb, Pt, Ta, Mo, Pd, and alloys of at least two metal elements. In the example embodiment, the thickness of the catalyst layer 402 is about 2 nm to 2 μm. The catalyst layer and barrier

or adhesion layer deposition methods can include physical vapour deposition techniques such as sputtering, evaporation, laser ablation, and chemical vapour deposition techniques; flame fusion spraying as well as electroplating and electroless plating. Preferably, but not limiting to, physical vapour deposition techniques are employed due to the low deposition temperature and well controllable thin layer thickness. The deposition can be performed at room temperature. Patterning methods include, but are not limited to, optical lithography, extreme-ultraviolet (EUV) lithography, X-ray lithography, e-beam lithography, focus ion beam lithography, mechanical lithography, physical lithography and chemical lithography. The pad sizes may range from about 10 nm to about 100 μm.

In a fifth example embodiment, the carbon nanotubes are directly grown on the patterned catalyst pads by the deposition methods described above, followed by the deposition and patterning of a metal layer. The individual bundles of carbon nanotubes used as bumps are fixed by the metal layer. The carbon nanotubes with such arrangement are robust enough for the bonding process. Next, the carbon nanotube bumps coated with metal are bonded with the metal pads on another substrate by using diffusion bonding or thermosonic bonding technique. After bonding, the gap between two substrates is filled with polymer, such as underfill. The interconnected or packaged devices or systems have low resistance and excellent reliability.

Figures 5(a) to (g) are schematic diagrams illustrating a process flow in the fifth example embodiment. Figure 5(a) illustrates a catalyst layer 502 deposited on a first substrate 504. The first substrate 504 comprises a circuit layer 506 and a dielectric/passivation layer 508. Figure 5(b) illustrates lithography and patterning carried out on the catalyst layer 502 of the first substrate 504. Figure 5(c) illustrates growing of high density carbon nanotubes e.g. 510 on the patterned catalyst layer 502 of the first substrate 504. Figure 5(d) illustrates a bonding metal layer 512 deposited and patterned on the carbon nanotubes e.g. 510. The patterned bonding metal layer 512 acts as a strengthening/stabiliser layer on the carbon nanotubes e.g. 510. Figure 5(e) illustrates a second substrate 518 comprising a dielectric/passivation layer 520, a circuit layer 522 and metal pads e.g. 524. Figure 5(f) illustrates bonding of the patterned bonding metal layer 512 of the first substrate 504 to the metal pads e.g. 524 of the second substrate

518. The bonding may be carried out using bonding techniques such as, but not limited to, thermal compression or thermosonic bonding techniques. Figure 5(g) illustrates filling the gap between the first substrate 504 and the second substrate 518 with a polymer 526.

In the described fifth example embodiment, the bonding metal layer 512 may comprise material such as, but not limited to, the transition metals, Ni, Co, Cu, Au, Ti, W, Cr, Zn, Sn, Zr, Al, Mg, V, Nb, Pb, Ag, Pt, Ta, Mo, Pd, Ru, Cd, In, Ge, Bi and alloys of at least two metal elements. The coating may be carried out using methods such as, but not limited to, physical vapour deposition, sputtering, vapor evaporating, electroplating, electroless plating, chemical vapor deposition, flame fusion spraying and sol gel coating.

In this example embodiment, the bonding metal layer 512 may include a single layer metal or a multilayer metal. The metal pads e.g. 524 are deposited on the second substrate 518 using methods such as, but not limited to, physical vapour deposition, sputtering, vapor evaporating, electroplating, electroless plating, chemical vapor deposition, flame fusion spraying and sol gel coating. The bonding (see Figure 5(f)) may be thermocompression bonding in solid state at elevated temperatures under pressure or may be thermosonic bonding in solid state at elevated temperatures under pressure and ultrasonic power. It is preferable that the bonding is subjected to further annealing to strengthen the bonds.

In this example embodiment, the catalyst metal pads formed by the catalyst layer 502 comprise material such as Ni, Co, Fe, or alloys and composites containing one or more of these elements. The catalyst metal pads may be directly deposited and formed on single metal layer pads such as Cu and Al pads. Alternatively, a barrier or adhesion layer comprising single or multiple metallic layers may be deposited on Cu or Al material, followed by the deposition of the catalyst layer. The barrier or adhesion layer materials may comprise Au, Ti, W, Cr, Zr, V, Nb, Pb, Pt, Ta, Mo, Pd, and alloys of at least two metal elements. In the example embodiment, the thickness of the catalyst layer 502 is about 2 nm to 2 μm. The catalyst layer 502 and barrier or adhesion layer deposition methods can include physical vapour deposition techniques such as sputtering, evaporation, laser ablation, and chemical vapour deposition techniques, flame fusion

spraying as well as electroplating and electroless plating. Preferably, but not limiting to, physical vapour deposition techniques are employed due to the low deposition temperature and well controllable thin layer thickness. The deposition can be performed at room temperature. Patterning methods include, but are not limited to, optical lithography, extreme-ultraviolet (EUV) lithography, X-ray lithography, e-beam lithography, focus ion beam lithography, mechanical lithography, physical lithography and chemical lithography. The pad sizes may range from about 10 nm to about 100 μm.

Figure 6 is a schematic flowchart 600 illustrating a method for interconnection for semiconductor devices. At step 602, a first substantially vertical nano structure is provided on a first substrate. At step 604, a solder free electrical contact between the first nano structure and an electrical circuit of a second substrate is formed.

In the described example embodiments, the carbon nanotubes are synthesized using arc-discharge, pyrolysis of hydrocarbons over metal particles, chemical vapor deposition (CVD), laser vaporization of graphite targets, solar carbon vaporization, and electrolysis of carbon electrodes in molten ionic salts etc. The carbon nanotubes may include single-wall carbon nanotubes and/or multi-wall carbon nanotubes. The carbon nanotubes may be in purified or unpurified form. In the described example embodiments, the carbon nanotubes are preferably purified.

As will be appreciated by a person skilled in the art, advantages of using CVD for processing carbon nanotubes include an ability to mass produce the carbon nanotubes, using a low growth temperature, an ability to control the orientation of the carbon nanotubes, an ability to predefine growth locations of the carbon nanotubes and there is no requirement for purification of grown carbon nanotubes.

In the described example embodiments, the interconnection and packaging may form part of micro/nano devices and systems fabrication. Such interconnection and packaging may offer superior mechanical, thermal and electrical properties of the devices and systems. The described example embodiments may provide an approach for integrating and packaging micro/nanodevices and systems, such as for the devices and systems using nanometer bump size and nanometer scale pitch. Thus, the

interconnect sizes may be scalable down to nanometers and the pitch sizes may be scalable down to nanometers. Therefore, the described example embodiments may be applicable for extremely high density devices. Furthermore, the example embodiments may produce devices having better reliability and performance over current devices. In addition, devices of the example embodiments may advantageously offer low contact resistance.

It will be appreciated by a person skilled in the art that the described example embodiments may be used in e.g. the fields of electronics, optoelectronics, Micro-Electro-Mechanical Systems (MEMS), Nano-Electro-Mechanical Systems (NEMS) and three-dimensional integrated circuits (3D ICs).

It will be appreciated by a person skilled in the art that numerous variations and/or modifications may be made to the present invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects to be illustrative and not restrictive.

For example, instead of using carbon nanotubes in example embodiments, conductive or semiconductive nanowires, nanorods, nanowiskers, nanoribbons etc may be used. For the bonding process, processes other than thermocompression and thermosonic bonding may be used, including e.g. conductive polymers or composites, metal and metal alloys used as intermediate layers to connect substantially vertical nano structures coated with metal on a first substrate to metal pads on a second substrate.

CLAIMS

1. A method for electrical interconnection, the method comprising,

providing a first substantially vertical nano structure on a first substrate;

strengthening the first nano structure; and

forming a solder free electrical contact between the first nano structure and an electrical circuit of a second substrate.

2. The method as claimed in claim 1, wherein said forming the solder free electrical contact comprises the steps of:

forming a second substantially vertical nano structure on the second substrate; and

engaging the first and second nano structures.

3. The method as claimed in claim 2, wherein the engaging the first and second nano structures comprises physically contacting the first and second nano structures.

4. The method as claimed in claim 2, wherein the engaging the first and second nano structures comprises inserting the first nano structure into the second nano structure.

5. The method as claimed in claim 2, wherein the engaging the first and second nano structures comprises inserting the first nano structure to contact a base of the second nano structure.

6. The method as claimed in any one of claims 2 to 5, wherein said forming the first and second nano structures comprise the steps of:

depositing respective catalyst layers on the first and second substrates;

performing patterning and lithography on the respective catalyst layers; and

growing the first and second nano structures on the respective patterned catalyst layers.

7. The method as claimed in any one of claims 2 to 6, further comprising the step of metallizing the first and second nano structures.

8. The method as claimed in claim 1, wherein said forming the solder free electrical contact comprises the steps of:

forming a contact pad on the second substrate; and

forming the electrical contact between the strengthened first nano structure to the contact pad of the second substrate.

9. The method as claimed in claim 8, wherein said forming the electrical contact to the contact pad of the second substrate comprises thermal compression, thermosonic bonding, or both.

10. The method as claimed in any one of claims 1 to 9, wherein the step of strengthening the first nano structure comprises forming a template for providing the first nano structure therein wherein the template is formed by depositing a layer of template material and performing patterning and lithography on the layer of template material.

11. The method as claimed in any one of claims 1 to 9, wherein the step of strengthening the first nano structure comprises encapsulating the first nano structure using a polymer material and exposing a contact surface of the encapsulated first nano structure prior to forming the electrical contact to the contact pad of the second substrate.

12. The method as claimed in any one of claims 8 to 11, further comprising depositing an intermediate electrically conducting layer on the first nano structure prior to forming the electrical contact.

13. The method as claimed in any one of claims 1 to 9, wherein the step of strengthening the first nano structure comprises providing an electrically conducting stabiliser layer on the first nano structure.

14. The method as claimed in any one of claims 8 to 13, wherein said forming the first nano structure comprises the steps of:

depositing a catalyst layer on the first substrate;

performing patterning and lithography on the catalyst layer; and

growing the first nano structure on the patterned catalyst layer.

15. The method as claimed in any one of claims 1 to 14, further comprising filling a gap between the first and second substrates using an electrically insolating material.

16. The method as claimed in claim 15, wherein the electrically insolating material is selected from a group consisting of polymeric underfill, polymer composite and adhesive.

17. An interconnection structure comprising:

a strengthened first substantially vertical nano structure of a first substrate; and

a solder free electrical contact between the first nano structure and an electrical circuit of the second substrate.

18. The interconnection structure as claimed in claim 17, wherein the solder free electrical contact comprises a second substantially vertical nano structure of the second substrate in engagement with the first nano structure.

19. The interconnection structure as claimed in claim 18, wherein the first nano structure is in physical contact with the second nano structure.

20. The interconnection structure as claimed in claim 18, wherein the first nano structure is inserted into the second nano structure.

21. The interconnection structure as claimed in claim 19, wherein the first nano structure is inserted into the second nano structure such that the first nano structure contacts a base of the second nano structure.

22. The interconnection structure as claimed in any one of claims 18 to 21, the interconnection structure further comprising a first patterned catalyst layer between the first nano structure and the first substrate and a second patterned catalyst layer between the second nano structure and the second substrate.

23. The interconnection structure as claimed in any one of claims 18 to 22, wherein the first nano structure and the second nano structure are metallized.

24. The interconnection structure as claimed in claim 17, comprising

a contact pad on the second substrate; and

wherein the electrical contact is formed between the strengthened first nano structure and the contact pad of the second substrate.

25. The interconnection structure as claimed in claim 17, the interconnection structure comprising a template formed around the first nano structure.

26. The interconnection structure as claimed in claim 17, the interconnection structure comprising a polymer material encapsulating the first nano structure.

27. The interconnection structure as claimed in any one of claims 24 to 26, the interconnection structure comprising an intermediate electrically conducting layer on the first nano structure.

28. The interconnection structure as claimed in claim 17, the interconnection structure comprising an electrically conducting stabiliser layer on the first nano structure.

29. The interconnection structure as claimed in any one of claims 24 to 28, the interconnection structure further comprising a patterned catalyst layer between the first nano structure and the first substrate.

30. The interconnection structure as claimed in any one of claims 17 to 29, further comprising an electrically insolating material filling between the first and second substrates.

31. The interconnection structure as claimed in claim 30, wherein the electrically insolating material filling is selected from a group consisting of polymeric underfill, polymer composite and adhesive.

A Method For Electrical Interconnection And An Interconnection Structure

ABSTRACT

A method for electrical interconnection and an interconnection structure are provided. The method comprises providing a first substantially vertical nano structure on a first substrate; and forming a solder free electrical contact between the first nano structure and an electrical circuit of a second substrate.

FIG. 6