

明 細 書

CMOS集積回路

技術分野

この発明は、CMOS（相補絶縁ゲート形半導体素子、Complementary Metal-Oxide Semiconductor）で構成された半導体集積回路（CMOS・Integrated circuit、CMOS・IC）に関し、特定すると、CMOSの超大規模集積回路（ULSI、Ultra-Large Scale Integrated circuit）内の信号伝送路の改良に関する。

背景技術

良く知られているように、1つの大規模集積回路（LSI）として形成された半導体素子や論理回路等は配線によって所定の電氣的接続が行なわれている。CMOSで構成された超大規模集積回路も同様に、配線によってCMOSやCMOS論理回路等が電氣的に接続されている。この配線は、例えば集積回路の表面に形成された所定のパターンの導電路（導体）よりなることがしばしばである。

図6は従来のCMOSの超大規模集積回路の内部回路の一例を示す。この例は1つのCMOSよりなる送信側ゲート11と同じく1つのCMOSよりなる受信側ゲート18が信号伝送路、この例では導電路（導体）15によって電氣的に接続されている事例を示す。送信側ゲート11及び受信側ゲート18は共にこの例ではCMOSインバータとして構成されている。

送信側ゲート11はpチャネルのMOSFET（MOS電界効果トランジスタ、Field Effect Transistor）12のゲートとnチャネルのMOSFET13のゲートとが互いに接続されて入力端子14に接続され、pチャネルのFET12のドレイン及びnチャネルのFET13のドレインが互いに接続されて導電路15の一端（入力端）に接続され、pチャネルのFET12のソースは+VDD（正電位）の電源端子16に、nチャネルのFET13のソースは-VSS（負電位）の電源端子17（共通電位点又は接地点に接続される場合もある）にそれ

ぞれ接続されている。

一方、受信側ゲート18はpチャネルのMOSFET21のゲートとnチャネルのMOSFET22のゲートとが互いに接続されて入力端子23に接続され、pチャネルのFET21のドレイン及びnチャネルのFET22のドレインが互いに接続されて出力端子（図示せず）に接続され、pチャネルのFET21のソースは+VDDの電源端子16に、nチャネルのFET13のソースは-VSSの電源端子17にそれぞれ接続されている。導電路15の他端（出力端）は入力端子23に接続されている。

このような回路構成においては、導電路15の分布容量CL（破線で示す）と、受信側ゲート18の入力容量CG（同じく破線で示す）が存在するから、送信側ゲート11からこの導電路15を通じて受信側ゲート18へ信号が伝送される際に、この信号によって導電路15の分布容量CLと、受信側ゲート18の入力容量CGが充電されることになる。送信側ゲート11の等価出力抵抗を R_0 とすると、受信側ゲート18の入力電圧波形の遷移時間は $R_0 \times (CL + CG)$ となる。

実際には導電路15の分布抵抗によっても遷移時間は影響を受けるが、通常、この分布抵抗に対し等価出力抵抗 R_0 が支配的であるから、この分布抵抗の影響を省略した。また、等価出力抵抗 R_0 は非線形な性質を有しており、電圧と共に抵抗値が変化するが、この点も説明を簡単にするために無視した。

近年、集積回路（IC）は高集積化、大規模化の一途をたどっており、チップサイズも大きくなってきている。例えば、図7に示すようにチップ24の一辺の長さが15mmを超えるような超大規模集積回路も珍しくない。このような大きなチップではその内部に形成された回路や素子間を相互接続する配線（導電路）の長さも長くなり、20mmを超える配線もある。ある超大規模集積回路の見積りによれば20mmを超える配線の本数が全体の5%以上となった。

図7はCMOSにより構成された超大規模集積回路の内部の回路構成の一例を示し、多数のゲートと、それら間を接続する配線、即ち、導電路25、26、27を模式的に示す。図示するように、比較的短い（200 μ m程度の）導電路25以外に、非常に長い（20mm以上の）導電路26や、非常に長く（20mm

以上で)、かつ多数のゲートを負荷としている導電路27が存在する。この導電路27はクロック信号の分配やバス信号の伝送などに用いられ、これらの信号はチップ全体の性能(動作速度)を左右する。

図7において、送信側ゲート(図の左側の3つのゲート)より導電路25、26、27を通じてステップ波形を伝送したときの対応するそれぞれの受信側ゲートの入力波形はそれぞれ図8Aの曲線25a、26a、27aのようになり、インパルスを送信したときの応答はそれぞれ図8Bの曲線25b、26b、27bに示すようにする。これら波形から明瞭のように、短い導電路25に対し、長い導電路26、27はそれらの遷移時間が非常に長いので、ステップ応答では伝搬遅延が著しく長くなり、パルス応答では、パルス幅が狭いとパルスが消失してしまう。このため周波数が高い(繰り返し周期の短い)クロック信号は長い導電路を通過することができない。換言すれば、チップ全体の性能(動作速度)を高くすることができないという重大な欠点がある。

また、高集積化、低電力化のためCMOSの微細化が進むにつれ、ゲート単体の動作速度は向上するが、等価出力抵抗 R_0 が高くなり、単位長当たりの配線容量は変化しないどころか、かえって増加する傾向にある。このため、遷移時間がさらに長くなり、チップの動作速度をより一層制限するという欠点があった。

このような点から、チップ内配線のスループットを向上させるために、近年、光を用いたチップ内信号伝送方法が研究されている。しかし、シリコンチップ上に化合物半導体による発光・受光素子を構成したり、電気配線層とは別に光導波路を構成する必要がある、実用化は現在困難であり、また、実現したとしてもサイズ、コストの上昇が大きなものとなる。

発明の開示

この発明の目的は、高速で信号を伝送することができるCMOS構造の大規模集積回路を提供することである。

この発明においては、CMOSで構成された集積回路において、上記集積回路の信号伝送路の受信側ゲートとして、入力インピーダンスが著しく低く、入力電流の大小に応じた出力電圧を発生する電流入力形ゲートを用いたCMOS集積回

路が提供され、上記目的は達成される。

好ましい一実施例においては、上記電流入力形ゲートは、入力端子がpチャネルMOSFETよりなる第1のカレントミラー回路を通じて正の電源端子に接続され、かつ上記入力端子がnチャネルMOSFETよりなる第2のカレントミラー回路を通じて負の電源端子に接続されている。

第1の変形例においては、上記電流入力形ゲートは、入力端と出力端が短絡接続されたCMOSインバータを含み、このインバータの入力端が上記入力端子に接続され、上記インバータの両電源接続端が上記第1のカレントミラー回路の入力側及び上記第2のカレントミラー回路の入力側にそれぞれ接続されている。

また、第2の変形例においては、上記電流入力形ゲートは、上記CMOSインバータの出力端が上記入力端子に接続され、上記CMOSインバータの入力端に、上記正の電源端子及び上記負の電源端子の midpoint 電位が与えられ、上記CMOSインバータの両電源接続端が上記第1のカレントミラー回路の入力側及び上記第2のカレントミラー回路の入力側にそれぞれ接続されている。

また、第3の変形例においては、上記電流入力形ゲートは、上記入力端子と上記第1のカレントミラー回路の入力側との間に直列に挿入されたnチャネルMOSFETと、上記入力端子と上記第2のカレントミラー回路の入力側との間に挿入されたpチャネルMOSFETとを含み、上記nチャネルMOSFETのゲートに、上記両電源端子間の midpoint 電位と上記nチャネルMOSFETのしきい値電圧とを加算した電位が印加され、上記pチャネルMOSFETのゲートに、上記両電源端子間の midpoint 電位から、上記pチャネルMOSFETのしきい値電圧を引いた電位が印加される。

好ましい他の実施例においては、上記電流入力形ゲートは、1つの差動増幅器の反転入力端を上記入力端子に接続し、この差動増幅器の反転入力端と出力端との間に負帰還コンデンサを接続し、上記差動増幅器の非反転入力端に、入力論理信号の midpoint 電位を印加した構成を有する。

各実施例及び各変形例において、上記信号伝送路の送信側ゲートは電流出力形ゲートであり、そしてこの電流出力形ゲートはCMOSインバータであることが好ましい。

また、一実施例においては、上記電流出力形ゲートは、CMOSインバータの出力端がコンデンサを通じて接地され、上記インバータの両電源接続端がそれぞれpチャネルMOSFETよりなる第1のカレントミラー回路及びnチャネルMOSFETよりなる第2のカレントミラー回路を通じて、正電源端子及び負電源端子にそれぞれ接続され、これら両カレントミラー回路の出力端が上記信号伝送路に接続されている構成を有する。なお、上記コンデンサと並列に電流保持用抵抗素子を接続してもよい。

上記この発明の構成によれば、受信側ゲートとして低入力インピーダンスの電流入力形のゲートを用いているため、配線容量CL、ゲート入力容量CGを急速に充電することができ、信号の遷移時間が著しく短くなる。従って、周波数が高い（繰り返し周期の短い）クロック信号でもCMOS・IC内の長い導電路を通過することが可能となり、CMOSチップ全体の性能（動作速度）を高くすることができる。

図面の簡単な説明

図1はこの発明によるCMOS大規模集積回路の第1の実施例の内部回路の一例を示す回路接続図である。

図2A及び図2Bは図1に示された電荷感应形ゲートの回路例をそれぞれ示す回路接続図である。

図3A、図3B及び図3Cは定常電流を零にすることができる電荷感应形ゲートの回路例をそれぞれ示す回路接続図である。

図4はこの発明によるCMOS大規模集積回路の第2の実施例の内部回路の一例を示す回路接続図である。

図5はこの発明によるCMOS大規模集積回路の第3の実施例の内部回路の一例を示す回路構成図である。

図6は従来のCMOS大規模集積回路の内部回路の一例を示す回路接続図である。

図7はCMOS大規模集積回路内の信号伝送路の各種の例を示す模式図である。

図8A及び図8Bは図7に示す種々の長さの伝送路にステップ波形及びインバ

ルスを送信したときの受信側ゲートの応答をそれぞれ示す波形図である。

発明を実施するための最良の形態

以下、図1～図5を参照してこの発明の実施例について詳細に説明する。

図1はこの発明によるCMOS大規模集積回路の第1の実施例の内部回路を示す。なお、図1～図5において、図6と対応する部分、素子には同一符号を付けて示し、必要のない限りそれらの説明を省略する。

この第1の実施例においても送信側ゲート11はpチャネルのMOSFET12とnチャネルのMOSFET13よりなるCMOS構成のインバータであり、図6に示した従来技術の送信側ゲート11と同じ構成であるので、その説明を省略する。

一方、導電路15の出力端に接続される受信側のゲート31は、電流入力形で、かつ低入力インピーダンスのゲート（以下、電荷感応形ゲートと呼ぶ）31によって構成される。この電荷感応形ゲート31の入力インピーダンス R_{in} は送信側のゲート11の等価出力抵抗 R_0 に対して十分小さく、従って、この電荷感応形ゲート31は入力電圧の振幅をほぼ零とし、負荷容量への電流の流入を実質的にゼロにして、入力電流に応じた出力電圧を発生するように動作する。

電荷感応形ゲート31の回路構成の一例を図2Aに示す。この電荷感応形ゲート31は、pチャネルMOSFET33とnチャネルMOSFET34とからなるインバータ35と、pチャネルMOSFET33のソースと+VDD電源端子16との間に接続されたpチャネルMOSFET37と、nチャネルFET34のソースと-VSS電源端子（又は接地端子）17との間に接続されたnチャネルMOSFET38と、これらMOSFET37及び38のゲートにそれぞれのゲートが接続されたpチャネルMOSFET39及びnチャネルMOSFET41とを含む。

インバータ35の入力端（共通接続のゲート）と出力端（共通接続のドレイン）は互いに短絡接続されて入力端子36に接続され、pチャネルFET33のソースがpチャネルFET37のドレインーソースを通じて+VDD電源端子16に接続され、nチャネルFET34のソースがnチャネルFET38のドレインー

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ソースを通じて $-VSS$ 電源端子（又は接地端子）17に接続される。FET37及び38の各ドレインとゲート間はそれぞれ短絡接続され、また、FET39及び41の各ドレインは互いに接続されて出力端子42に接続され、それらの各ソースはそれぞれ電源端子16及び17に接続される。つまり、インバータ35の両電源接続端はpチャネルMOSFETカレントミラー（current Miller）回路及びnチャネルMOSFETカレントミラー回路の各入力側にそれぞれ接続されている。

上記構成によれば、インバータ35の入力端と出力端が短絡されているため、入力端子36より見たインピーダンス R_{in} は著しく小さなものとなり、かつ入力端子36の電位は $+VDD$ と $-VSS$ （又は $0V$ ）のほぼ中点の電位となる。つまり、入力端子36の電位はインバータ35のしきい値電圧、即ち、出力の論理が反転するときの入力電圧となり、両FET33、34のゲートソース間がこのしきい値電圧によってそれぞれ自己バイアスされる。

このように入力端子36の電位はインバータ35が反転する電位レベルであるから、両FET33及び34の各ドレインソース間のインピーダンスは十分小さく、入力端子36のインピーダンスはこれらドレインソース間インピーダンスの並列の値となり、最も小さくなる。加えて、負帰還の効果によりインピーダンスはさらに小さくなり、しかも、その最小インピーダンス点からずれようとすると元に戻す作用が働く。

さらに、FET37と39、FET38と41はそれぞれカレントミラー回路を構成しており、これらカレントミラー回路の入力インピーダンス、つまり、FET37、38のドレインのインピーダンスが等しくしてあり、加えてFET33、34のベータ（ β ）比を $1:1$ とし、かつFET33、34のしきい値電圧が等しくなるように設計してある。これにより、入力端子36の電圧は電源電圧 $+VDD$ と $-VSS$ との中点に丁度なる。

なお、このゲート回路は入力オープン（開放状態）でもFET33、34、37、38に定常的な貫通電流が流れる。従って、消費電力をなるべく小とする点から、FET33、34、37、38のサイズ、つまり、ゲート幅を小さくすることが望ましいが、実際には動作速度とのトレードオフ（trade off）により

ゲート幅は決定される。

送信側ゲート 11 から入力端子 36 に流れる電流は全てカレントミラー回路の FET 37 又は 38 に流れ、FET 33、34 からそれぞれ FET 37、38 側を見たインピーダンスは電流入力であるために著しく小さい。この場合、電流が送信側ゲート 11 から入力端子 36 の方向に流れる（図 1 の I_H 参照）ときには FET 38 に流れ、その逆方向に流れる（図 1 の I_L 参照）ときには FET 37 に流れる。このとき、FET 37、38 にそれぞれ流れる電流の差に比例した電流の差が FET 39、41 を流れる電流に現れる。FET 39 の方に多く電流が流れるときには、出力端子 42 の電位が上昇し、ほぼ +V_{DD} となり、逆に FET 41 の方に多く電流が流れるときには出力端子 42 の電流は低下し、ほぼ -V_{SS} となる。

図 1 中の電荷感应形ゲート 31 は、このように入力インピーダンス R_{in} が著しく小さいため、配線容量 C_L 及びゲート入力容量 C_G は、共にゲート 31 の小さい入力インピーダンスで短絡に近い状態となっている。このため、送信側ゲート 11 から出力される信号が配線容量 C_L 及びゲート入力容量 C_G を充電する必要が殆どなく、遷移時間は著しく小さくなる。つまり、送信側ゲート 11 から出力される信号の変化が受信側ゲート 31 の入力端子 36 に高速で到達する。しかも、送信側ゲート 11 の出力が高レベルになれば、図 2 A の回路例では、受信側ゲート 31 の出力端子 42 の電位はほぼ -V_{SS} になり、逆に送信側ゲート 11 の出力が低レベルになれば受信側ゲート 31 の出力端子 42 の電位はほぼ +V_{DD} となるから、送信側ゲート 11 の出力が反転されて受信側ゲート 31 の出力 42 に現れる。

電荷感应形ゲート 31 としては、図 2 B に示すように、図 2 A 中のインバータ 35 を省略して、入力端子 36 を FET 37、38 の各ドレインに直接接続してもよい。この第 1 の変形例においても、入力端子 36 の電位が +V_{DD} と -V_{SS} の中点となり、かつカレントミラー回路への電流入力であるので入力インピーダンスが小さい。このため、図 2 A に示した電荷感应形ゲート回路と同様の作用効果が得られる。ただし、図 2 A の場合よりも入力インピーダンスが大きく、かつ貫通電流も大きい難点があるが、FET の素子数が図 2 A のものより少ないと

いう利点がある。

図3Aは電荷感应形ゲート31の第2の変形例を示す。この第2の変形例は、図2A中のインバータ35の代わりに、nチャネルMOSFET44とpチャネルMOSFET45の各ソースを入力端子36に接続し、両FET44及び45のゲートを端子46に接続し、両ドレインをそれぞれFET37及び38のドレインに接続し、端子46に+VDD電源端子16と-VSS電源端子17の midpoint 電位 V_c を印加するように構成したものである。

上記構成において、入力端子36の電位が $V_c \pm V_{th}$ (V_{th} は両FET44、45のしきい値電圧)の範囲にある場合には、FET44、45にソース電流が流れず、従って、入力インピーダンスは高インピーダンス状態となる。入力オープン状態では定常的な貫通電流は流れない。

入力端子36の入力電圧が $V_c \pm V_{th}$ の範囲より僅かでも外れると、FET44又は45が導通し、これに応じて出力端子42の出力電圧が+VDD又は-VSSに近づく。 V_{th} は電源電圧の1割程度に取られることが多いので、入力端子36の電圧振幅が電源電圧の20%位で済み、この程度なら通常、十分な高速化が期待できる。具体的に説明すると、入力電圧の振幅を $2V_{th}$ 程度の小さなものとすることができるから、配線容量 C_L 、ゲート入力容量 C_G にそれ程影響されずに信号を伝送することができる。即ち、従来より遷移時間を著しく小さくすることができる。なお、実際には V_{th} はpチャネルFETとnチャネルFETとで多少異なるが、理解を容易にするために等しいものとした。

定常貫通電流をゼロとし、しかも、入力端子36の電圧の振幅をさらに小さくしたい場合には、図3Bに示すようにFET44及び45のゲートを互いに分離し、それぞれのゲートに、 $V_c + V_{th}(n)$ ($V_{th}(n)$ はnチャネルFET44のしきい値電圧)及び $V_c - V_{th}(p)$ ($V_{th}(p)$ はpチャネルFET45のしきい値電圧)をそれぞれ印加する。この状態ではFET44はそのゲートに $V_c + V_{th}(n)$ が与えられており、FET45はそのゲートに $V_c - V_{th}(p)$ が与えられているから、入力端子36の電位が V_c より僅かでも下がると、FET44に電流が流れ、逆に入力端子36の電位が V_c より僅かでも上がると、FET45に電流が流れることになる。

電荷感应形ゲート 31 としては、図 3C に示すように、高利得、広帯域、高速動作の差動増幅器 48 の反転入力端子を入力端子 36 に接続し、その出力端子を出力端子 42 に接続し、これら出力端子と反転入力端子間に負帰還コンデンサ 49 を接続し、差動増幅器 48 の非反転入力端子に中点電位 V_c を印加した構成としてもよい。

この差動増幅器 48 は入力端子 36 に流れ込む電流を積分し、それに比例した出力電圧を極性反転して出力する。従って、入力端子 36 の電位が V_c よりも僅かでも上昇すると、この差をなくすようにコンデンサ 49 に負帰還電流による充電が急速になされ、出力端子 42 の出力電位が低下する。また、入力端子 36 の電位が V_c よりも僅かでも低下すると、コンデンサ 49 に逆極性の負帰還電流による充電が急速になされて出力端子 42 の出力電位が上昇する。よって、入力端子 36 の電位は V_c に保持され、入力インピーダンスはほぼゼロになる。

このように入力インピーダンスがほぼゼロになり、かつ差動増幅器 48 の利得が大きく、広帯域動作であるから、入力端子 36 に供給される入力電流の積分を急速に行うことができる。よって、配線容量 C_L 、入力ゲート容量 C_G を急速に充電することができるから、遷移時間は非常に短くなり、高速動作が可能になる。なお、次段の入力電圧範囲に合わせるために、出力端子 42 に必要に応じて出力電圧の振幅を制限する回路を接続する。

図 2A 及び図 2B に示した電荷感应形ゲート 31 は定常的に電力を消費する。送信側ゲート 11 が過渡電流だけを出力する形式の場合には、信号伝送に寄与する電流は信号の遷移時に流れる過渡電流だけであるから、この過渡電流のみを流すようにすることがより好ましい。

図 4 はこの発明による CMOS 大規模集積回路の第 2 の実施例の内部回路を示すもので、過渡電流のみを流すように構成した事例を示す。

この第 2 の実施例では送信側のゲート 11 として、図 2A に示した受信側ゲートである電荷感应形ゲート 31 の回路構成と類似するゲートを使用する。この送信側ゲート 11 は、p チャネル MOSFET 51 と n チャネル MOSFET 52 とからなるインバータ 53 と、p チャネル MOSFET 51 のソースと $+V_{DD}$ (正電位) の電源端子 16 との間に接続された p チャネル MOSFET 55 と、

nチャネルFET 52のソースと-VSS（負電位又は共通電位）の電源端子17との間に接続されたnチャネルMOSFET 56と、これらMOSFET 55及び56のゲートにそれぞれのゲートが接続されたpチャネルMOSFET 57及びnチャネルMOSFET 58とを含む。

インバータ53の入力端、即ち、共通接続されたゲートは入力端子14に接続され、インバータ53の出力端、即ち、共通接続されたドレインはコンデンサ54を通じて共通電位点又は接地電位に接続され、pチャネルFET 51のソースがpチャネルFET 55のドレインソースを通じて+VDD電源端子16に接続され、nチャネルFET 52のソースがnチャネルFET 56のドレインソースを通じて-VSS電源端子17に接続される。FET 55及び56の各ドレインとゲート間はそれぞれ短絡接続され、また、FET 57及び58の各ドレインは互いに接続されて導電路15の入力端に接続され、それらの各ソースはそれぞれ電源端子16及び17に接続される。つまり、この第2の実施例でもインバータ53の両電源接続端はpチャネルMOSFETカレントミラー回路及びnチャネルMOSFETカレントミラー回路の各入力側にそれぞれ接続されている。

よって、この送信側ゲートの構成は図2Aに示した電荷感応形ゲート31において、そのインバータ35の入出力端を共通に接続しないで、入力端のみを入力端子36に接続し、出力端をコンデンサ54を通じて共通電位点又は接地電位点に接続したものと同一であることが理解されよう。

上記構成において、入力端子14の電位が両電源+VDDと-VSSの midpoint の電位 V_c より高レベルになると、FET 52に電流が流れ、コンデンサ54はFET 52側が負に充電される。この電流はFET 56及び58よりなるカレントミラー回路で増倍され、導電路15に受信側ゲート31から電流（ I_L ）を吸い込む過渡電流を発生する。この電流信号の遷移期間が終わると電流は零になり、定常的な消費電力は無くなる。

入力端子14の電位が V_c より低下すると、FET 51に電流が流れ、コンデンサ54は今度はFET 51側が正に充電される。この電流はFET 55及び57よりなるカレントミラー回路で増倍され、導電路15を通じて受信側ゲート31の方向に電流（ I_H ）を供給する。この場合も電流信号の遷移期間が終わると

電流は零となり、定常的な電力消費はない。

このように信号の遷移期間のみ電流を流す送信側のゲート 11 を用いる場合でも、受信側の電荷感应形ゲート 31 として、図 2 A 及び 2 B に示したように、定常的な貫通電流が流れる形式のものを用いる場合には、入力端子 14 の信号の遷移の間隔が長いと（電流が全く流れない期間が長いと）、配線容量 CL 及びゲート入力容量 CG に充電された電荷が放電され、送信側ゲート 11 の信号出力状態を保持することができない。

このような場合には図 4 に点線で示すように、コンデンサ 54 と並列に、抵抗素子（又は抵抗素子として動作する FET）61 を接続して電位保持のための微少の電流を流し、入力端子 14 の信号入力状態と対応した信号出力状態が導電路 15 に対して保持されるようにする。この抵抗素子 61 としては遷移期間以外でも信号出力状態を保持することができる最低限の電流を流すことができるものであればよい。

受信側の電荷感应形ゲート 31 として、図 3 A 及び 3 B に示すように、定常的貫通電流やリーク電流がないものを用いれば、図 4 に示した送信側ゲートを用いることができる。しかし、電荷感应形ゲート 31 の入力電位を長期間一定に保持することは、微少なリーク電流の存在により困難である場合には、伝送しようとする信号が長期にわたって変化しない場合は、先に述べたようにコンデンサ 54 と並列に抵抗素子を接続する。

受信側の電荷感应形ゲート 31 として図 3 C に示したものを用いる場合には、差動増幅器 48 の入力リーク電流に依存するが、この場合も伝送しようとする信号が長期にわたって変化しない場合を除けば、コンデンサ 54 と並列の抵抗素子による電位保持電流を流す必要はない。

なお、送信側ゲート 11 として、図 1 に示すように、定常電流を流せるゲートを用いる場合には、いずれの電荷感应形ゲートでも使用できる。クロック信号のように信号の遷移が常時、高速で行われる信号の伝送においては、図 4 に示した送信側ゲートに対し、図 2 A 及び 2 B、図 3 A ~ 3 C のいずれの形式の電荷感应形ゲートを受信側に設けてもよい。

送信側ゲート 11 は電流出力形であり、受信側ゲート 31 は電荷感应形ゲート、

つまり、電流入力形であるから、例えば図5に示すように導電路15に、送信用の電流出力形ゲート63を複数接続し、また、受信用の電流入力形ゲート64を複数接続して導電路15をバスとして用いることも容易に実行できる。特に、電流出力形ゲート63として遷移期間のみ電流を出力する図4に示した遷移電流出力ゲートを用い、電流入力形ゲート64として図3A及び3Bに示した定常電流がゼロの電荷感応形ゲートを用いれば、定常状態では導電路15に電流が流れないため、電流出力形ゲート63を高インピーダンス状態（インヒビット（inhibit）状態）にする必要がなく、そのための制御回路、タイミング調整も不要となる。

以上説明したように、この発明によれば、受信側ゲートとして低入力インピーダンスの電流入力形のゲートを用いているため、配線容量CL、ゲート入力容量CGを急速に充電することができ、信号の遷移時間が著しく短くなる。従って、周波数が高い（繰り返し周期の短い）クロック信号でもCMOS・IC内の長い導電路を通過することが可能となり、CMOSチップ全体の性能（動作速度）を高くすることができる。特に、送信側ゲートとして、信号の遷移期間だけ電流を流し、受信側ゲートとして定常電流は流さないものを用いることによって消費電力を小とすることができる。



請 求 の 範 囲

1. CMOSで構成された集積回路において、

上記集積回路の信号伝送路の受信側ゲートとして、入力インピーダンスが著しく低く、入力電流の大小に応じた出力電圧を発生する電流入力形ゲートが用いられていることを特徴とするCMOS集積回路。

2. 上記電流入力形ゲートは、入力端子がpチャネルMOSFETよりなる第1のカレントミラー回路を通じて正の電源端子に接続され、かつ上記入力端子がnチャネルMOSFETよりなる第2のカレントミラー回路を通じて負の電源端子に接続されていることを特徴とする請求の範囲第1項に記載のCMOS集積回路。

3. 入力端と出力端が短絡接続されたCMOSインバータの入力端が上記入力端子に接続され、上記CMOSインバータの両電源接続端が上記第1のカレントミラー回路の入力側及び上記第2のカレントミラー回路の入力側にそれぞれ接続されていることを特徴とする請求の範囲第2項に記載のCMOS集積回路。

4. 上記CMOSインバータの出力端が上記入力端子に接続され、上記CMOSインバータの入力端に、上記正の電源端子電圧及び上記負の電源端子電圧の midpoint 電位が与えられ、上記CMOSインバータの両電源接続端が上記第1のカレントミラー回路の入力側及び上記第2のカレントミラー回路の入力側にそれぞれ接続されていることを特徴とする請求の範囲第2項に記載のCMOS集積回路。

5. 上記入力端子と上記第1のカレントミラー回路の入力側との間にnチャネルMOSFETが直列に挿入され、このnチャネルMOSFETのゲートに、上記両電源端子間の midpoint 電位と上記nチャネルMOSFETのしきい値電圧とを加算した電位が印加され、上記入力端子と上記第2のカレントミラー回路の入力側との間にpチャネルMOSFETが直列に挿入され、このpチャネルMOSFETのゲートに、上記両電源端子間の midpoint 電位から、上記pチャネルMOSFETの



しきい値電圧を引いた電位が印加されていることを特徴とする請求の範囲第2項に記載のCMOS集積回路。

6. 上記電流入力形ゲートは、1つの差動増幅器の反転入力端を上記入力端子に接続し、この差動増幅器の反転入力端と出力端との間に負帰還コンデンサを接続し、上記差動増幅器の非反転入力端に、入力論理信号の midpoint 電位を印加した構成を有することを特徴とする請求の範囲第1項に記載のCMOS集積回路。

7. 上記信号伝送路の送信側ゲートは電流出力形ゲートであることを特徴とする請求の範囲第1項乃至第6項のいずれか1つに記載のCMOS集積回路。

8. 上記電流出力形ゲートはCMOSインバータであることを特徴とする請求の範囲第7項に記載のCMOS集積回路。

9. 上記電流出力形ゲートは、CMOSインバータの出力端がコンデンサを通じて接地され、上記インバータの両電源接続端がそれぞれpチャネルMOSFETよりなる第1のカレントミラー回路及びnチャネルMOSFETよりなる第2のカレントミラー回路を通じて、正電源端子及び負電源端子に接続され、これら両カレントミラー回路の出力端が上記信号伝送路に接続されている構成を有することを特徴とする請求の範囲第7項に記載のCMOS集積回路。

10. 上記コンデンサと並列に電流保持用抵抗素子が接続されていることを特徴とする請求の範囲第9項に記載のCMOS集積回路。

1/4

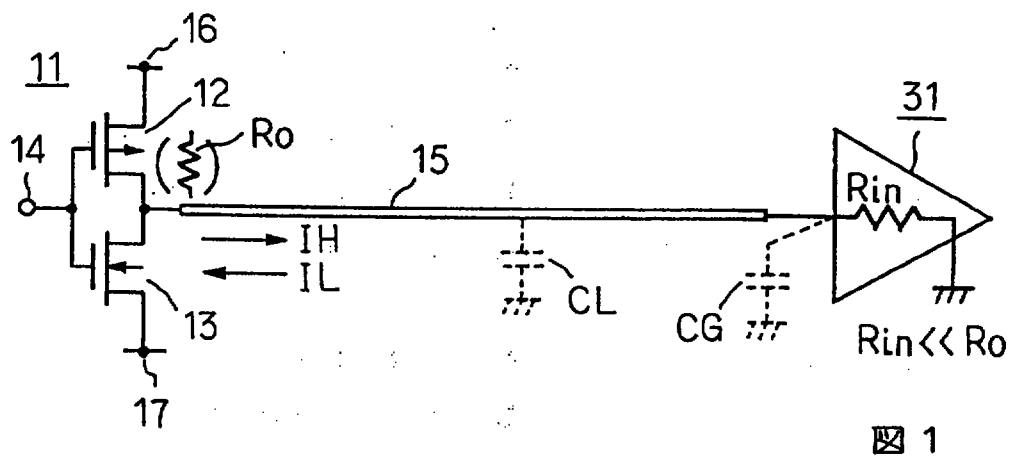


図 1

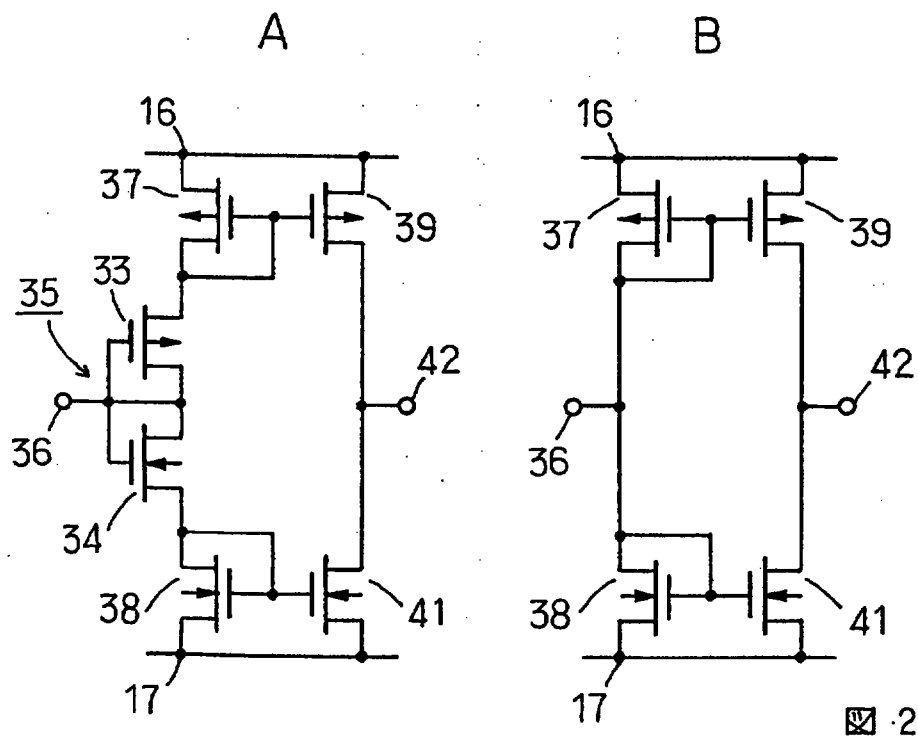
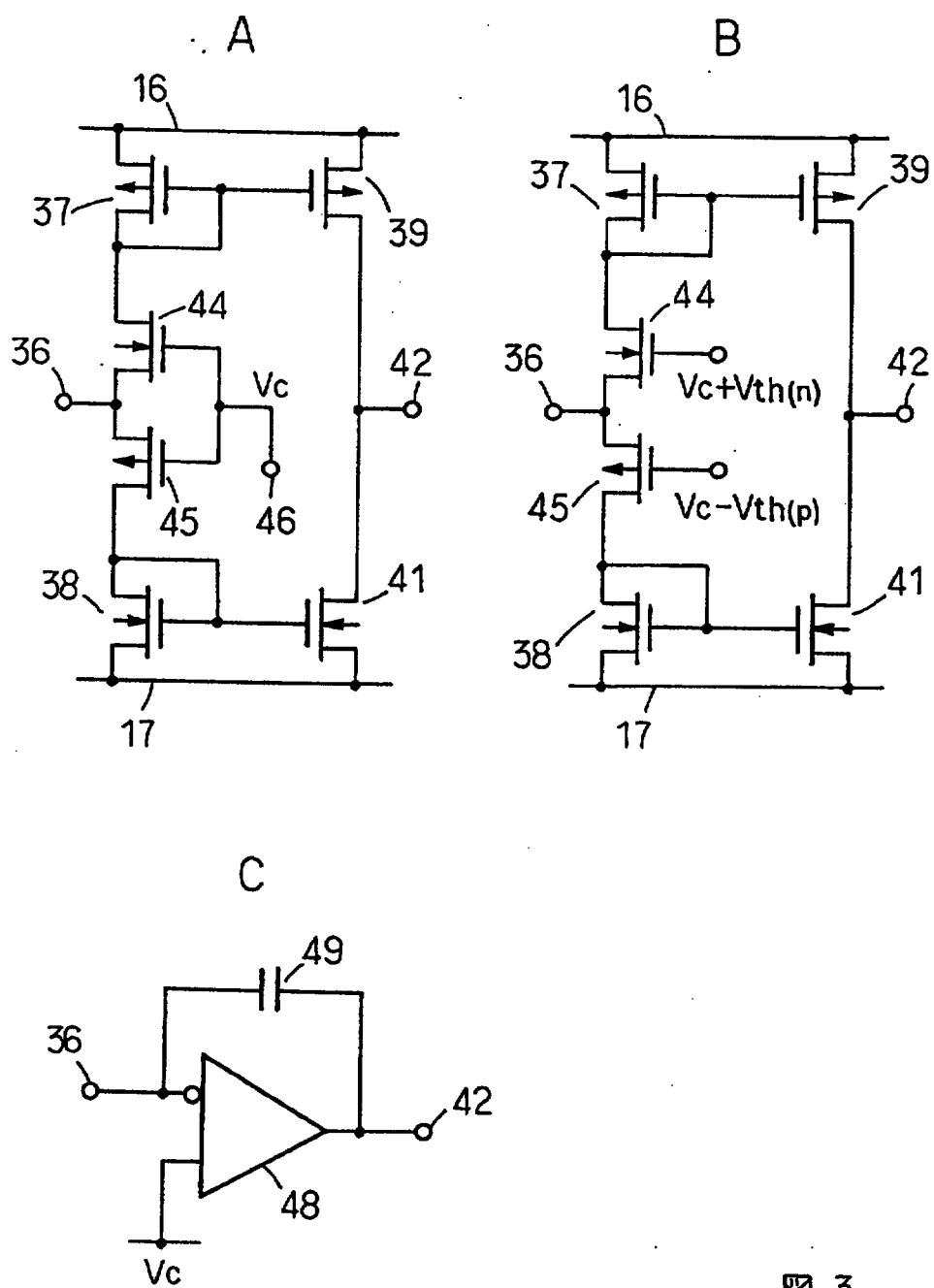


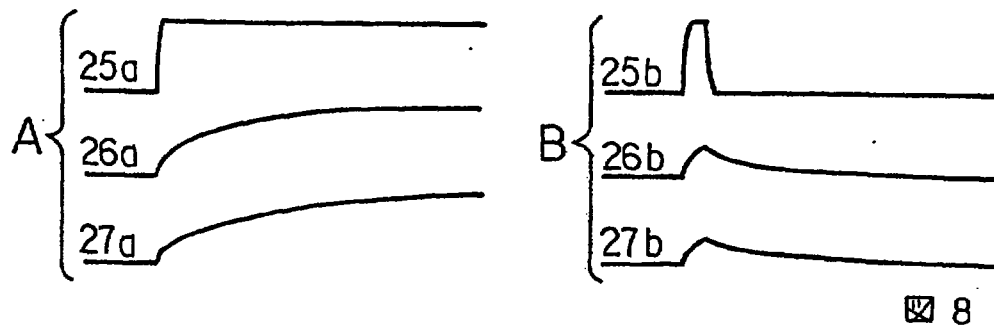
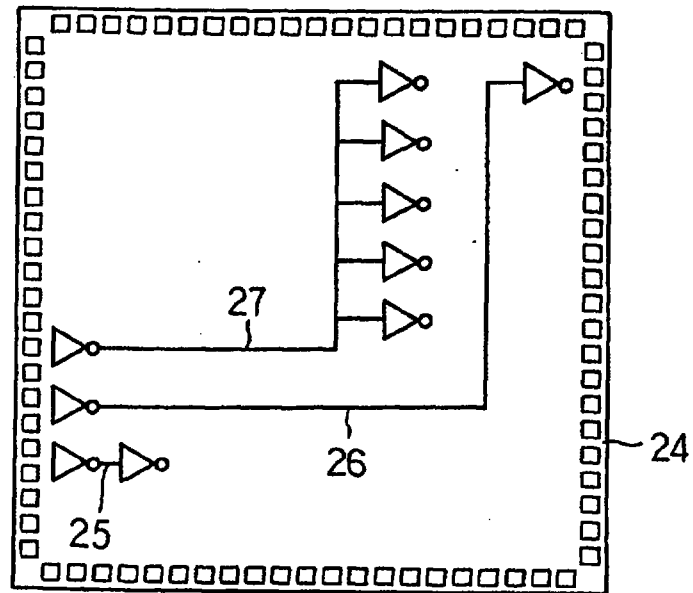
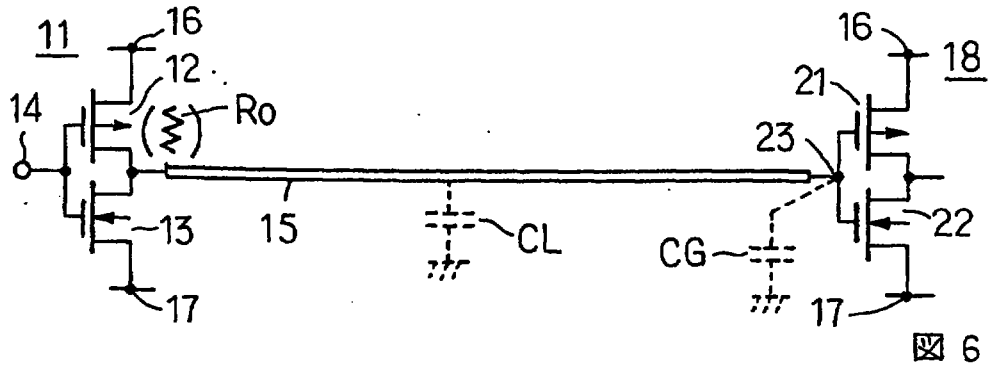
図 2

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☒ Description	: paged ...1... to paged ...25...
☐ Claim(s)	: paged ... to paged ...
☐ Drawing(s)	: paged ... to paged ...
☒ Abstract	: paged ...30... to paged ...30...

CMOS INTEGRATED CIRCUIT

TECHNICAL FIELD

The present invention relates to an integrated circuit
5 (IC) having a multiplicity of CMOSs (Complementary Metal-
Oxide Semiconductors) formed therein, and more particularly,
to an improvement in a signal transmission path or line in a
ULSI (Ultra-Large Scale Integrated Circuit) of CMOS.

10 BACKGROUND ART

As is well known, semiconductor elements, logical
circuits and the like formed as an LSI (Large Scale
Integrated Circuit) are electrically connected in a
predetermined manner by wiring. Likewise, in a ULSI having a
15 multiplicity of CMOSs formed therein, CMOSs, logical
circuits of CMOSs, and the like are electrically connected in
a predetermined manner by wiring. Such wiring may be often
formed by conductive paths or conductors of a predetermined
pattern formed, for example, on the surface of an integrated
20 circuit.

Fig. 6 shows an internal circuit of a conventional ULSI
of CMOSs. In this example, there is shown a case in which a
gate 11 of one CMOS at a transmitting side (hereinafter,
referred to as transmitting gate) and a gate 18 of one CMOS
25 at a receiving side (hereinafter, referred to as receiving
gate) are electrically connected through a signal
transmission path which is conductive path or conductor 15 in



this example. Both of the transmitting gate 11 and the receiving gate 18 are constituted, in this example, by CMOS inverters (each inverter is constituted by a CMOS), respectively.

5 The transmitting gate 11 comprises a p-channel MOS·FET (MOS Field Effect Transistor) 12 and a n-channel MOS·FET 13 in which both gates thereof are connected with each other and connected to an input terminal 14, both drains thereof are connected with each other and connected to one end (input
10 end) of the conductive path 15, source of the p-channel MOS·FET 12 is connected to a power supply terminal 16 of +VDD (a positive voltage), and source of the n-channel MOS·FET 13 is connected to a power supply terminal 17 of -VSS (a negative voltage). Source of the n-channel MOS·FET 13 may be
15 connected to a common electric potential point or ground potential point.

On the other hand, the receiving gate 18 comprises a p-channel MOS·FET 21 and a n-channel MOS·FET 22 in which both gates thereof are connected with each other and connected to
20 an input terminal 23, both drains thereof are connected with each other and connected to an output terminal (not shown), source of the p-channel MOS·FET 21 is connected to the power supply terminal 16 of +VDD, and source of the n-channel MOS·FET 22 is connected to the power supply terminal 17 of
25 -VSS. The other end (output end) of the conductive path 15 is connected to the input terminal 23.

In such circuit configuration, since there inevitably



exist a distributed capacity CL (shown by broken line) of the
conductive path 15 and an input capacity CG (also shown by
broken line) of the receiving gate 18, when a signal is
transmitted from the transmitting gate 11 to the receiving
gate 18 through the conductive path 15, the distributed
5 capacity CL of the conductive path 15 and the input capacity
CG of the receiving gate 18 will be charged by this signal.
Assuming that an equivalent output resistance of the
transmitting gate 11 is R_0 , the transition time in waveform
10 of a voltage inputted to the receiving gate 18 is equal to
 $R_0 \times (CL + CG)$.

In reality, the transition time is also affected by a
distributed resistance of the conductive path 15, but usually
the equivalent output resistance R_0 is dominative over this
15 distributed resistance and hence the influence of the
distributed resistance is omitted herein. In addition, the
equivalent output resistance R_0 has a nature of non-linearity
so that the resistance value can be varied with change of the
voltage. However, for clarity of the explanation, such
20 characteristic is ignored herein.

Recently, ICs are growing in density of integration and
degree of scale thereof higher and larger, and the size of an
IC chip is also increasing more and more. For example, as
shown in Fig. 7, there is not rare a ULSI in which the length
25 of one side of its chip 24 is longer than 15 mm. In such
large IC chip, wiring or conductive paths connecting
circuits, elements, and the like formed in the IC chip with



one another become long in their lengths, and there appears a conductive path which is longer than 20 mm. In an estimation of some ULSI, the number of conductive paths larger than 20 mm has become more than 5% of the total number of conductive paths.

Fig. 7 shows an example of the internal circuits of a conventional ULSI of CMOSs. It diagrammatically illustrates a multiplicity of gates, and wiring connecting therebetween, namely, conductive paths 25, 26 and 27. As shown, in addition to the conductive path 25 having a comparatively short length (200 μ m or so), there are the conductive path 26 being a very long (larger than 20 mm) and the conductive path 27 which is a very long (larger than 20 mm) and has a plurality of gates as its loads. Such conductive path 27 is used in distributing a clock signal or transmitting a bus signal, and these signals affect the whole performance (operation speed or rate) of the IC chip, namely, ULSI.

In Fig. 7, in case that a step waveform is transmitted from transmitting gates (three gates at left side in the drawing) to corresponding receiving gates through the respective conductive paths 25, 26 and 27, the input waveforms at the receiving gates are as shown in Fig. 8A by curves 25a, 26a and 27a, respectively, and in case that an impulse is transmitted from the transmitting gates to the corresponding receiving gates through the respective conductive paths 25, 26 and 27, the input waveforms at the receiving gates are as shown in Fig. 8B by curves 25b, 26b



and 27b, respectively. As is apparent from these waveforms, owing to that the longer conductive paths 26 and 27 have very long transition times respectively as compared with the short conductive path 25, the propagation delay-times of the
5 conductive paths 26 and 27 are remarkably long in respect to the step response thereof and in respect to the pulse response thereof, if the pulse width is short, the pulse is disappeared. As a result, a clock signal having a high frequency (a short repetitive period) cannot pass through a
10 conductive path of long distance. In other words, there is an important drawback that the performance (operation speed or rate) of the whole IC chip cannot be made high.

In addition, in order to increase the density of integration of an IC and to reduce the power consumption of
15 an IC more and more, miniaturization of a CMOS is growing and the operation speed of an unity gate is improved. However, the equivalent output resistance R_0 becomes high and the distributed capacity of wiring per unit length tends to rather increase than is unchanged. Consequently, the
20 transition time is further long, resulting in a shortcoming that the operation speed of the IC chip is limited more and more.

In view of such disadvantages, recently, in order to improve the throughput of wiring in an IC chip, a method of
25 transmitting a signal in an IC chip using light has been researched or studied. However, it is necessary that light emitting elements and light receiving elements of compound



semiconductors are formed on the surface of a silicon (Si) chip and that an optical waveguide is constituted separately of an electrical wiring layer. Therefore, it is difficult at present to implement such optical signal transmission method, and even if such method should be implemented, vast increases in size and cost are estimated.

DISCLOSURE OF THE INVENTION

An object of the present invention is to provide a large scale integrated circuit of CMOS structure in which a signal can be transmitted therein at high speed or rate.

In the present invention, in order to attain the above object, there is provided an integrated circuit of CMOS structure which is characterized in that a current-input type gate having a remarkably low input impedance is used as a gate at the receiving side in respect to a signal transmission path in the integrated circuit, the current-input type gate generating an output voltage depending upon the magnitude of an input current.

In a preferred embodiment, the current-input type gate has its input terminal which is connected to a positive power supply terminal through a first current Miller circuit constituted by p-channel MOS-FETs and connected to a negative power supply terminal through a second current Miller circuit constituted by n-channel MOS-FETs.

In a first modification, the current-input type gate further includes an inverter of CMOS structure the input end



and the output end of which are interconnected, and wherein the input end of the inverter is connected to the input terminal and respective ends of the inverter to be connected to power supply terminals are connected to the input side of the first current Miller circuit and the input side of the second current Miller circuit, respectively.

In a second modification, the current-input type gate is arranged such that the output end of the inverter of CMOS structure is connected to the input terminal, to the input end of the inverter is supplied with the mid point potential between the positive power supply voltage and the negative power supply voltage, and respective ends of the inverter to be connected to power supply terminals are connected to the input side of the first current Miller circuit and the input side of the second current Miller circuit, respectively.

In a third modification, the current-input type gate includes an n-channel MOS·FET inserted in series between the input terminal and the input side of the first current Miller circuit, and a p-channel MOS·FET inserted in series between the input terminal and the input side of the second current Miller circuit, and a potential of addition of the mid-point potential between the positive and negative power supply voltages to a threshold voltage of the n-channel MOS·FET is applied to gate of the n-channel MOS·FET, a potential of subtraction of a threshold voltage of the p-channel MOS·FET from the mid point potential between the positive and negative power supply voltages being applied to gate of the



p-channel MOS·FET.

In another preferred embodiment, the current-input type gate comprises a differential amplifier an inverting input end of which is connected to the input terminal, and a
5 negative feedback capacitor connected between the inverting input end and an output end of the differential amplifier, the mid point potential of an input logical signal being applied to a non-inverting input end of the differential amplifier.

10 In each of the embodiments and each of the modifications, a gate at the transmitting side in respect to the signal transmission path is a current-output type gate, and it is preferred that this current-output type gate is an inverter of CMOS structure.

15 In a further embodiment, the current-output type gate is a gate arranged such that an output end of an inverter of CMOS structure is grounded through a capacitor, respective ends of the inverter to be connected to power supplies are connected to a positive power supply terminal through a first
20 current Miller circuit constituted by p-channel MOS·FETs and connected to a negative power supply terminal through a second current Miller circuit constituted by n-channel MOS·FETs respectively, and the output ends of the first and second current Miller circuits are connected to the signal
25 transmission path. Further, a resistance element for maintaining a current may be connected in parallel with the capacitor.



According to the construction of the present invention as mentioned above, since a current-input type gate having a low impedance is used as a receiving gate, the wiring capacitance CL and the gate input capacitance CG can be rapidly charged, and hence the transition time of a signal is rendered remarkably short. As a result, it is possible that even a clock signal having a high frequency (short repetitive period) passes through a long conductive path in the CMOS-IC, and so the performance (operation speed or rate) of the whole CMOS-IC chip can be made high.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram showing an internal circuit of a first embodiment of the large scale integrated circuit of CMOS structure according to the present invention;

Figs. 2A and 2B are schematic diagrams showing two electric circuits of the charge responsive type gate shown in Fig. 1, respectively;

Fig. 3A, 3B and 3C are schematic diagrams showing three electric circuits of the charge responsive type gate in which a steady-state current can be zero;

Fig. 4 is a schematic diagram showing an internal circuit of a second embodiment of the large scale integrated circuit of CMOS structure according to the present invention;

Fig. 5 is a block diagram showing an internal circuit of a third embodiment of the large scale integrated circuit of CMOS structure according to the present invention;



Fig. 6 a schematic diagram showing an example of the internal circuits of a conventional large scale integrated circuit of CMOS structure;

Fig. 7 is a diagrammatical illustration showing signal transmission paths of various lengths in a conventional large scale integrated circuit of CMOS structure; and

Figs. 8A and 8B are waveforms showing responses of a receiving gate when a step waveform and an impulse are transmitted through the transmission paths of various lengths shown in Fig. 7, respectively.

BEST MODES FOR CARRYING OUT THE INVENTION

Now, some embodiments of the present invention will be described in detail with reference to Figs. 1 to 5.

Fig. 1 shows an internal circuit of the first embodiment of the large scale integrated circuit of CMOS structure according to the present invention. In the following, portions and elements in Figs. 1 to 5 corresponding to those in Fig. 6 are denoted by the same reference characters as those in Fig. 6, and the explanations thereof are omitted unless necessary.

In the first embodiment, a transmitting gate 11 is also constituted as an inverter comprising a p-channel MOS-FET 12 and an n-channel MOS-FET 13, and has the same configuration as that of the conventional transmitting gate 11 shown in Fig. 6. Accordingly, the explanation thereof is omitted.

A receiving gate 31 connected to the output end of a



conductive path or conductor (signal transmission path) 15 is constituted as a gate 31 which is of a current-input type and having a low input impedance (hereinafter, referred to as charge responsive type gate). The input impedance R_{in} of this charge responsive type gate 31 is sufficiently low as compared to the equivalent output resistance R_0 of the transmitting gate 11. As a result, the charge responsive type gate 31 acts to make the amplitude of an input voltage substantially zero and hence to make a current flowing in the load capacitance substantially zero thereby generating an output voltage depending on an input current.

An example of the circuit diagrams of the charge responsive type gate 31 is shown in Fig. 2A. This charge responsive type gate 31 comprises an inverter 35 constituted by a p-channel MOS-FET 33 and an n-channel MOS-FET 34, a p-channel MOS-FET 37 connected between source of the p-channel MOS-FET 33 and a power supply terminal 16 of +VDD, an n-channel MOS-FET 38 connected between source of the n-channel MOS-FET 34 and a power supply terminal 17 of -VSS or ground potential terminal, and a p-channel MOS-FET 39 and an n-channel MOS-FET 41 connected in their gates to gates of the MOS-FETs 37 and 38 respectively.

The input end (gates connected in common) and the output end (drains connected in common) of the inverter 35 are interconnected and are connected to an input terminal 36. Source of the p-channel MOS-FET 33 is connected to the power supply terminal 16 of +VDD through drain-source of the p-



channel MOS-FET 37, and source of the n-channel MOS-FET 34 is connected to the power supply terminal 17 of -VSS or ground potential terminal through drain-source of the n-channel MOS-FET 38. Drain and gate of the MOS-FET 37 are
5 interconnected, and also drain and gate of the MOS-FET 38 are interconnected. Drains of the MOS-FET 39 and 41 are interconnected and are connected to an output terminal 42, and sources thereof are connected to the power supply terminals 16 and 17, respectively. In other words, both ends
10 of the inverter 35 to be connected to power sources are connected to input sides of a current Miller circuit constituted by the p-channel MOS-FETs 37, 39 and a current Miller circuit constituted by the n-channel MOS-FETs 38, 41 respectively.

15 In accordance with the arrangement discussed above, since the input end and the output end of the inverter 35 are short-circuited, the impedance R_{in} as has seen from the input terminal 36 is very low, and the potential of the input terminal 36 comes to substantially one at the mid point of
20 +VDD and -VSS (or 0 V). That is, the potential of the input terminal 36 becomes the threshold voltage of the inverter 35, namely, the input voltage by which the output logic of the inverter 35 is inverted, and both the MOS-FETs 33 and 34 are self-biased in between drain and source of each of them by
25 this threshold voltage, respectively.

As described above, since the potential of the input terminal 36 is one by which the inverter 35 is inverted, the



impedance between drain and source of each of the MOS-FETs 33 and 34 is remarkably low, and the impedance of the input terminal 36 is a value of parallel connected impedances between drains and sources of the MOS-FETs 33 and 34 and hence is the lowest value. In addition, due to the effect of the negative feedback, the impedance of the input terminal 36 is further lowered, and yet, if it will depart from the lowest impedance point, an action exerts thereon for returning back to the lowest impedance point.

Moreover, the MOS-FETs 37 and 39 form a current Miller circuit and also the MOS-FETs 38 and 41 form a current Miller circuit. The input impedance of the current Miller circuit of the MOS-FETs 37 and 39, namely, the impedance of drain of the MOS-FET 37 is set to be equal to the input impedance of the current Miller circuit of the MOS-FETs 38 and 41, namely, the impedance of drain of the MOS-FET 38. In addition, it is designed that ratio of beta (β) of the FET 33 to that of the FET 34 is 1:1 and the threshold voltages of both the FETs 33 and 34 are equal to each other. Consequently, the voltage of the input terminal 36 just becomes the mid point of the power supply voltages +VDD and -VSS.

Further, the illustrated gate circuit has a steady-state current flow passing through the FETs 33, 34, 37 and 38 even if the input of the gate circuit is open. Therefore, in view of reducing the power consumption, it is desired that sizes of the FETs 33, 34, 37 and 38, that is, gate widths thereof are decreased. In practice, the gate widths of the FETs 33,



34, 37 and 38 are determined based on a trade-off between the power consumption and the operation speed or rate.

A current flowing from the transmitting gate 11 to the input terminal 36 all of it passes through the FET 37 or 38 of the current Miller circuit and hence the impedance as seen from the FET 33 or 34 toward the FET 37 or 38 is very low because of the current input. In this case, when a current flows from the transmitting gate 11 toward the input terminal 36 (see IH in Fig. 1), it flows through the FET 38, and when a current flows from the input terminal 36 toward the transmitting gate 11 (see IL in Fig. 1), it flows through the FET 37. At that time, a current flows through the FET 39 or 41 and a difference between the current flows through the FET 39 and the FET 41 is proportional to the difference between the current flows through the FET 37 and the FET 38. In case the current flow through the FET 39 is larger than that through the FET 41, the potential of the output terminal 42 rises to about +VDD. On the contrary, in case the current flow through the FET 41 is larger than that through the FET 39, the potential of the output terminal 42 falls to about -VSS.

Since the charge responsive type gate 31 shown in Fig. 1 has a remarkably low input impedance R_{in} as described above, the distributed capacity C_L of the conductive path 15 (wiring capacitance) and the input capacity C_G of the gate 31 are both in substantially short-circuited state by such very low input impedance of the gate 31. As a result, it is hardly



necessary that a signal outputted from the transmitting gate 11 charges the wiring capacitance CL and the gate input capacitance CG, and the transition time is very short. In other words, a change of the signal outputted from the transmitting gate 11 is transmitted to the input terminal 36 of the receiving gate 31 at high speed. In addition, if the output of the transmitting gate 11 comes to a high level, in the example shown in Fig. 2A, the potential of the output terminal 42 of the receiving gate 31 reaches about -VSS, and if the output of the transmitting gate 11 comes to a low level, the potential of the output terminal 42 of the receiving gate 31 reaches about +VDD. Accordingly, the output of the transmitting gate 11 is inverted and the inverted output appears at the output terminal 42 of the receiving gate 31.

As the charge responsive type gate 31, a gate as shown in Fig. 2B may be used wherein the inverter 35 shown in Fig. 2A is omitted and the input terminal 36 is directly connected to drain of the FET 37 and drain of the FET 38. In this first modification of the charge responsive type gate 31, the potential of the input terminal 36 becomes a potential at the mid point between +VDD and -VSS and it is a current input to both the current Miller circuits, and therefore the input impedance is low. As a result, similar functional effects to the charge responsive type gate circuit shown in Fig. 2A can be obtained. In this case, the input impedance of the charge responsive type gate circuit shown in Fig. 2B is higher than



that of the charge responsive type gate circuit shown in Fig. 2A and also a current flowing through the FETs in steady-state in Fig. 2B is larger than that in Fig. 2A. However, an advantage is obtained from the charge responsive type gate circuit of Fig. 2B that the number of elements, namely, FETs is smaller than that of the charge responsive type gate circuit of Fig. 2A.

Fig. 3A shows a second modification of the charge responsive type gate 31. This second modification includes an n-channel MOS-FET 44 and a p-channel MOS-FET 45 in place of the inverter 35 in Fig. 2A, and is arranged such that sources of the MOS-FETs 44 and 35 are connected to the input terminal 36, gates thereof are connected to a terminal 46, drains thereof are connected to corresponding drains of the MOS-FETs 37 and 38 respectively, and a potential V_c at the mid point between the power supply terminal 16 of +VDD and the power supply terminal 17 of -VSS is applied to the terminal 46.

In the above circuit configuration, if the potential of the input terminal 36 is within limits of $V_c \pm V_{th}$ (V_{th} is a threshold voltage of each of the FETs 44 and 45), no source current flows through the FETs 44 and 45, and hence the input impedance becomes high. In case the input of the gate is open, any steady-state current does not flow through the FETs 44 and 45.

If the input voltage of the input terminal 36 is even slightly out of the limits of $V_c \pm V_{th}$, the FET 44 or 45



becomes conductive, and in response thereto, the output voltage of the output terminal 42 approaches +VDD or -VSS. Since there are many cases that V_{th} is set to 10% or so of the power supply voltage, the amplitude of the voltage at the input terminal 36 will come to 20% or so of the power supply voltage. If the amplitude of the voltage is of such value, an operation of sufficiently high speed or rate is usually expected. More particularly, it is possible to make the amplitude of an input voltage a small value of about $2V_{th}$, and so a signal can be transmitted without being greatly affected by the wiring capacitance C_L and the gate input capacitance C_G . In other words, the transition time can be remarkably shorted as compared to the prior art. Further, in practice, V_{th} differs between a p-channel MOS-FET and an n-channel MOS-FET. For the purpose of easy understanding, it is assumed here that V_{th} of a p-channel MOS-FET is equal to that of an n-channel MOS-FET.

If it is desired to make a steady-state current flow zero and to make the amplitude of the voltage at the input terminal 36 smaller, as shown in Fig. 3B, gates of the FETs 44 and 45 are disconnected from each other and gate of the FET 44 is supplied with $V_c + V_{th}(n)$ ($V_{th}(n)$ is a threshold voltage of the n-channel FET 44) and gate of the FET 45 is supplied with $V_c - V_{th}(p)$ ($V_{th}(p)$ is a threshold voltage of the p-channel FET 45). In this state, since the FET 44 has its gate supplied with $V_c + V_{th}(n)$ and the FET 45 has its gate supplied with $V_c - V_{th}(p)$, if the potential of the input



terminal 36 should be lowered even slightly below V_c , a current flows through the FET 44. On the contrary, if the potential of the input terminal 36 should be increased even slightly over V_c , a current flows through the FET 45.

5 As the charge responsive type gate 31, a gate as shown in Fig. 3C may be used wherein an inverting input terminal of a differential amplifier 48 is connected to the input terminal 36, its output terminal is connected to the output terminal 42, a negative feedback capacitor 49 is connected between the
10 output terminal and the inverting input terminal of the amplifier 48, and the mid point voltage V_c is applied to a non-inverting input terminal of the amplifier 48, the differential amplifier 48 having high gain and wide or broad band and operating at high speed or rate.

15 This differential amplifier 48 integrates a current flowing into the input terminal 36, and outputs an output voltage which is proportional to the integrated value and is inverted in polarity. As a result, if the potential at the input terminal 36 should rise even slightly over V_c , a rapid
20 charge of the capacitor 49 is effected by a negative feedback current so as to cancel the difference between the potential of the input terminal 36 and V_c so that the output voltage at the output terminal 42 is lowered. On the other hand, if the potential at the input terminal 36 should fall even slightly
25 below V_c , a rapid charge of the capacitor 49 is effected by a negative feedback current having the inverted polarity so as to cancel the difference between the potential of the input



terminal 36 and V_c so that the output voltage at the output terminal 42 is increased. Accordingly, the potential at the input terminal 36 is maintained at V_c and the input impedance becomes substantially zero.

5 As described above, since the differential amplifier 48 has high gain and operates in wide-band, and moreover the input impedance comes to substantially zero, it can rapidly integrate an input current supplied to the input terminal 36. Therefore, the wiring capacitance C_L and the gate input
10 capacitance C_G are quickly charged and the transition time is rendered very short so that high speed operation can be performed. Further, in order to meet the range of input voltage of the succeeding stage, a circuit for limiting the amplitude of the output voltage may be connected to the
15 output terminal 42, if necessary.

 The charge responsive type gates 31 shown in Figs. 2A and 2B always consume the power. In case the transmitting gate 11 is of the type in which it outputs only a transient current, the current contributing to a signal transmission is
20 only a transient current flowing in transition of a signal, and hence it is much preferred to arrange such that only the transient current flows.

 Fig. 4 shows an internal circuit of the second embodiment of the large scale integrated circuit of CMOS structure
25 according to the present invention, and illustrates a case arranged to flow only a transient current.

 In the second embodiment, as the transmitting gate 11, a



gate is used which has its circuit configuration similar to that of the charge responsive type gate 31 that is the receiving gate shown in Fig. 2A. This transmitting gate 11 comprises an inverter 53 constituted by a p-channel MOS·FET 51 and an n-channel MOS·FET 52, a p-channel MOS·FET 55 connected between source of the p-channel MOS·FET 51 and a power supply (positive potential) terminal 16 of +VDD, an n-channel MOS·FET 56 connected between source of the n-channel MOS·FET 52 and a power supply (negative potential) terminal 17 of -VSS or ground or common potential terminal, and a p-channel MOS·FET 57 and an n-channel MOS·FET 58 connected in their gates to gates of the MOS·FETs 55 and 56 respectively.

The input end, namely, gates connected in common of the inverter 53 are connected to the input terminal 14 and the output end, namely drains connected in common of the inverter 53 are connected to the common potential point or ground potential point through a capacitor 54. Source of the p-channel MOS·FET 51 is connected to the power supply terminal 16 of +VDD through drain-source of the p-channel MOS·FET 55, and source of the n-channel MOS·FET 52 is connected to the power supply terminal 17 of -VSS through drain-source of the n-channel MOS·FET 56. Drain and gate of the MOS·FET 55 are interconnected, and also drain and gate of the MOS·FET 56 are interconnected. Drains of the MOS·FET 57 and 58 are interconnected and are connected to the input end of the conductive path 15, and sources thereof are connected to the power supply terminals 16 and 17, respectively. In other



words, in this second embodiment, both ends of the inverter 53 to be connected to power sources are also connected to input sides of a current Miller circuit constituted by the p-channel MOS-FETs 55, 57 and a current Miller circuit
5 constituted by the n-channel MOS-FETs 56, 58 respectively.

Thus, it will be understood that the construction of this transmitting gate is the same as that of the charge responsive type gate 31 shown in Fig. 2A except that the input and output ends of the inverter 35 are not connected in
10 common, and in place thereof, only the input end is connected to input terminal 36 and the output end is connected to the common potential or ground potential point through the capacitor 54.

In the above circuit configuration, when the potential at
15 the input terminal 14 becomes a higher level than V_c of the mid point potential between the power supply voltages $+V_{DD}$ and $-V_{SS}$, a current flows through the FET 52 so that the capacitor 54 is charged with its electrode connected to the FET 52 being negative. The current signal is multiplied by
20 the current Miller circuit constituted by the FETs 56 and 58 thereby generating a transient current on the conductive path 15, which acts to draw a current (I_L) from the receiving gate 31. When the transition time of this current signal ends, the current through the FETs of the transmitting gate comes
25 to zero so that no steady-state power consumption occurs in the transmitting gate.

When the potential at the input terminal 14 is lowered



below V_c , a current flows through the FET 51 so that the capacitor 54 is charged with its electrode connected to the FET 51 being positive. The current signal is multiplied by the current Miller circuit constituted by the FETs 55 and 57
5 thereby supplying a current (I_H) to the conductive path 15, which flows toward the receiving gate 31 through the conductive path 15. In this case, when the transition time of this current signal ends, the current through the FETs of the transmitting gate also comes to zero so that no steady-
10 state power consumption occurs in the transmitting gate.

Even in the case the transmitting gate 11 is used which is arranged such that a current flows only during the transition time of a signal as discussed above, if a gate of the type in which a steady-state current flows through the
15 gate, as shown in Figs. 2A and 2B, is used as the receiving charge responsive type gate 31, electric charges stored in the wiring capacitance C_L and the gate input capacitance C_G are discharged so that the signal output state of the receiving gate 11 cannot be maintained when the interval
20 between successive transitions of the signal on the input terminal 14 is long (the time duration in which no current flows at all is long).

In such case, as shown in Fig. 4 by dotted lines, a resistance element (or an FET acting as a resistance element)
25 61 may be connected in parallel with the capacitor 54 to flow a minute current through the resistance element 61 for maintaining the charged potentials of the capacitances,



thereby to retain the signal output state corresponding to the signal input state of the input terminal 14 in respect to the conductive path 15. This resistance element 61 may be one through which a minimum current can flow so that the
5 signal output state can be retained in any time duration other than the transition time.

In case a gate of the type in which any steady-state current or any leakage current does not flow through the gate, as shown in Figs. 3A and 3B, is used as the receiving
10 charge responsive type gate 31, the transmitting gate shown in Fig. 4 can be used. However, if it is difficult to retain the input potential of the charge responsive type gate 31 stationarily for a long time due to the existence of a minute leakage current, as previously mentioned, a resistance
15 element is connected in parallel with the capacitor 54 in case a signal to be transmitted does not change for a long time.

In case the charge responsive type gate shown in Fig. 3C is used as the receiving charge responsive type gate 31, it
20 is unnecessary in this case to connect a resistance element in parallel with the capacitor 54 so that a current can flow through the resistance element for maintaining the charged potentials of the capacitances except a case that a signal to be transmitted does not change for a long time, though it is
25 depending upon the input leakage current of the differential amplifier 48.

Further, in case a gate of the type in which a steady-



state current flows through the gate, as shown in Fig. 1, is used as the transmitting charge responsive type gate 11, any one of the charge responsive type gates can be used. In case of transmitting a signal the transition of which always occurs at high rate or speed such as a clock signal, if the transmitting gate shown in Fig. 4 is used, any one of the charge responsive type gates shown in Figs. 2A and 2B, and Figs. 3A, 3B and 3C may be provided at the receiving side.

Since the transmitting gate 11 is a current-output type gate and the receiving gate 31 is a charge responsive type gate, namely, a current-input type gate, it can be easily implemented that, as shown in Fig. 5 for example, a plurality of transmitting current-output type gates 63 are connected to the conductive path 15, and in addition, a plurality of receiving current-input type gates 64 are connected to the conductive path 15 thereby using the conductive path 15 as a bus. Particularly, if as the current-output type gate 63 is used the transition current output gate which outputs a current only during the transition time as shown in Fig. 4 and as the current-input type gate 64 is used the charge responsive type gate through which no steady-state current flows as shown in Figs. 3A and 3B, no current flows through the conductive path 15 in the steady-state, and hence it is not required to set the current-output type gate 63 in high impedance state (inhibit state). Consequently, the control circuit and the control of timing therefor are not needed.

As described above, in accordance with the present



invention, since a current-input type gate having a low impedance is used as a receiving gate, the wiring capacitance C_L and the gate input capacitance C_G can be quickly charged, and hence the transition time of a signal is rendered

5 remarkably short. As a result, it is possible that even a clock signal having a high frequency (short repetitive period) passes through a long conductive path in the CMOS-IC, and so the performance (operation speed or rate) of the whole CMOS-IC chip can be made high. In particular, the power

10 consumption can be reduced to minimum by using, as a transmitting gate, a gate which outputs a current flow only during the transition time of a signal and, as a receiving gate, a gate through which no steady-state current flows.





WHAT IS CLAIMED IS:

1. An integrated circuit of CMOS structure being characterized in that a current-input type gate having a remarkably low input impedance is used as a gate at the receiving side in respect to a signal transmission path in said integrated circuit, said current-input type gate generating an output voltage depending upon the magnitude of an input current.
2. The integrated circuit of CMOS structure according to claim 1, wherein said current-input type gate has its input terminal which is connected to a positive power supply terminal through a first current Miller circuit constituted by p-channel MOS-FETs and connected to a negative power supply terminal through a second current Miller circuit constituted by n-channel MOS-FETs.
3. The integrated circuit of CMOS structure according to claim 2, wherein said current-input type gate further includes an inverter of CMOS structure the input end and the output end of which are interconnected, and wherein the input end of said inverter is connected to said input terminal and respective ends of said inverter to be connected to power supply terminals are connected to the input side of said first current Miller circuit and the input side of said second current Miller circuit, respectively.

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4. The integrated circuit of CMOS structure according to claim 2, wherein the output end of said inverter of CMOS structure is connected to said input terminal, to the input end of said inverter is supplied with the mid point potential between the positive power supply voltage and the negative power supply voltage, and respective ends of said inverter to be connected to power supply terminals are connected to the input side of said first current Miller circuit and the input side of said second current Miller circuit, respectively.

5. The integrated circuit of CMOS structure according to claim 2, wherein an n-channel MOS·FET is inserted in series between said input terminal and the input side of said first current Miller circuit, a potential of addition of the mid point potential between said positive and negative power supply voltages to a threshold voltage of said n-channel MOS·FET is applied to gate of said n-channel MOS·FET, a p-channel MOS·FET is inserted in series between said input terminal and the input side of said second current Miller circuit, and a potential of subtraction of a threshold voltage of said p-channel MOS·FET from said mid point potential between said positive and negative power supply voltages is applied to gate of said p-channel MOS·FET.

6. The integrated circuit of CMOS structure according to claim 1, wherein said current-input type gate comprises a differential amplifier an inverting input end of which is





connected to said input terminal, and a negative feedback capacitor connected between said inverting input end and an output end of said differential amplifier, the mid point potential of an input logical signal being applied to a non-inverting input end of said differential amplifier.

7. The integrated circuit of CMOS structure according to any one of claims 1 to 6, wherein a gate at the transmitting side in respect to said signal transmission path is a current-output type gate.

8. The integrated circuit of CMOS structure according to claim 7, wherein said current-output type gate is an inverter of CMOS structure.

9. The integrated circuit of CMOS structure according to claim 7, wherein said current-output type gate is a gate arranged such that an output end of an inverter of CMOS structure is grounded through a capacitor, respective ends of said inverter to be connected to power supplies are connected to a positive power supply terminal through a first current Miller circuit constituted by p-channel MOS-FETs and connected to a negative power supply terminal through a second current Miller circuit constituted by n-channel MOS-FETs respectively, and the output ends of said first and second current Miller circuits are connected to said signal transmission path.





10. The integrated circuit of CMOS structure according to claim 79, wherein a resistance element for maintaining a current is connected in parallel with said capacitor.

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ABSTRACT

In a ultra-large scale integrated circuit of CMOS structure, high speed operation can be performed without being affected by the wiring capacitance and the gate input capacitance. A current-output type gate is used as a transmitting gate 11, and a capacitor 54 is charged or discharged only during the transition time of a signal. The charge or discharge current is multiplied by current Miller circuits 55, 56 to supply the current to a conductive path 15. A current-input type gate is used as a receiving gate 31. This gate 31 is arranged such that the output and input ends of an inverter 35 of CMOS structure are interconnected, respective ends of the inverter to be connected to power supplies are connected to a positive power supply terminal 16 through the current Miller circuit of p-channel MOS-FETs 37, 39 and connected to a negative power supply terminal 17 through the current Miller circuit of n-channel MOS-FETs 38, 41 respectively, and the output ends of both the current Miller circuits are connected to the signal transmission path 15.



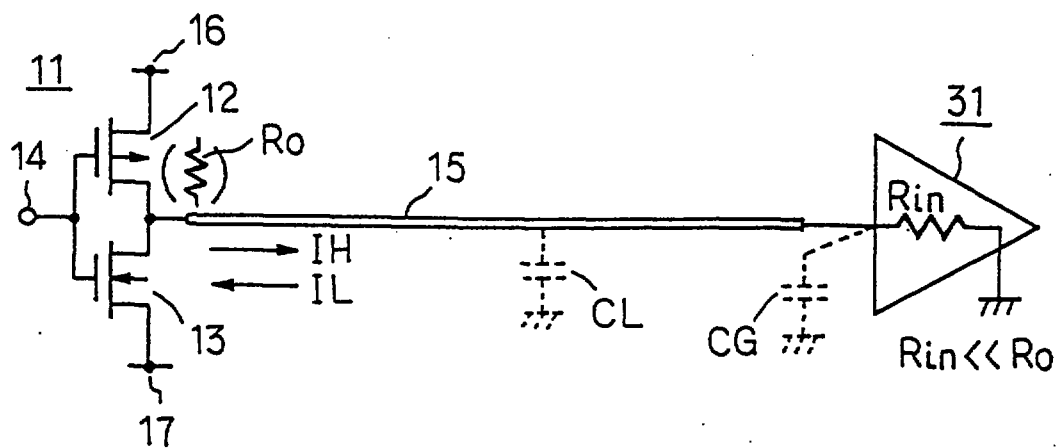


FIG. 1

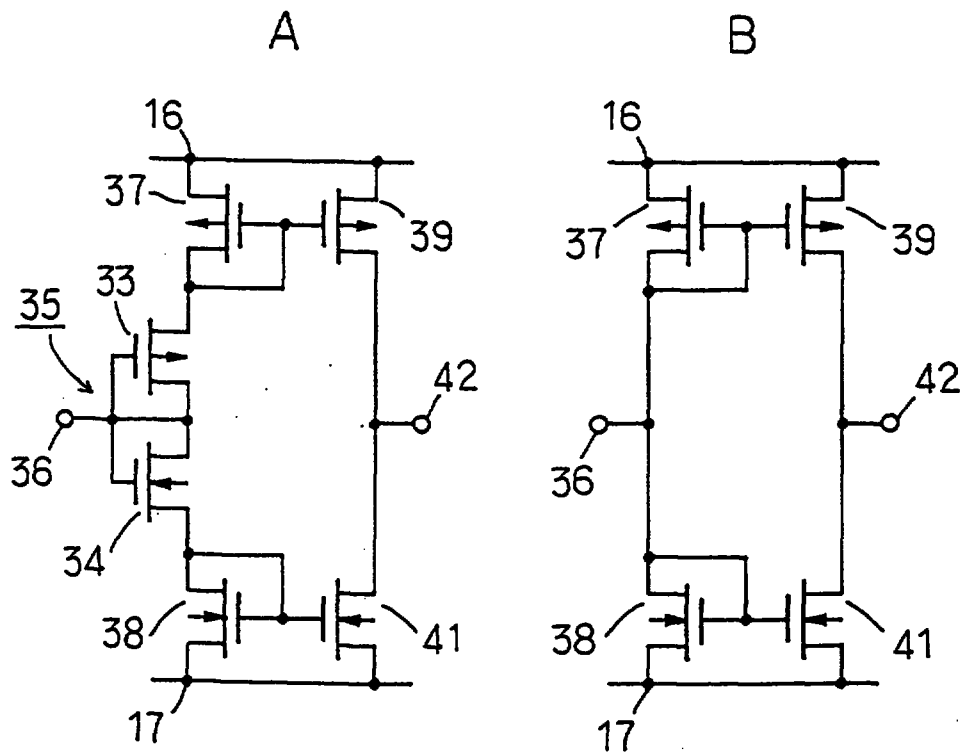


FIG. 2



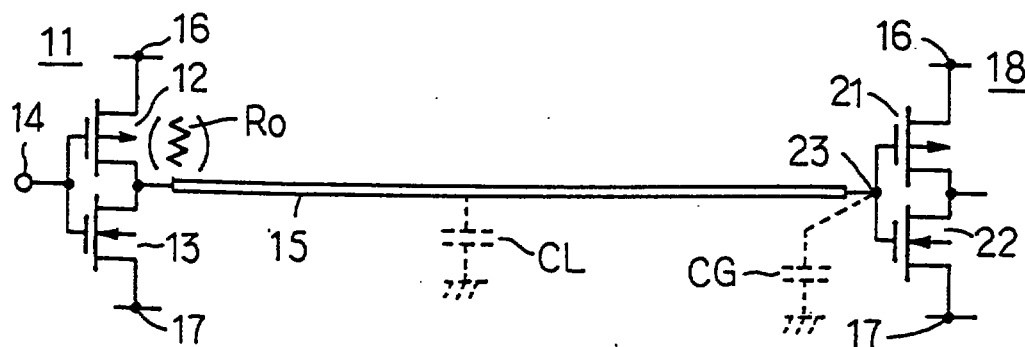


FIG. 6

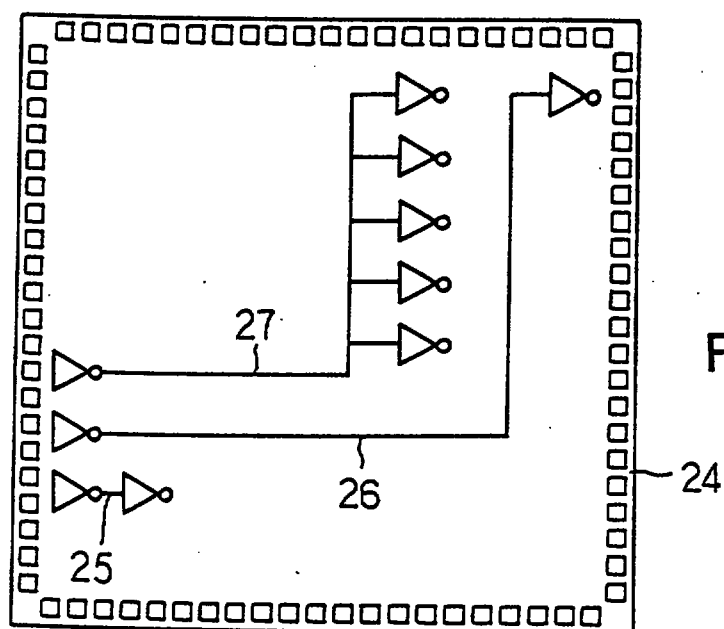


FIG. 7

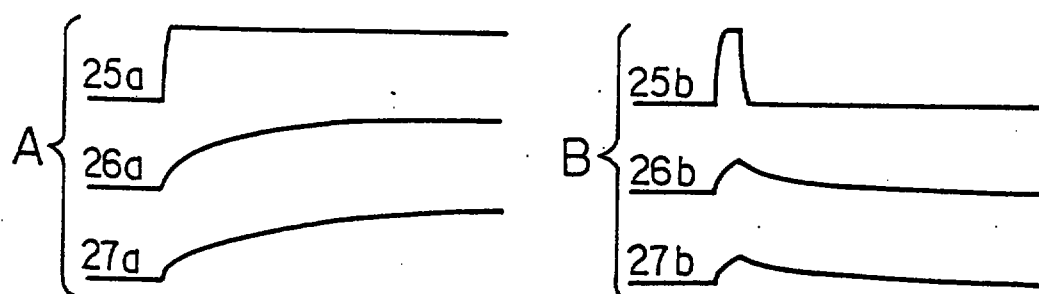


FIG. 8



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THE CLAIMS

1. An integrated circuit of CMOS structure capable of transmitting an input signal to be transmitted from a transmitting side through a signal transmission path to a receiving side at high speed, said integrated circuit being characterized in that
 a current-input type gate having a remarkably low input impedance is used as a receiving gate at the receiving side in respect to said signal transmission path in said integrated circuit, said current-input type gate having a low input impedance in comparison to an equivalent output resistance of the transmitting side whereby generating an output signal a voltage magnitude of which is depending upon a current magnitude of said input signal.

2. The integrated circuit of CMOS structure according to claim 1, wherein said current-input type gate has its input terminal which is connected to a positive power supply terminal through a first current mirror circuit constituted by first and second p-channel MOS FETs and connected to a negative power supply terminal through a second current mirror circuit constituted by first and second n-channel MOS FETs.



3. The integrated circuit of CMOS structure according to claim 2, wherein said current-input type gate further includes a first inverter of CMOS structure input end and output end of

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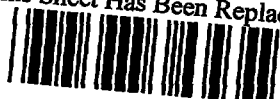
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which are interconnected, and wherein the input end of said inverter is connected to said input terminal and respective source electrodes of said inverter which are to be connected to the power supply terminals are connected to input side of said first current mirror circuit and input side of said second current mirror circuit, respectively.

4. The integrated circuit of CMOS structure according to claim 2, wherein output end of said inverter of CMOS structure is connected to said input terminal, input end of said inverter is supplied with a mid point potential between a positive power supply voltage and a negative power supply voltage, and respective source electrodes of said inverter which are to be connected to the power supply terminals are connected to input side of said first current mirror circuit and input side of said second current mirror circuit, respectively.

5. The integrated circuit of CMOS structure according to claim 2, wherein an n-channel MOS-FET is inserted in series between said input terminal and the input side of said first current mirror circuit, a potential of addition of a mid point potential between said positive and negative power supply voltages to a threshold voltage of said n-channel MOS-FET is applied to gate of said n-channel MOS-FET, a p-channel MOS-FET is inserted in series between said input terminal and the input side of said second current mirror circuit, and a potential of subtraction of a threshold voltage of said p-channel MOS-FET from said mid point potential





between said positive and negative power supply voltages is applied to gate of said p-channel MOS-FET.

6. The integrated circuit of CMOS structure according to claim 1, wherein said current-input type gate comprises a differential amplifier an inverting input end of which is connected to said input terminal, and a negative feedback capacitor connected between said inverting input end and an output end of said differential amplifier, a mid point potential between said positive and negative power supply voltages being applied to a non-inverting input end of said differential amplifier.

7. The integrated circuit of CMOS structure according to any one of claims 1 to 6, wherein a gate at the transmitting side in respect to said signal transmission path is a current-output type gate.

8. The integrated circuit of CMOS structure according to claim 7, wherein said current-output type gate is a second inverter of CMOS structure.

9. The integrated circuit of CMOS structure according to claim 7, wherein said current-output type gate is a gate arranged such that an output end of the second inverter of CMOS structure is grounded through a capacitor, respective source electrodes of said second inverter which are to be connected to power supply terminals are connected to a positive power supply terminal through a first current mirror circuit constituted by p-channel



MOS-FETs and connected to a negative power supply terminal through a second current mirror circuit constituted by n-channel MOS-FETs respectively, and output ends of said first and second current mirror circuits are connected to said signal transmission path.

10. The integrated circuit of CMOS structure according to claim 9, wherein a resistance element for maintaining a current is connected in parallel with said capacitor.

11. An integrated circuit of CMOS structure capable of transmitting an input signal to be transmitted from a transmitting side to a receiving side at high speed comprising:

a transmitting gate of CMOS structure provided in the transmitting side;

a receiving gate of CMOS structure provided in the receiving side; and

a signal transmission path provided between the transmitting gate and the receiving gate and having a substantial length with a distributed capacitance; wherein

said transmitting gate is capable of supplying said input signal to be transmitted to the signal transmission path,

said receiving gate receives said input signal of the transmitting gate from the transmission path and

said receiving gate is formed of a current-input type gate having a low input impedance in comparison to an equivalent output





resistance of the transmitting gate and capable of making a voltage magnitude of the thus received input signal substantially zero and hence making a current magnitude flowing in a load capacitance including the distributed capacitance substantially zero to thereby issue an output signal a voltage magnitude of which is responsive to a current magnitude of said input signal.

12. The integrated circuit of CMOS structure according to claim 11, wherein said current-input type gate comprises:

- an input terminal connected to the transmission path;

- an output terminal from which said output signal is derived;

- a first current mirror circuit having input and output ends and constituted by first and second p-channel MOS-FETs in such a manner that

 - source electrodes of the first and second p-channel MOS-FETs are connected to a positive power supply terminal, respectively,

 - gate electrodes of the first and second p-channel MOS-FETs are connected together to form the input end of the first current mirror circuit and also connected to a drain electrode of the first p-channel MOS-FET as well as the input terminal, and

 - a drain electrode of the second p-channel MOS-FET, which forms the output end of the first current mirror circuit, is connected to the output terminal; and

- a second current mirror circuit having input and output ends and constituted by first and second n-channel MOS-FETs in such a manner that





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source electrodes of the first and second n-channel MOS-FETs are connected to a negative power supply terminal, respectively,

gate electrodes of the first and second n-channel MOS-FETs are connected together to form the input end of the second current mirror circuit and also connected to a drain electrode of the first n-channel MOS-FET as well as the input terminal, and

a drain electrode of the second n-channel MOS-FET, which forms the output end of the second current mirror circuit, is connected to the output terminal.

13. The integrated circuit of CMOS structure according to claim 12, wherein said current-input type gate further comprises:

a first inverter of CMOS structure having input and output ends and constituted by a third p-channel MOS-FET and a third n-channel MOS-FET;

wherein said first inverter is inserted between said input terminal and the first and second current mirror circuits in such a manner that

a gate electrode of the third p-channel MOS-FET and a gate electrode of the third n-channel MOS-FET are connected together to form the input end of said first inverter and also connected to the input terminal,

a drain electrode of the third p-channel MOS-FET and a drain electrode of the third n-channel MOS-FET are connected together to form the output end of said first inverter and also connected to the input terminal,





a source electrode of the third p-channel MOS-FET is connected to the input end of said first current mirror circuit, and

a source electrode of the third n-channel MOS-FET is connected to the input end of said second current mirror circuit.

14. The integrated circuit of CMOS structure according to claim 12, wherein said current-input type gate further comprises:

a third n-channel MOS-FET and a third p-channel MOS-FET which are inserted between the input terminal and the first and second current mirror circuits in such a manner that

a gate electrode of the third n-channel MOS-FET and a gate electrode of the third p-channel MOS-FET are connected together to which a mid point potential between a positive power supply voltage of the positive power supply terminal and a negative power supply voltage of the negative power supply terminal is supplied,

a source electrode of the third n-channel MOS-FET and a source electrode of the third p-channel MOS-FET are connected together and also connected to the input terminal,

a drain electrode of the third n-channel MOS-FET is connected to the input end of the first current mirror circuit, and

a drain electrode of the third p-channel MOS-FET is connected to the input end of the second current mirror circuit.

15. The integrated circuit of CMOS structure according to claim 12, wherein said current-input type gate further comprises:

a third n-channel MOS-FET inserted in series between said input terminal and the input end of said first current mirror circuit in





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such a manner that

a source electrode of the third n-channel MOS-FET is connected to the input terminal,

a drain electrode of the third n-channel MOS-FET is connected to the input end of the first current mirror circuit, and

a potential of a sum of a mid point potential between said positive and negative power supply voltages and a threshold voltage of said third n-channel MOS-FET is applied to a gate of said third n-channel MOS-FET; and

a third p-channel MOS-FET inserted in series between said input terminal and the input end of said second current mirror circuit in such a manner that

a source electrode of the third p-channel MOS-FET is connected to the input terminal,

a drain electrode of the third p-channel MOS-FET is connected to the input end of the second current mirror circuit, and

a potential of a subtraction of a threshold voltage of said third p-channel MOS-FET from said mid point potential between said positive and negative power supply voltages is applied to a gate of said third p-channel MOS-FET.

16. The integrated circuit of CMOS structure according to claim 11, wherein said current-input type gate comprises:

a differential amplifier having an inverting input end, a non-inverting input end, and an output end; and

a negative feedback capacitor; and

wherein

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said inverting input end is connected to said input terminal,
said negative feedback capacitor is connected between said
inverting input end and said output end, and

a mid point potential between a positive power supply voltage of
the positive power supply terminal and a negative power supply
voltage of the negative power supply terminal is supplied to said non-
inverting input end of said differential amplifier.

17. The integrated circuit of CMOS structure according to any
one of claims 11 to 16, wherein said transmitting gate is formed of a
current-output type gate.

18. The integrated circuit of CMOS structure according to claim
17, wherein said current-output type gate comprises:

a second inverter of CMOS structure having input and output
ends thereof and constituted by a fourth p-channel MOS-FET and a
fourth n-channel MOS-FET in such a manner that

a gate electrode of the fourth p-channel MOS-FET and a gate
electrode of the fourth n-channel MOS-FET are connected together to
form said input end of said second inverter to which said input signal
to be transmitted is applied,

a drain electrode of the fourth p-channel MOS-FET and a
drain electrode of the fourth n-channel MOS-FET are connected
together to form said output end of said second inverter and connected
to said signal transmission path,

a source electrode of said fourth p-channel MOS-FET is
connected to the positive power supply terminal, and





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a source electrode of said fourth n-channel MOS-FET is connected to the negative power supply terminal.

19. The integrated circuit of CMOS structure according to claim 17, wherein said current-output type gate comprises:

a second inverter of CMOS structure having input and output ends thereof and constituted by a fourth p-channel MOS-FET and a fourth n-channel MOS-FET in such a manner that

gate electrodes of the fourth p-channel MOS-FET and the fourth n-channel MOS-FET are connected together to form the input end of said second inverter to which said input signal to be transmitted is applied,

drain electrodes of the fourth p-channel MOS-FET and the fourth n-channel MOS-FET are connected together and grounded through a capacitor; and

a third current mirror circuit having input and output ends and constituted by fifth and sixth p-channel MOS-FETs in such a manner that

source electrodes of the fifth and sixth p-channel MOS-FETs are connected to a positive power supply terminal, respectively,

gate electrodes of the fifth and sixth p-channel MOS-FETs are connected together to form the input end of the third current mirror circuit and also connected to a drain electrode of the fifth p-channel MOS-FET as well as the source electrode of the fourth p-channel MOS-FET of said second inverter, and

a drain electrode of the sixth p-channel MOS-FET, which forms the output end of the third current mirror circuit, is connected to the signal transmission path; and

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a fourth current mirror circuit having input and output ends and constituted by fifth and sixth n-channel MOS-FETs in such a manner that

source electrodes of the fifth and sixth n-channel MOS-FETs are connected to a negative power supply terminal, respectively,

gate electrodes of the fifth and sixth n-channel MOS-FETs are connected together to form the input end of the fourth current mirror circuit and also connected to drain electrode of the fifth n-channel MOS-FET as well as the source electrode of the fourth n-channel MOS-FET of said second inverter, and

a drain electrode of the sixth n-channel MOS-FET, which forms the output end of the fourth current mirror circuit, is connected to the signal transmission path.

20. The integrated circuit of CMOS structure according to claim 19, wherein a resistance element is connected in parallel with said capacitor.



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☒	Description	: paged 1 to paged 25
☒	Claim(s)	: paged 26 to paged 36
☐	Drawing(s)	: paged 37 to paged 37
☒	Abstract	: paged 37 to paged 37
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CMOS INTEGRATED CIRCUIT

TECHNICAL FIELD

The present invention relates to an integrated circuit
5 (IC) having a multiplicity of CMOSs (Complementary Metal-
Oxide Semiconductors) formed therein, and more particularly,
to an improvement in a signal transmission path or line in a
ULSI (Ultra-Large Scale Integrated Circuit) of CMOS.

10 BACKGROUND ART

As is well known, semiconductor elements, logical
circuits and the like formed as an LSI (Large Scale
Integrated Circuit) are electrically connected in a
predetermined manner by wiring. Likewise, in a ULSI having a
15 multiplicity of CMOSs formed therein, CMOSs, logical
circuits of CMOSs, and the like are electrically connected in
a predetermined manner by wiring. Such wiring may be often
formed by conductive paths or conductors of a predetermined
pattern formed, for example, on the surface of an integrated
20 circuit.

Fig. 6 shows an internal circuit of a conventional ULSI
of CMOSs. In this example, there is shown a case in which a
gate 11 of one CMOS at a transmitting side (hereinafter,
referred to as transmitting gate) and a gate 18 of one CMOS
25 at a receiving side (hereinafter, referred to as receiving
gate) are electrically connected through a signal
transmission path which is conductive path or conductor 15 in

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this example. Both of the transmitting gate 11 and the receiving gate 18 are constituted, in this example, by CMOS inverters (each inverter is constituted by a CMOS), respectively.

5 The transmitting gate 11 comprises a p-channel MOS·FET (MOS Field Effect Transistor) 12 and a n-channel MOS·FET 13 in which both gates thereof are connected with each other and connected to an input terminal 14, both drains thereof are connected with each other and connected to one end (input
10 end) of the conductive path 15, source of the p-channel MOS·FET 12 is connected to a power supply terminal 16 of +VDD (a positive voltage), and source of the n-channel MOS·FET 13 is connected to a power supply terminal 17 of -VSS (a negative voltage). Source of the n-channel MOS·FET 13 may be
15 connected to a common electric potential point or ground potential point.

On the other hand, the receiving gate 18 comprises a p-channel MOS·FET 21 and a n-channel MOS·FET 22 in which both gates thereof are connected with each other and connected to
20 an input terminal 23, both drains thereof are connected with each other and connected to an output terminal (not shown), source of the p-channel MOS·FET 21 is connected to the power supply terminal 16 of +VDD, and source of the n-channel MOS·FET 22 is connected to the power supply terminal 17 of
25 -VSS. The other end (output end) of the conductive path 15 is connected to the input terminal 23.

In such circuit configuration, since there inevitably

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exist a distributed capacity CL (shown by broken line) of the conductive path 15 and an input capacity CG (also shown by broken line) of the receiving gate 18, when a signal is transmitted from the transmitting gate 11 to the receiving gate 18 through the conductive path 15, the distributed capacity CL of the conductive path 15 and the input capacity CG of the receiving gate 18 will be charged by this signal. Assuming that an equivalent output resistance of the transmitting gate 11 is R_0 , the transition time in waveform of a voltage inputted to the receiving gate 18 is equal to $R_0 \times (CL + CG)$.

In reality, the transition time is also affected by a distributed resistance of the conductive path 15, but usually the equivalent output resistance R_0 is dominative over this distributed resistance and hence the influence of the distributed resistance is omitted herein. In addition, the equivalent output resistance R_0 has a nature of non-linearity so that the resistance value can be varied with change of the voltage. However, for clarity of the explanation, such characteristic is ignored herein.

Recently, ICs are growing in density of integration and degree of scale thereof higher and larger, and the size of an IC chip is also increasing more and more. For example, as shown in Fig. 7, there is not rare a ULSI in which the length of one side of its chip 24 is longer than 15 mm. In such large IC chip, wiring or conductive paths connecting circuits, elements, and the like formed in the IC chip with

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one another become long in their lengths, and there appears a conductive path which is longer than 20 mm. In an estimation of some ULSI, the number of conductive paths larger than 20 mm has become more than 5% of the total number of conductive paths.

Fig. 7 shows an example of the internal circuits of a conventional ULSI of CMOSs. It diagrammatically illustrates a multiplicity of gates, and wiring connecting therebetween, namely, conductive paths 25, 26 and 27. As shown, in addition to the conductive path 25 having a comparatively short length (200 μ m or so), there are the conductive path 26 being a very long (larger than 20 mm) and the conductive path 27 which is a very long (larger than 20 mm) and has a plurality of gates as its loads. Such conductive path 27 is used in distributing a clock signal or transmitting a bus signal, and these signals affect the whole performance (operation speed or rate) of the IC chip, namely, ULSI.

In Fig. 7, in case that a step waveform is transmitted from transmitting gates (three gates at left side in the drawing) to corresponding receiving gates through the respective conductive paths 25, 26 and 27, the input waveforms at the receiving gates are as shown in Fig. 8A by curves 25a, 26a and 27a, respectively, and in case that an impulse is transmitted from the transmitting gates to the corresponding receiving gates through the respective conductive paths 25, 26 and 27, the input waveforms at the receiving gates are as shown in Fig. 8B by curves 25b, 26b

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and 27b, respectively. As is apparent from these waveforms, owing to that the longer conductive paths 26 and 27 have very long transition times respectively as compared with the short conductive path 25, the propagation delay-times of the

5 conductive paths 26 and 27 are remarkably long in respect to the step response thereof and in respect to the pulse response thereof, if the pulse width is short, the pulse is disappeared. As a result, a clock signal having a high frequency (a short repetitive period) cannot pass through a

10 conductive path of long distance. In other words, there is an important drawback that the performance (operation speed or rate) of the whole IC chip cannot be made high.

In addition, in order to increase the density of integration of an IC and to reduce the power consumption of

15 an IC more and more, miniaturization of a CMOS is growing and the operation speed of an unity gate is improved. However, the equivalent output resistance R_0 becomes high and the distributed capacity of wiring per unit length tends to rather increase than is unchanged. Consequently, the

20 transition time is further long, resulting in a shortcoming that the operation speed of the IC chip is limited more and more.

In view of such disadvantages, recently, in order to improve the throughput of wiring in an IC chip, a method of

25 transmitting a signal in an IC chip using light has been researched or studied. However, it is necessary that light emitting elements and light receiving elements of compound

semiconductors are formed on the surface of a silicon (Si) chip and that an optical waveguide is constituted separately of an electrical wiring layer. Therefore, it is difficult at present to implement such optical signal transmission method, and even if such method should be implemented, vast increases in size and cost are estimated.

DISCLOSURE OF THE INVENTION

An object of the present invention is to provide a large scale integrated circuit of CMOS structure in which a signal can be transmitted therein at high speed or rate.

In the present invention, in order to attain the above object, there is provided an integrated circuit of CMOS structure which is characterized in that a current-input type gate having a remarkably low input impedance is used as a gate at the receiving side in respect to a signal transmission path in the integrated circuit, the current-input type gate generating an output voltage depending upon the magnitude of an input current.

In a preferred embodiment, the current-input type gate has its input terminal which is connected to a positive power supply terminal through a first current mirror circuit constituted by p-channel MOS-FETs and connected to a negative power supply terminal through a second current mirror circuit constituted by n-channel MOS-FETs.

In a first modification, the current-input type gate further includes an inverter of CMOS structure the input end

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and the output end of which are interconnected, and wherein the input end of the inverter is connected to the input terminal and respective ends of the inverter to be connected to power supply terminals are connected to the input side of the first current mirror circuit and the input side of the second current mirror circuit, respectively.

In a second modification, the current-input type gate is arranged such that the output end of the inverter of CMOS structure is connected to the input terminal, to the input end of the inverter is supplied with the mid point potential between the positive power supply voltage and the negative power supply voltage, and respective ends of the inverter to be connected to power supply terminals are connected to the input side of the first current mirror circuit and the input side of the second current mirror circuit, respectively.

In a third modification, the current-input type gate includes an n-channel MOS-FET inserted in series between the input terminal and the input side of the first current mirror circuit, and a p-channel MOS-FET inserted in series between the input terminal and the input side of the second current mirror circuit, and a potential of addition of the mid point potential between the positive and negative power supply voltages to a threshold voltage of the n-channel MOS-FET is applied to gate of the n-channel MOS-FET, a potential of subtraction of a threshold voltage of the p-channel MOS-FET from the mid point potential between the positive and negative power supply voltages being applied to gate of the

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p-channel MOS-FET.

In another preferred embodiment, the current-input type gate comprises a differential amplifier an inverting input end of which is connected to the input terminal, and a
5 negative feedback capacitor connected between the inverting input end and an output end of the differential amplifier, the mid point potential of an input logical signal being applied to a non-inverting input end of the differential amplifier.

10 In each of the embodiments and each of the modifications, a gate at the transmitting side in respect to the signal transmission path is a current-output type gate, and it is preferred that this current-output type gate is an inverter of CMOS structure.

15 In a further embodiment, the current-output type gate is a gate arranged such that an output end of an inverter of CMOS structure is grounded through a capacitor, respective ends of the inverter to be connected to power supplies are connected to a positive power supply terminal through a first
20 current mirror circuit constituted by p-channel MOS-FETs and connected to a negative power supply terminal through a second current mirror circuit constituted by n-channel MOS-FETs respectively, and the output ends of the first and second current mirror circuits are connected to the signal
25 transmission path. Further, a resistance element for maintaining a current may be connected in parallel with the capacitor.

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According to the construction of the present invention as mentioned above, since a current-input type gate having a low impedance is used as a receiving gate, the wiring capacitance CL and the gate input capacitance CG can be rapidly charged, and hence the transition time of a signal is rendered remarkably short. As a result, it is possible that even a clock signal having a high frequency (short repetitive period) passes through a long conductive path in the CMOS-IC, and so the performance (operation speed or rate) of the whole CMOS-IC chip can be made high.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic diagram showing an internal circuit of a first embodiment of the large scale integrated circuit of CMOS structure according to the present invention;

Figs. 2A and 2B are schematic diagrams showing two electric circuits of the charge responsive type gate shown in Fig. 1, respectively;

Fig. 3A, 3B and 3C are schematic diagrams showing three electric circuits of the charge responsive type gate in which a steady-state current can be zero;

Fig. 4 is a schematic diagram showing an internal circuit of a second embodiment of the large scale integrated circuit of CMOS structure according to the present invention;

Fig. 5 is a block diagram showing an internal circuit of a third embodiment of the large scale integrated circuit of CMOS structure according to the present invention;

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Fig. 6 a schematic diagram showing an example of the internal circuits of a conventional large scale integrated circuit of CMOS structure;

Fig. 7 is a diagrammatical illustration showing signal transmission paths of various lengths in a conventional large scale integrated circuit of CMOS structure; and

Figs. 8A and 8B are waveforms showing responses of a receiving gate when a step waveform and an impulse are transmitted through the transmission paths of various lengths shown in Fig. 7, respectively.

BEST MODES FOR CARRYING OUT THE INVENTION

Now, some embodiments of the present invention will be described in detail with reference to Figs. 1 to 5.

Fig. 1 shows an internal circuit of the first embodiment of the large scale integrated circuit of CMOS structure according to the present invention. In the following, portions and elements in Figs. 1 to 5 corresponding to those in Fig. 6 are denoted by the same reference characters as those in Fig. 6, and the explanations thereof are omitted unless necessary.

In the first embodiment, a transmitting gate 11 is also constituted as an inverter comprising a p-channel MOS-FET 12 and an n-channel MOS-FET 13, and has the same configuration as that of the conventional transmitting gate 11 shown in Fig. 6. Accordingly, the explanation thereof is omitted.

A receiving gate 31 connected to the output end of a

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conductive path or conductor (signal transmission path) 15 is constituted as a gate 31 which is of a current-input type and having a low input impedance (hereinafter, referred to as charge responsive type gate). The input impedance R_{in} of this charge responsive type gate 31 is sufficiently low as compared to the equivalent output resistance R_0 of the transmitting gate 11. As a result, the charge responsive type gate 31 acts to make the amplitude of an input voltage substantially zero and hence to make a current flowing in the load capacitance substantially zero thereby generating an output voltage depending on an input current.

An example of the circuit diagrams of the charge responsive type gate 31 is shown in Fig. 2A. This charge responsive type gate 31 comprises an inverter 35 constituted by a p-channel MOS-FET 33 and an n-channel MOS-FET 34, a p-channel MOS-FET 37 connected between source of the p-channel MOS-FET 33 and a power supply terminal 16 of +VDD, an n-channel MOS-FET 38 connected between source of the n-channel MOS-FET 34 and a power supply terminal 17 of -VSS or ground potential terminal, and a p-channel MOS-FET 39 and an n-channel MOS-FET 41 connected in their gates to gates of the MOS-FETs 37 and 38 respectively.

The input end (gates connected in common) and the output end (drains connected in common) of the inverter 35 are interconnected and are connected to an input terminal 36. Source of the p-channel MOS-FET 33 is connected to the power supply terminal 16 of +VDD through drain-source of the p-

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channel MOS-FET 37, and source of the n-channel MOS-FET 34 is connected to the power supply terminal 17 of -VSS or ground potential terminal through drain-source of the n-channel MOS-FET 38. Drain and gate of the MOS-FET 37 are
5 interconnected, and also drain and gate of the MOS-FET 38 are interconnected. Drains of the MOS-FET 39 and 41 are interconnected and are connected to an output terminal 42, and sources thereof are connected to the power supply terminals 16 and 17, respectively. In other words, both ends
10 of the inverter 35 to be connected to power sources are connected to input sides of a current mirror circuit constituted by the p-channel MOS-FETs 37, 39 and a current mirror circuit constituted by the n-channel MOS-FETs 38, 41 respectively.

15 In accordance with the arrangement discussed above, since the input end and the output end of the inverter 35 are short-circuited, the impedance R_{in} as has seen from the input terminal 36 is very low, and the potential of the input terminal 36 comes to substantially one at the mid point of
20 +VDD and -VSS (or 0 V). That is, the potential of the input terminal 36 becomes the threshold voltage of the inverter 35, namely, the input voltage by which the output logic of the inverter 35 is inverted, and both the MOS-FETs 33 and 34 are self-biased in between drain and source of each of them by
25 this threshold voltage, respectively.

As described above, since the potential of the input terminal 36 is one by which the inverter 35 is inverted, the

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impedance between drain and source of each of the MOS-FETs 33 and 34 is remarkably low, and the impedance of the input terminal 36 is a value of parallel connected impedances between drains and sources of the MOS-FETs 33 and 34 and hence is the lowest value. In addition, due to the effect of the negative feedback, the impedance of the input terminal 36 is further lowered, and yet, if it will depart from the lowest impedance point, an action exerts thereon for returning back to the lowest impedance point.

Moreover, the MOS-FETs 37 and 39 form a current mirror circuit and also the MOS-FETs 38 and 41 form a current mirror circuit. The input impedance of the current mirror circuit of the MOS-FETs 37 and 39, namely, the impedance of drain of the MOS-FET 37 is set to be equal to the input impedance of the current mirror circuit of the MOS-FETs 38 and 41, namely, the impedance of drain of the MOS-FET 38. In addition, it is designed that ratio of beta (β) of the FET 33 to that of the FET 34 is 1:1 and the threshold voltages of both the FETs 33 and 34 are equal to each other. Consequently, the voltage of the input terminal 36 just becomes the mid point of the power supply voltages +VDD and -VSS.

Further, the illustrated gate circuit has a steady-state current flow passing through the FETs 33, 34, 37 and 38 even if the input of the gate circuit is open. Therefore, in view of reducing the power consumption, it is desired that sizes of the FETs 33, 34, 37 and 38, that is, gate widths thereof are decreased. In practice, the gate widths of the FETs 33,

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34, 37 and 38 are determined based on a trade-off between the power consumption and the operation speed or rate.

A current flowing from the transmitting gate 11 to the input terminal 36 all of it passes through the FET 37 or 38 of the current mirror circuit and hence the impedance as seen from the FET 33 or 34 toward the FET 37 or 38 is very low because of the current input. In this case, when a current flows from the transmitting gate 11 toward the input terminal 36 (see IH in Fig. 1), it flows through the FET 38, and when a current flows from the input terminal 36 toward the transmitting gate 11 (see IL in Fig. 1), it flows through the FET 37. At that time, a current flows through the FET 39 or 41 and a difference between the current flows through the FET 39 and the FET 41 is proportional to the difference between the current flows through the FET 37 and the FET 38. In case the current flow through the FET 39 is larger than that through the FET 41, the potential of the output terminal 42 rises to about +VDD. On the contrary, in case the current flow through the FET 41 is larger than that through the FET 39, the potential of the output terminal 42 falls to about -VSS.

Since the charge responsive type gate 31 shown in Fig. 1 has a remarkably low input impedance R_{in} as described above, the distributed capacity C_L of the conductive path 15 (wiring capacitance) and the input capacity C_G of the gate 31 are both in substantially short-circuited state by such very low input impedance of the gate 31. As a result, it is hardly

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necessary that a signal outputted from the transmitting gate 11 charges the wiring capacitance CL and the gate input capacitance CG, and the transition time is very short. In other words, a change of the signal outputted from the transmitting gate 11 is transmitted to the input terminal 36 of the receiving gate 31 at high speed. In addition, if the output of the transmitting gate 11 comes to a high level, in the example shown in Fig. 2A, the potential of the output terminal 42 of the receiving gate 31 reaches about -VSS, and if the output of the transmitting gate 11 comes to a low level, the potential of the output terminal 42 of the receiving gate 31 reaches about +VDD. Accordingly, the output of the transmitting gate 11 is inverted and the inverted output appears at the output terminal 42 of the receiving gate 31.

As the charge responsive type gate 31, a gate as shown in Fig. 2B may be used wherein the inverter 35 shown in Fig. 2A is omitted and the input terminal 36 is directly connected to drain of the FET 37 and drain of the FET 38. In this first modification of the charge responsive type gate 31, the potential of the input terminal 36 becomes a potential at the mid point between +VDD and -VSS and it is a current input to both the current mirror circuits, and therefore the input impedance is low. As a result, similar functional effects to the charge responsive type gate circuit shown in Fig. 2A can be obtained. In this case, the input impedance of the charge responsive type gate circuit shown in Fig. 2B is higher than

that of the charge responsive type gate circuit shown in Fig. 2A and also a current flowing through the FETs in steady-state in Fig. 2B is larger than that in Fig. 2A. However, an advantage is obtained from the charge responsive type gate circuit of Fig. 2B that the number of elements, namely, FETs is smaller than that of the charge responsive type gate circuit of Fig. 2A.

Fig. 3A shows a second modification of the charge responsive type gate 31. This second modification includes an n-channel MOS-FET 44 and a p-channel MOS-FET 45 in place of the inverter 35 in Fig. 2A, and is arranged such that sources of the MOS-FETs 44 and 35 are connected to the input terminal 36, gates thereof are connected to a terminal 46, drains thereof are connected to corresponding drains of the MOS-FETs 37 and 38 respectively, and a potential V_c at the mid point between the power supply terminal 16 of +VDD and the power supply terminal 17 of -VSS is applied to the terminal 46.

In the above circuit configuration, if the potential of the input terminal 36 is within limits of $V_c \pm V_{th}$ (V_{th} is a threshold voltage of each of the FETs 44 and 45), no source current flows through the FETs 44 and 45, and hence the input impedance becomes high. In case the input of the gate is open, any steady-state current does not flow through the FETs 44 and 45.

If the input voltage of the input terminal 36 is even slightly out of the limits of $V_c \pm V_{th}$, the FET 44 or 45

becomes conductive, and in response thereto, the output voltage of the output terminal 42 approaches +VDD or -VSS. Since there are many cases that V_{th} is set to 10% or so of the power supply voltage, the amplitude of the voltage at the input terminal 36 will come to 20% or so of the power supply voltage. If the amplitude of the voltage is of such value, an operation of sufficiently high speed or rate is usually expected. More particularly, it is possible to make the amplitude of an input voltage a small value of about $2V_{th}$, and so a signal can be transmitted without being greatly affected by the wiring capacitance C_L and the gate input capacitance C_G . In other words, the transition time can be remarkably shortened as compared to the prior art. Further, in practice, V_{th} differs between a p-channel MOS-FET and an n-channel MOS-FET. For the purpose of easy understanding, it is assumed here that V_{th} of a p-channel MOS-FET is equal to that of an n-channel MOS-FET.

If it is desired to make a steady-state current flow zero and to make the amplitude of the voltage at the input terminal 36 smaller, as shown in Fig. 3B, gates of the FETs 44 and 45 are disconnected from each other and gate of the FET 44 is supplied with $V_c + V_{th}(n)$ ($V_{th}(n)$ is a threshold voltage of the n-channel FET 44) and gate of the FET 45 is supplied with $V_c - V_{th}(p)$ ($V_{th}(p)$ is a threshold voltage of the p-channel FET 45). In this state, since the FET 44 has its gate supplied with $V_c + V_{th}(n)$ and the FET 45 has its gate supplied with $V_c - V_{th}(p)$, if the potential of the input

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terminal 36 should be lowered even slightly below V_c , a current flows through the FET 44. On the contrary, if the potential of the input terminal 36 should be increased even slightly over V_c , a current flows through the FET 45.

5 As the charge responsive type gate 31, a gate as shown in Fig. 3C may be used wherein an inverting input terminal of a differential amplifier 48 is connected to the input terminal 36, its output terminal is connected to the output terminal 42, a negative feedback capacitor 49 is connected between the
10 output terminal and the inverting input terminal of the amplifier 48, and the mid point voltage V_c is applied to a non-inverting input terminal of the amplifier 48, the differential amplifier 48 having high gain and wide or broad band and operating at high speed or rate.

15 This differential amplifier 48 integrates a current flowing into the input terminal 36, and outputs an output voltage which is proportional to the integrated value and is inverted in polarity. As a result, if the potential at the input terminal 36 should rise even slightly over V_c , a rapid
20 charge of the capacitor 49 is effected by a negative feedback current so as to cancel the difference between the potential of the input terminal 36 and V_c so that the output voltage at the output terminal 42 is lowered. On the other hand, if the potential at the input terminal 36 should fall even slightly
25 below V_c , a rapid charge of the capacitor 49 is effected by a negative feedback current having the inverted polarity so as to cancel the difference between the potential of the input

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terminal 36 and V_c so that the output voltage at the output terminal 42 is increased. Accordingly, the potential at the input terminal 36 is maintained at V_c and the input impedance becomes substantially zero.

5 As described above, since the differential amplifier 48 has high gain and operates in wide-band, and moreover the input impedance comes to substantially zero, it can rapidly integrate an input current supplied to the input terminal 36. Therefore, the wiring capacitance C_L and the gate input
10 capacitance C_G are quickly charged and the transition time is rendered very short so that high speed operation can be performed. Further, in order to meet the range of input voltage of the succeeding stage, a circuit for limiting the amplitude of the output voltage may be connected to the
15 output terminal 42, if necessary.

 The charge responsive type gates 31 shown in Figs. 2A and 2B always consume the power. In case the transmitting gate 11 is of the type in which it outputs only a transient current, the current contributing to a signal transmission is
20 only a transient current flowing in transition of a signal, and hence it is much preferred to arrange such that only the transient current flows.

 Fig. 4 shows an internal circuit of the second embodiment of the large scale integrated circuit of CMOS structure
25 according to the present invention, and illustrates a case arranged to flow only a transient current.

 In the second embodiment, as the transmitting gate 11, a

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gate is used which has its circuit configuration similar to that of the charge responsive type gate 31 that is the receiving gate shown in Fig. 2A. This transmitting gate 11 comprises an inverter 53 constituted by a p-channel MOS-FET 51 and an n-channel MOS-FET 52, a p-channel MOS-FET 55 connected between source of the p-channel MOS-FET 51 and a power supply (positive potential) terminal 16 of +VDD, an n-channel MOS-FET 56 connected between source of the n-channel MOS-FET 52 and a power supply (negative potential) terminal 17 of -VSS or ground or common potential terminal, and a p-channel MOS-FET 57 and an n-channel MOS-FET 58 connected in their gates to gates of the MOS-FETs 55 and 56 respectively.

The input end, namely, gates connected in common of the inverter 53 are connected to the input terminal 14 and the output end, namely drains connected in common of the inverter 53 are connected to the common potential point or ground potential point through a capacitor 54. Source of the p-channel MOS-FET 51 is connected to the power supply terminal 16 of +VDD through drain-source of the p-channel MOS-FET 55, and source of the n-channel MOS-FET 52 is connected to the power supply terminal 17 of -VSS through drain-source of the n-channel MOS-FET 56. Drain and gate of the MOS-FET 55 are interconnected, and also drain and gate of the MOS-FET 56 are interconnected. Drains of the MOS-FET 57 and 58 are interconnected and are connected to the input end of the conductive path 15, and sources thereof are connected to the power supply terminals 16 and 17, respectively. In other

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words, in this second embodiment, both ends of the inverter
53 to be connected to power sources are also connected to
input sides of a current mirror circuit constituted by the p-
channel MOS-FETs 55, 57 and a current mirror circuit
5 constituted by the n-channel MOS-FETs 56, 58 respectively.

Thus, it will be understood that the construction of this
transmitting gate is the same as that of the charge
responsive type gate 31 shown in Fig. 2A except that the
input and output ends of the inverter 35 are not connected in
10 common, and in place thereof, only the input end is connected
to input terminal 36 and the output end is connected to the
common potential or ground potential point through the
capacitor 54.

In the above circuit configuration, when the potential at
15 the input terminal 14 becomes a higher level than V_c of the
mid point potential between the power supply voltages +VDD
and -VSS, a current flows through the FET 52 so that the
capacitor 54 is charged with its electrode connected to the
FET 52 being negative. The current signal is multiplied by
20 the current mirror circuit constituted by the FETs 56 and 58
thereby generating a transient current on the conductive path
15, which acts to draw a current (I_L) from the receiving gate
31. When the transition time of this current signal ends,
the current through the FETs of the transmitting gate comes
25 to zero so that no steady-state power consumption occurs in
the transmitting gate.

When the potential at the input terminal 14 is lowered

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below V_c , a current flows through the FET 51 so that the capacitor 54 is charged with its electrode connected to the FET 51 being positive. The current signal is multiplied by the current mirror circuit constituted by the FETs 55 and 57
5 thereby supplying a current (I_H) to the conductive path 15, which flows toward the receiving gate 31 through the conductive path 15. In this case, when the transition time of this current signal ends, the current through the FETs of the transmitting gate also comes to zero so that no steady-
10 state power consumption occurs in the transmitting gate.

Even in the case the transmitting gate 11 is used which is arranged such that a current flows only during the transition time of a signal as discussed above, if a gate of the type in which a steady-state current flows through the
15 gate, as shown in Figs. 2A and 2B, is used as the receiving charge responsive type gate 31, electric charges stored in the wiring capacitance C_L and the gate input capacitance C_G are discharged so that the signal output state of the receiving gate 11 cannot be maintained when the interval
20 between successive transitions of the signal on the input terminal 14 is long (the time duration in which no current flows at all is long).

In such case, as shown in Fig. 4 by dotted lines, a resistance element (or an FET acting as a resistance element)
25 61 may be connected in parallel with the capacitor 54 to flow a minute current through the resistance element 61 for maintaining the charged potentials of the capacitances,

thereby to retain the signal output state corresponding to the signal input state of the input terminal 14 in respect to the conductive path 15. This resistance element 61 may be one through which a minimum current can flow so that the
5 signal output state can be retained in any time duration other than the transition time.

In case a gate of the type in which any steady-state current or any leakage current does not flow through the gate, as shown in Figs. 3A and 3B, is used as the receiving
10 charge responsive type gate 31, the transmitting gate shown in Fig. 4 can be used. However, if it is difficult to retain the input potential of the charge responsive type gate 31 stationarily for a long time due to the existence of a minute leakage current, as previously mentioned, a resistance
15 element is connected in parallel with the capacitor 54 in case a signal to be transmitted does not change for a long time.

In case the charge responsive type gate shown in Fig. 3C is used as the receiving charge responsive type gate 31, it
20 is unnecessary in this case to connect a resistance element in parallel with the capacitor 54 so that a current can flow through the resistance element for maintaining the charged potentials of the capacitances except a case that a signal to be transmitted does not change for a long time, though it is
25 depending upon the input leakage current of the differential amplifier 48.

Further, in case a gate of the type in which a steady-

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state current flows through the gate, as shown in Fig. 1, is used as the transmitting charge responsive type gate 11, any one of the charge responsive type gates can be used. In case of transmitting a signal the transition of which always occurs at high rate or speed such as a clock signal, if the transmitting gate shown in Fig. 4 is used, any one of the charge responsive type gates shown in Figs. 2A and 2B, and Figs. 3A, 3B and 3C may be provided at the receiving side.

Since the transmitting gate 11 is a current-output type gate and the receiving gate 31 is a charge responsive type gate, namely, a current-input type gate, it can be easily implemented that, as shown in Fig. 5 for example, a plurality of transmitting current-output type gates 63 are connected to the conductive path 15, and in addition, a plurality of receiving current-input type gates 64 are connected to the conductive path 15 thereby using the conductive path 15 as a bus. Particularly, if as the current-output type gate 63 is used the transition current output gate which outputs a current only during the transition time as shown in Fig. 4 and as the current-input type gate 64 is used the charge responsive type gate through which no steady-state current flows as shown in Figs. 3A and 3B, no current flows through the conductive path 15 in the steady-state, and hence it is not required to set the current-output type gate 63 in high impedance state (inhibit state). Consequently, the control circuit and the control of timing therefor are not needed.

As described above, in accordance with the present

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invention, since a current-input type gate having a low impedance is used as a receiving gate, the wiring capacitance CL and the gate input capacitance CG can be quickly charged, and hence the transition time of a signal is rendered
5 remarkably short. As a result, it is possible that even a clock signal having a high frequency (short repetitive period) passes through a long conductive path in the CMOS-IC, and so the performance (operation speed or rate) of the whole CMOS-IC chip can be made high. In particular, the power
10 consumption can be reduced to minimum by using, as a transmitting gate, a gate which outputs a current flow only during the transition time of a signal and, as a receiving gate, a gate through which no steady-state current flows.



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THE CLAIMS

1. An integrated circuit of CMOS structure capable of transmitting an input signal to be transmitted from a transmitting side through a signal transmission path to a receiving side at high speed, said integrated circuit being characterized in that

a current-input type gate having a remarkably low input impedance is used as a receiving gate at the receiving side in respect to said signal transmission path in said integrated circuit, said current-input type gate having a low input impedance in comparison to an equivalent output resistance of the transmitting side whereby generating an output signal a voltage magnitude of which is depending upon a current magnitude of said input signal.

2. The integrated circuit of CMOS structure according to claim 1, wherein said current-input type gate has its input terminal which is connected to a positive power supply terminal through a first current mirror circuit constituted by first and second p-channel MOS-FETs and connected to a negative power supply terminal through a second current mirror circuit constituted by first and second n-channel MOS-FETs.

3. The integrated circuit of CMOS structure according to claim 2, wherein said current-input type gate further includes a first inverter of CMOS structure input end and output end of



which are interconnected, and wherein the input end of said inverter is connected to said input terminal and respective source electrodes of said inverter which are to be connected to the power supply terminals are connected to input side of said first current mirror circuit and input side of said second current mirror circuit, respectively.

4. The integrated circuit of CMOS structure according to claim 2, wherein output end of said inverter of CMOS structure is connected to said input terminal, input end of said inverter is supplied with a mid point potential between a positive power supply voltage and a negative power supply voltage, and respective source electrodes of said inverter which are to be connected to the power supply terminals are connected to input side of said first current mirror circuit and input side of said second current mirror circuit, respectively.

5. The integrated circuit of CMOS structure according to claim 2, wherein an n-channel MOS-FET is inserted in series between said input terminal and the input side of said first current mirror circuit, a potential of addition of a mid point potential between said positive and negative power supply voltages to a threshold voltage of said n-channel MOS-FET is applied to gate of said n-channel MOS-FET, a p-channel MOS-FET is inserted in series between said input terminal and the input side of said second current mirror circuit, and a potential of subtraction of a threshold voltage of said p-channel MOS-FET from said mid point potential



between said positive and negative power supply voltages is applied to gate of said p-channel MOS-FET.

6. The integrated circuit of CMOS structure according to claim 1, wherein said current-input type gate comprises a differential amplifier an inverting input end of which is connected to said input terminal, and a negative feedback capacitor connected between said inverting input end and an output end of said differential amplifier, a mid point potential between said positive and negative power supply voltages being applied to a non-inverting input end of said differential amplifier.

7. The integrated circuit of CMOS structure according to any one of claims 1 to 6, wherein a gate at the transmitting side in respect to said signal transmission path is a current-output type gate.

8. The integrated circuit of CMOS structure according to claim 7, wherein said current-output type gate is a second inverter of CMOS structure.

9. The integrated circuit of CMOS structure according to claim 7, wherein said current-output type gate is a gate arranged such that an output end of the second inverter of CMOS structure is grounded through a capacitor, respective source electrodes of said second inverter which are to be connected to power supply terminals are connected to a positive power supply terminal through a first current mirror circuit constituted by p-channel



MOS-FETs and connected to a negative power supply terminal through a second current mirror circuit constituted by n-channel MOS-FETs respectively, and output ends of said first and second current mirror circuits are connected to said signal transmission path.

10. The integrated circuit of CMOS structure according to claim 9, wherein a resistance element for maintaining a current is connected in parallel with said capacitor.

11. An integrated circuit of CMOS structure capable of transmitting an input signal to be transmitted from a transmitting side to a receiving side at high speed comprising:

a transmitting gate of CMOS structure provided in the transmitting side;

a receiving gate of CMOS structure provided in the receiving side and having a load capacitance; and

a signal transmission path provided between the transmitting gate and the receiving gate and having a substantial length with a distributed capacitance; wherein

said transmitting gate is capable of supplying said input signal to be transmitted to the signal transmission path,

said receiving gate receives said input signal of the transmitting gate from the transmission path and

said receiving gate is formed of a current-input type gate having a low input impedance in comparison to an equivalent output



resistance of the transmitting gate and capable of making a voltage magnitude of the thus received input signal across the low input impedance thereof substantially zero and hence making a current magnitude flowing in the load capacitance including the distributed capacitance substantially zero to thereby issue an output signal a voltage magnitude of which is responsive to a current magnitude of said input signal.

12. The integrated circuit of CMOS structure according to claim 11, wherein said current-input type gate comprises:

- an input terminal connected to the transmission path;
- an output terminal from which said output signal is derived;
- a first current mirror circuit having input and output ends and constituted by first and second p-channel MOS-FETs in such a manner that

- source electrodes of the first and second p-channel MOS-FETs are connected to a positive power supply terminal, respectively,

- gate electrodes of the first and second p-channel MOS-FETs are connected together to form the input end of the first current mirror circuit and also connected to a drain electrode of the first p-channel MOS-FET as well as the input terminal, and

- a drain electrode of the second p-channel MOS-FET, which forms the output end of the first current mirror circuit, is connected to the output terminal; and

- a second current mirror circuit having input and output ends and constituted by first and second n-channel MOS-FETs in such a manner that



source electrodes of the first and second n-channel MOS·FETs are connected to a negative power supply terminal, respectively,

gate electrodes of the first and second n-channel MOS·FETs are connected together to form the input end of the second current mirror circuit and also connected to a drain electrode of the first n-channel MOS·FET as well as the input terminal, and

a drain electrode of the second n-channel MOS·FET, which forms the output end of the second current mirror circuit, is connected to the output terminal.

13. The integrated circuit of CMOS structure according to claim 12, wherein said current-input type gate further comprises:

a first inverter of CMOS structure having input and output ends and constituted by a third p-channel MOS·FET and a third n-channel MOS·FET;

wherein said first inverter is inserted between said input terminal and the first and second current mirror circuits in such a manner that

a gate electrode of the third p-channel MOS·FET and a gate electrode of the third n-channel MOS·FET are connected together to form the input end of said first inverter and also connected to the input terminal,

a drain electrode of the third p-channel MOS·FET and a drain electrode of the third n-channel MOS·FET are connected together to form the output end of said first inverter and also connected to the input terminal,



a source electrode of the third p-channel MOS-FET is connected to the input end of said first current mirror circuit, and

a source electrode of the third n-channel MOS-FET is connected to the input end of said second current mirror circuit.

14. The integrated circuit of CMOS structure according to claim 12, wherein said current-input type gate further comprises:

a third n-channel MOS-FET and a third p-channel MOS-FET which are inserted between the input terminal and the first and second current mirror circuits in such a manner that

a gate electrode of the third n-channel MOS-FET and a gate electrode of the third p-channel MOS-FET are connected together to which a mid point potential between a positive power supply voltage of the positive power supply terminal and a negative power supply voltage of the negative power supply terminal is supplied,

a source electrode of the third n-channel MOS-FET and a source electrode of the third p-channel MOS-FET are connected together and also connected to the input terminal,

a drain electrode of the third n-channel MOS-FET is connected to the input end of the first current mirror circuit, and

a drain electrode of the third p-channel MOS-FET is connected to the input end of the second current mirror circuit.

15. The integrated circuit of CMOS structure according to claim 12, wherein said current-input type gate further comprises:

a third n-channel MOS-FET inserted in series between said input terminal and the input end of said first current mirror circuit in



such a manner that

a source electrode of the third n-channel MOS-FET is connected to the input terminal,

a drain electrode of the third n-channel MOS-FET is connected to the input end of the first current mirror circuit, and

a potential of a sum of a mid point potential between said positive and negative power supply voltages and a threshold voltage of said third n-channel MOS-FET is applied to a gate of said third n-channel MOS-FET; and

a third p-channel MOS-FET inserted in series between said input terminal and the input end of said second current mirror circuit in such a manner that

a source electrode of the third p-channel MOS-FET is connected to the input terminal,

a drain electrode of the third p-channel MOS-FET is connected to the input end of the second current mirror circuit, and

a potential of a subtraction of a threshold voltage of said third p-channel MOS-FET from said mid point potential between said positive and negative power supply voltages is applied to a gate of said third p-channel MOS-FET.

16. The integrated circuit of CMOS structure according to claim 11, wherein said current input type gate comprises:

a differential amplifier having an inverting input end, a non-inverting input end, and an output end; and

a negative feedback capacitor; and
wherein



said inverting input end is connected to said input terminal,
said negative feedback capacitor is connected between said
inverting input end and said output end, and

a mid point potential between a positive power supply voltage of
the positive power supply terminal and a negative power supply
voltage of the negative power supply terminal is supplied to said non-
inverting input end of said differential amplifier.

17. The integrated circuit of CMOS structure according to any
one of claims 11 to 16, wherein said transmitting gate is formed of a
current-output type gate.

18. The integrated circuit of CMOS structure according to claim
17, wherein said current-output type gate comprises:

a second inverter of CMOS structure having input and output
ends thereof and constituted by a fourth p-channel MOS-FET and a
fourth n-channel MOS-FET in such a manner that

a gate electrode of the fourth p-channel MOS-FET and a gate
electrode of the fourth n-channel MOS-FET are connected together to
form said input end of said second inverter to which said input signal
to be transmitted is applied,

a drain electrode of the fourth p-channel MOS-FET and a
drain electrode of the fourth n-channel MOS-FET are connected
together to form said output end of said second inverter and connected
to said signal transmission path,

a source electrode of said fourth p-channel MOS-FET is
connected to the positive power supply terminal, and



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a source electrode of said fourth n-channel MOS-FET is connected to the negative power supply terminal;

19. The integrated circuit of CMOS structure according to claim 17, wherein said current-output type gate comprises:

a second inverter of CMOS structure having input and output ends thereof and constituted by a fourth p-channel MOS-FET and a fourth n-channel MOS-FET in such a manner that

gate electrodes of the fourth p-channel MOS-FET and the fourth n-channel MOS-FET are connected together to form the input end of said second inverter to which said input signal to be transmitted is applied,

drain electrodes of the fourth p-channel MOS-FET and the fourth n-channel MOS-FET are connected together and grounded through a capacitor; and

a third current mirror circuit having input and output ends and constituted by fifth and sixth p-channel MOS-FETs in such a manner that

source electrodes of the fifth and sixth p-channel MOS-FETs are connected to a positive power supply terminal, respectively,

gate electrodes of the fifth and sixth p-channel MOS-FETs are connected together to form the input end of the third current mirror circuit and also connected to a drain electrode of the fifth p-channel MOS-FET as well as the source electrode of the fourth p-channel MOS-FET of said second inverter, and

a drain electrode of the sixth p-channel MOS-FET, which forms the output end of the third current mirror circuit, is connected to the signal transmission path; and



a fourth current mirror circuit having input and output ends and constituted by fifth and sixth n-channel MOS-FETs in such a manner that

source electrodes of the fifth and sixth n-channel MOS-FETs are connected to a negative power supply terminal, respectively,

gate electrodes of the fifth and sixth n-channel MOS-FETs are connected together to form the input end of the fourth current mirror circuit and also connected to drain electrode of the fifth n-channel MOS-FET as well as the source electrode of the fourth n-channel MOS-FET of said second inverter, and

a drain electrode of the sixth n-channel MOS-FET, which forms the output end of the fourth current mirror circuit, is connected to the signal transmission path.

20. The integrated circuit of CMOS structure according to claim 19, wherein a resistance element is connected in parallel with said capacitor.

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ABSTRACT

In a ultra-large scale integrated circuit of CMOS structure, high speed operation can be performed without being affected by the wiring capacitance and the gate input capacitance. A current-output type gate is used as a transmitting gate 11, and a capacitor 54 is charged or discharged only during the transition time of a signal. The charge or discharge current is multiplied by current mirror circuits 55, 56 to supply the current to a conductive path 15. A current-input type gate is used as a receiving gate 31. This gate 31 is arranged such that the output and input ends of an inverter 35 of CMOS structure are interconnected, respective ends of the inverter to be connected to power supplies are connected to a positive power supply terminal 16 through the current mirror circuit of p-channel MOS-FETs 37, 39 and connected to a negative power supply terminal 17 through the current mirror circuit of n-channel MOS-FETs 38, 41 respectively, and the output ends of both the current mirror circuits are connected to the signal transmission path 15.

PCT

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(54)Title: CMOS INTEGRATED CIRCUIT (54)発明の名称 CMOS集積回路 (57) Abstract A super large scale integration which has a CMOS structure and can operate at a high speed regardless of the wiring capacitance of the circuit and the input capacitances of gates. The integration is constituted in such a way that a transmission-side gate (11) is constituted of a current output type gate and a capacitor (54) is charged and discharged only during the transition period of signals. On addition, the current of the capacitor (54) is made to flow to a conducting path (15) after the current is doubled by means of current mirror circuits (55 and 56). A reception-side gate (31) is constituted of a low-input impedance current inputting type gate. The gate (31) short-circuits the input and output terminals of a CMOS inverter (35) to each other and both the power source connecting terminals are respectively connected to positive and negative power terminals (16 and 17) through p-channel MOSFET current mirror circuits (37 and 39) and n-channel MOSFET current mirror circuits (38 and 41). The output sides of the current mirror circuits (37, 39, 38 and 41) are connected to the conducting path (15). (54)Title: CMOS INTEGRATED CIRCUIT (54)発明の名称 CMOS集積回路 (57) Abstract A super large scale integration which has a CMOS structure and can operate at a high speed regardless of the wiring capacitance of the circuit and the input capacitances of gates. The integration is constituted in such a way that a transmission-side gate (11) is constituted of a current output type gate and a capacitor (54) is charged and discharged only during the transition period of signals. On addition, the current of the capacitor (54) is made to flow to a conducting path (15) after the current is doubled by means of current mirror circuits (55 and 56). A reception-side gate (31) is constituted of a low-input impedance current inputting type gate. The gate (31) short-circuits the input and output terminals of a CMOS inverter (35) to each other and both the power source connecting terminals are respectively connected to positive and negative power terminals (16 and 17) through p-channel MOSFET current mirror circuits (37 and 39) and n-channel MOSFET current mirror circuits (38 and 41). The output sides of the current mirror circuits (37, 39, 38 and 41) are connected to the conducting path (15).		

CMOS構造の超大規模集積回路において配線容量、ゲート入力容量に影響されずに高速動作を可能にする。送信側ゲート11を電流出力形ゲートとし、信号の遷移期間のみコンデンサ54を充放電させ、その電流をカレントミラー回路55、56で増倍して導電路15に流す。受信側ゲート31は低入力インピーダンス電流入力形ゲートとする。このゲート31は、CMOSインバータ35の入出力端を短絡し、その両電源接続端をpチャネルMOSFETカレントミラー回路37、39及びnチャネルMOSFETカレントミラー回路38、41を通じて正及び負の電源端子16及び17にそれぞれ接続し、両カレントミラー回路の出力側を導電路15に接続した構成とする。

PCTに基づいて公開される国際出願のパンフレット第一頁に掲載されたPCT加盟国を同定するために使用されるコード (参考情報)

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