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AMETHOD TO FORM AN INVERTED STAIRCASE STI STRUCTURE BY ETCH-DEPOSITION-ETCH AND SELECTIVE EPITAXIAL GROWTH

FIELD OF THE INVENTION

The present invention relates generally to forming isolation structures ir semiconductor devices, and more specifically to methods forming shallow trench is olation regions (STI) in semiconductor devices.

BACKGROUND OF THE INVENTION

Latchup has been a concern for most of the complementary metal-oxide semiconductor (CMOS) technologies. Latchup is a parasitic circuit effect, the result of which is the shorting of the V_{DD} and V_{SS} lines that usually results in chip self-destruction or at least system failure with the requirement to power down. Latchup effects will become severe when the VLSI circuit dimension is scaled. There are currently various ways to improve the latchup immunity by transistor design.

U.S. Patent No. 5,681,776 to Hebert et al. describes selective epitaxial growth (SEG) active areas formed on an opening in an oxide layer.

U.S. Patent No. 4,900,692 to Robinson describes epitaxial silicon (epi) active areas in a trench.

U.S. Patent No. 5,212,110 to Pfiester et al. describes an epi active growth area.

U.S. Patent No. 5,773,351 to Choi describes an SEG active area formed on an opening in an insulation layer.

U.S. Patent No. 4,886,763 to Suzuki describes a process for forming EPI active areas between isolation areas.

SUMMARY OF THE INVENTION

Accordingly, it is an object of the present invention to provide a method of reducing latchup effect in adjacent semiconductor devices.

Another object of the present invention to provide a method of reducing latchup effect in adjacent semiconductor devices by increasing the distance between the n^+ S/D area of one semiconductor device to the p^+ S/D area of an adjacent semiconductor device.

Another object of the present invention to provide a method of reducing latchup effect in adjacent semiconductor devices by increasing the distance between the n^+ S/D area of one NMOS semiconductor device, for example, to the p^+ S/D area of an adjacent PMOS semiconductor device, for example, without sacrificing the isolation and the real estate.

Other objects will appear hereinafter.

It has now been discovered that the above and other objects of the present invention may be accomplished in the following manner. Specifically, a semiconductor substrate having an overlying oxide layer is provided. The substrate having at least a pair of active areas defining an STI region therebetween. The oxide layer is etched a first time within the active areas to form first step trenches. The first step trenches having exposed sidewalls. Continuous side wall spacers are formed on said exposed first step trench sidewalls. The oxide layer is etched X + 1 more successive times using the previously formed step side wall spacers as masks

to form successive step trenches within the active areas. Each of the successive step trenches having exposed sidewalls and have side wall spacers successively formed on the successive step trench exposed sidewalls. The oxide layer is etched a final time using the previously formed step side wall spacers as masks to form final step trenches exposing the substrate within the active areas. The STI region comprising an inverted staircase shaped STI structure. The step side wall spacers are removed from the X + 2 step trenches. A planarized active area silicon structure is formed within the X + 2 and final step trenches.

BRIEF DESCRIPTION OF THE DRAWINGS

The features and advantages of the present invention will be more clearly understood from the following description taken in conjunction with the accompanying drawings in which like reference numerals designate similar or corresponding elements, regions and portions and in which:

Figs. 1 to 10 schematically illustrate in cross-sectional representation a preferred embodiment of the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Unless otherwise specified, all structures, layers, etc. may be formed or accomplished by conventional methods known in the prior art.

Definition of Active Areas 16 / STI 20

Accordingly as shown in Fig. 1, starting semiconductor substrate 10 may be a silicon substrate.

Oxide (SiO_2) layer 12 is formed over substrate 10 to a thickness of preferably from about 1000 to 8000Å, and more preferably from about 2500 to 4500Å.

Hard mask layer 14 is formed over oxide layer 12 to a thickness of preferably from about 300 to 2000Å, and more preferably from about 300 to 800Å. Hard mask layer 14 is preferably formed of polysilicon.

Hard mask layer 14 is patterned to expose oxide layer 12 within active areas 16. Hard mask layer 14 may be patterned by, for example, forming a patterned photoresist layer 17 over hard mask layer 14 as shown in Fig. 1, exposing hard mask 14 within, and defining, active areas 16. Hard mask 14 is then etched, exposing oxide layer 12 within active areas 16 and the patterned photoresist layer 17 is removed.

Active areas 16 are each preferably from about 0.05μm to 50μm wide, and more preferably from about 0.05 to 30μm wide [size of typical active layer mask].

Adjacent active areas 16 define inverted staircase STI region 20 therebetween. Semiconductor devices 22, 23 will be formed within active areas 16 and electrically isolated by inverted staircase STI region 20 (see Fig. 9).

Formation of First Step trench 18

As shown in Fig. 2, oxide layer 12 is etched to a depth of from about 500 to 1500Å within active area 16 to form first step trench 18.

Formation of First Spacers 26

As shown in Fig. 3, first spacer layer 24 is formed over the structure, partially filling trench 18. Spacer layer 24 is preferably comprised of Si_3N_4 or SiON deposited by LPCVD or PECVD using precursors SiH_2Cl_2 / SiH_4 and BTBAS (bis(tertiary-butylamino) silane) with NH_3. Spacer layer 24 is more preferably comprised of Si_3N_4 (SiN) as will be used for illustrative purposes hereafter for each of the successive spacer layers 32, 40, (and others as desired).

First SiN spacer layer 24 is deposited to a thickness of from preferably about 100 to 1000Å, and more preferably from about 100 to 350Å.

As shown in Fig. 4, first SiN spacer layer 24 is then isotropically etched to form first SiN spacers 26 on the sidewalls 28 of first trench / first step 18. First SiN spacers 26 are preferably from about 80 to 1200Å wide, and more preferably from about 80 to 600Å wide.

Formation of Second Step trench 30

As shown in Fig. 4, oxide layer 12 is then etched a second time to a depth of from about 500 to 1500Å within active areas 16, using first SiN spacers 26 and patterned polysilicon hard mask layer 14 as masks, to form second step trench 30.

Formation of Second Spacer 34

As shown in Fig. 5, second SiN spacer layer 32 is formed over the structure of Fig. 4 by the same method as the first SiN spacer layer 24 is formed.

Second SiN spacer layer 32 is deposited to a thickness of from preferably about 100 to 1000Å, and more preferably from about 100 to 350Å.

As shown in Fig. 6, second SiN spacer layer 32 is then isotropically etched to form second SiN spacers 34 on the sidewalls 36 of second trench / second step 30 and on first SiN spacers 26. Second SiN spacers 34 are preferably from about 80 to 1200Å wide, and more preferably from about 80 to 600Å wide.

Formation of Third Step trench 38

As shown in Fig. 6, oxide layer 12 is then etched a third time to a depth of from about 500 to 1500Å within active areas 16, using first SiN spacers 26, second SiN spacers 32, and patterned polysilicon hard mask layer 14 as masks, to form third step trench 38.

Formation of Third Spacer 42

As shown in Fig. 7, third SiN spacer layer 40 is formed over the structure of Fig. 6 by the same method as the first and second SiN spacer layers 24, 32 are formed.

Third SiN spacer layer 40 is deposited to a thickness of from preferably about 100 to 1000Å, and more preferably from about 100 to 350Å.

As shown in Fig. 8, third SiN spacer layer 40 is then isotropically etched to form third SiN spacers 42 on the sidewalls 44 of third trench / third step 38, and on second SiN spacers 34. Third SiN spacers 42 are preferably from about 80 to 1200Å wide, and more preferably from about 80 to 600Å wide.

Although for illustrative purposes, three trenches / steps 18, 30, 39 have been fabricated, fewer trenches / steps or more trenches / steps may be formed. Preferably, from two to five trenches / steps are formed.

Formation of Final Step trench 70

As shown in Fig. 8, final step trench 70 is formed through the remainder of oxide layer12 within active area 16 to expose substrate 10 using first, second, and third SiN spacers 26, 34, 42 (and any other SiN spacers formed) and patterned polysilicon hard mask layer 14 as masks.

Removal of SiN Spacers 26, 34, 42 and Patterned Hard Mask Layer 14

As shown in Fig. 9, first, second, and third SiN spacers 26, 34, 42 and patterned hard mask layer 14 are removed from the structure of Fig. 8, exposing first, second, and third trenches/steps 18, 30, 38 and their respective sidewalls 28, 36, 44.

Formation of Active Area Silicon Structures 46'

As shown in Fig. 9, silicon layer 46 is selectively deposited over the structure, filling first, second, third trenches and final / steps 18, 30, 38, 70 and planarized to form planarized active area silicon structures 46' contacting substrate 10 and within active areas 16. Silicon layer 46 is preferably formed from epitaxial silicon (epi).

Formation of Semiconductor Devices 22, 23 over Active Area Epi Structures 46'

As shown in Fig. 10, conventional processes may be used to form semiconductor devices 22, 23 over active area epi structures 46' within active areas

16. Semiconductor devices 22, 23 including, for example: gate electrodes 50 with underlying gate dielectric layers 52; and S/D areas 54, 56. For example, as shown in Fig. 10, device 22 may be an N metal-oxide semiconductor (NMOS) with N^+ doped S/D areas 54, 56 and device 22 may be a P metal-oxide semiconductor (PMOS) with P^+ doped S/D areas 54, 56. It is noted that adjacent devices 22, 23 may both be either NMOS or PMOS devices.

The intervening inverted staircase shaped STI region 20 between adjacent semiconductor devices 22, 23 formed over staircase shaped active area epi structures 46' serve to electrically isolate adjacent semiconductor devices 22, 23. The inverted staircase structure of the active area epi structures 46' increases the path between the NMOS n^+ S/D area of one semiconductor device 22 and the PMOS p^+ S/D area of the adjacent semiconductor device 23. This would also be the case for two adjacent NMOS or PMOS devices.

This beneficially improves the latchup immunity. This path length may be modified by formation of fewer or greater number of trenches / steps, and is a function of the height and width of the trenches / steps so formed, for example.

By fabricating the sloped, stepped staircase active area epi structures 46' of the present invention, the basewidth 60 between the n^+ S/D area of one semiconductor device 22 and the p^+ S/D area of the adjacent semiconductor device 23 is effectively extended which improves latchup immunity for the chips employing the method of the present invention. This reduces system failure and the requirement to power down.

While particular embodiments of the present invention have been illustrated and described, it is not intended to limit the invention, except as defined by the following claims.

CLAIMS

We claim:

1. A method of forming an inverted staircase shaped STI structure, comprising the steps of:

a) providing a semiconductor substrate having an overlying oxide layer; said substrate having at least a pair of active areas defining an STI region therebetween;

b) etching said oxide layer a first time within said active areas to form first step trenches; said first step trenches having exposed sidewalls;

c) forming continuous side wall spacers on said exposed first step trench sidewalls;

d) etching said oxide layer X + 1 more successive times using the previously formed step side wall spacers as masks to form successive step trenches within said active areas; each said successive step trenches having exposed sidewalls and having side wall spacers successively formed on said successive step trench exposed sidewalls;

e) etching said oxide layer a final time using the previously formed step side wall spacers as masks to form final step trenches exposing said substrate within said active areas; said STI region comprising an inverted staircase shaped STI structure;

f) removing said step side wall spacers from said X + 2 step trenches; and

g) forming planarized active area silicon structures within said X + 2 and final step trenches.

2. The method of claim 1, wherein X is a number from 0 to 3.

4. The method of claim 1, wherein said active areas have a width of from about 0.05 to 50μm; said first step trench has a depth below said semiconductor substrate of from about 500 to 1500Å; said successive step trenches have a depth below the respective previous step trench of from about 500 to 1500Å.

5. The method of claim 1, wherein said oxide layer is from about 1000 to 8000Å thick, said side wall spacers are from about 80 to 1200Å wide and are formed of Si_3N_4; and said active area silicon structure is formed of epitaxial silicon.

6. The method of claim 1, wherein said oxide layer is from about 2500 to 4500Å thick, said side wall spacers are from about 80 to 600Å wide and are formed of Si_3N_4; and said active area silicon structure is formed of epitaxial silicon.

7. The method of claim 1, wherein said oxide layer includes an overlying patterned hard mask exposing said oxide layer within said active areas.

8. The method of claim 1, wherein said oxide layer includes an overlying patterned polysilicon hard mask exposing said oxide layer within said active areas.

9. The method of claim 1, wherein semiconductor devices are formed on the upper surface of said planarized active area silicon structures.

10. A method of forming an inverted staircase shaped STI structure, comprising the steps of:

a) providing a semiconductor substrate having an overlying oxide layer; said oxide layer having an overlying patterned hard mask layer defining at least a pair of active areas; said active areas defining an STI region therebetween;

b) etching said oxide layer through said patterned hard mask a first time within said active areas to form first step trenches; said first step trenches having exposed sidewalls;

c) forming continuous side wall spacers on said exposed first step trench sidewalls;

d) etching said oxide layer X + 1 more successive times using said patterned hard mask and the previously formed step side wall spacers as masks to form successive step trenches within said active areas; each said successive step trenches having exposed sidewalls and having side wall spacers successively formed on said successive step trench exposed sidewalls;

e) etching said oxide layer a final time using said patterned hard mask and the previously formed step side wall spacers as masks to form final step trenches exposing said substrate within said active areas; said STI region comprising an inverted staircase shaped STI structure;

f) removing said patterned hard mask and said step side wall spacers, from said X + 2 step trenches; and

g) forming planarized active area silicon structures within said X + 2 and final step trenches.

10. The method of claim 9, wherein X is a number from 0 to 3.

11. The method of claim 9, wherein said active areas have a width of from about 0.05 to 50μm; said first step trench has a depth below said semiconductor substrate

of from about 500 to 1500Å; said successive step trenches have a depth below the respective previous step trench of from about 500 to 1500Å.

12. The method of claim 9, wherein said oxide layer is from about 1000 to 8000Å thick; said patterned hard mask is from about 300 to 2000Å thick and is formed of polysilicon; said side wall spacers are from about 80 to 1200Å wide and are formed of Si_3N_4; and said active area silicon structure is formed of epitaxial silicon.

13. The method of claim 9, wherein said oxide layer is from about 2500 to 4500Å thick; said patterned hard mask is from about 300 to 800Å thick and is formed of polysilicon; said side wall spacers are from about 80 to 600Å wide and are formed of Si_3N_4; and said active area silicon structure is formed of epitaxial silicon.

14. The method of claim 9, wherein semiconductor devices are formed on the upper surface of said planarized active area silicon structures.

15. A method of forming an inverted staircase shaped STI structure, comprising the steps of:

a) providing a semiconductor substrate having an overlying oxide layer; said oxide layer having an overlying patterned polysilicon hard mask layer defining at least a pair of active areas; said active areas defining an STI region therebetween;

b) etching said oxide layer through said patterned polysilicon hard mask a first time within said active areas to form first step trenches; said first step trenches having exposed sidewalls;

c) forming continuous Si_3N_4 side wall spacers on said exposed first step trench sidewalls;

d) etching said oxide layer X + 1 more successive times using said patterned polysilicon hard mask and the previously formed step Si_3N_4 side wall spacers as masks to form successive step trenches within said active areas; each said successive step trenches having exposed sidewalls and having Si_3N_4 side wall spacers successively formed on said successive step trench exposed sidewalls;

e) etching said oxide layer a final time using said patterned polysilicon hard mask and the previously formed step Si_3N_4 side wall spacers as masks to form final step trenches exposing said substrate within said active areas; said STI region comprising an inverted staircase shaped STI structure;

f) removing said patterned polysilicon hard mask and said Si_3N_4 step side wall spacers from said X + 2 step trenches; and

g) forming planarized active area silicon structures within said X + 2 and final step trenches.

16. The method of claim 15, wherein X is a number from 0 to 3.

17. The method of claim 15, wherein said active areas have a width of from about 0.05 to 50μm; said first step trench has a depth below said semiconductor substrate of from about 500 to 1500Å; said successive step trenches have a depth below the respective previous step trench of from about 500 to 1500Å.

18. The method of claim 15, wherein said oxide layer is from about 1000 to 8000Å thick; said patterned polysilicon hard mask is from about 300 to 2000Å thick; said Si_3N_4 side wall spacers are from about 80 to 1200Å wide; and said active area silicon structure is formed of epitaxial silicon.

.9. The method of claim 15, wherein said oxide layer is from about 2500 to 4500Å thick; said patterned polysilicon hard mask is from about 300 to 800Å thick; said Si_3N_4 side wall spacers are from about 80 to 600Å wide; and said active area silicon structure is formed of epitaxial silicon.

20. The method of claim 15, wherein semiconductor devices are formed on the upper surface of said planarized active area silicon structures.

21. A method of forming an inverted staircase shaped STI structure, comprising the steps of:

a) providing a semiconductor substrate having an overlying oxide layer; said oxide layer having an overlying patterned polysilicon hard mask layer defining at least a pair of active areas; said active areas defining an STI region therebetween; said active areas have a width of from about 0.05 to 50μm;

b) etching said oxide layer through said patterned polysilicon hard mask a first time within said active areas to form first step trenches; said first step trenches having exposed sidewalls; said first step trench having a depth below said semiconductor substrate of from about 500 to 1500Å;

c) forming continuous Si_3N_4 side wall spacers on said exposed first step trench sidewalls;

d) etching said oxide layer X + 1 more successive times using said patterned polysilicon hard mask and the previously formed step Si_3N_4 side wall spacers as masks to form successive step trenches within said active areas; each said successive step trenches having exposed sidewalls and having Si_3N_4 side wall spacers successively formed on said successive step trench exposed sidewalls;

e) etching said oxide layer a final time using said patterned polysilicon hard mask and the previously formed step Si_3N_4 side wall spacers as masks to form final step trenches exposing said substrate within said active areas; said STI region comprising an inverted staircase shaped STI structure; said successive step trenches having a depth below the respective previous step trench of from about 500 to 1500Å;

f) removing said patterned polysilicon hard mask and said Si_3N_4 step side wall spacers from said X + 2 step trenches; and

g) forming planarized active area silicon structures within said X + 2 and final step trenches.

22. The method of claim 21, wherein X is a number from 0 to 3.

23. The method of claim 21, wherein said oxide layer is from about 1000 to 10000Å thick; said patterned polysilicon hard mask is from about 300 to 2000Å thick; said Si_3N_4 side wall spacers are from about 80 to 1200Å wide; and said active area silicon structure is formed of epitaxial silicon.

24. The method of claim 21, wherein said oxide layer is from about 2500 to 4500Å thick; said patterned polysilicon hard mask is from about 300 to 800Å thick; said Si_3N_4 side wall spacers are from about 80 to 600Å wide; and said active area silicon structure is formed of epitaxial silicon.

25. The method of claim 21, wherein semiconductor devices are formed on the upper surface of said planarized active area silicon structures.