A METHOD AND APPARATUS FOR PHASE SENSITIVE DETECTION OF EDDY CURRENT MEASUREMENTS

Background to the Invention

Eddy Current (EC) instruments are typically used to detect defects, such as cracks and thinning in electrically conductive structures, usually made from metals or to measure material properties such as conductivity and permeability, which in turn are related to hardness and material structure. All of these are observed by monitoring the change in the magnitude and phase of magnetically induced eddy currents. A drive coil that produces an alternating magnetic field is generally provided close to a test piece to induce current in the test piece. The presence of defects disrupts the circulating Eddy Currents. Eddy currents can be sensed by picking up their magnetic field or by measuring the change of impedance of the drive coil.

There are many arrangements for inducing and sensing eddy currents, but in nearly every case there is a need to measure the phase and amplitude relationship between the sensed and drive signal. This can be done either digitally or by using analogue methods. Often the change in the sensed signal due to a defect is small and electrical noise can mask the measurement. In some cases it is necessary to remove effects on the signal due to other parts of the structure, such as supports. This is often done using multi-frequency drive currents, in which one or more of the frequencies is sensitive to the defect and the others are largely only affected by the support structure.

To achieve good detectivity the instrument has to have both good amplitude and phase discrimination for both single and multi-frequency signals. Figure 1 shows one way of doing this. A received signal 1 is multiplied by a sine function 2 and a cosine function 3, followed by a low pass filter 4 to obtain the real 5 and imaginary 6 components respectively. These can then either be used directly in a complex impedance plane view of the data or with a little additional computation the phase and amplitude data can be obtained from these numbers.

The multiplication of the signal is readily performed using analog multipliers or can be done digitally using a fast processing device such as an FPGA. Digital methods have the advantage that once the signal has been digitized there are no offset and phase errors. In analog systems the physical components used in the separate real and imaginary signal processing paths will have small differences that result in errors that can be temperature and time dependent.

US 4,207,520 discloses a multiple frequency digital eddy current inspection system. Received eddy current signals from a test coil are filtered to select a desired signal which is changed into a digital signal and passed to a computer for processing and to provide results of the eddy current inspection.

US 6,734,669 discloses digital demodulation of an eddy current signal. Digital sine and cosine functions are generated and multiplied with a digitized received signal. The eddy current signal is isolated by filtering the mixed signal with a low pass filter.

Summary of the Invention

According to a first aspect of the present invention, there is provided a method of detecting defects using eddy currents, the method comprising:

exciting eddy currents in a test material using an eddy current probe;

detecting induced eddy currents in the test material;

converting the detected signal into integer values using an analog to digital convertor; and either

adding or subtracting the generated integer values to or from each of two accumulators or taking no action, so that one accumulator produces a value proportional to the real component and the other produces a value proportional to the imaginary component. These values are used to detect the presence of a defect.

Embodiments of this invention provide a method that has advantages inherent to digital methods with the simplicity of an analogue switching method. Unlike

prior methods that use multiplication followed by low pass filtering, our method is a single step process using just addition and subtraction to an accumulator and is capable of being carried out without the need for floating point arithmetic, using just simple integer mathematics.

The simplicity of the method means that it can be performed at a very fast rate and that it can, if required, be carried out using less power hungry and lower cost logic and is therefore also suitable for battery power operation.

Most FPGA devices have a limited number of multipliers. Most of the space is occupied by gates that can easily be arranged for simple addition operations and storage and so are well suited to implement examples of the present invention.

Each generated integer value is added to or subtracted from each accumulator according to the status of the accumulators flag.

The status of this flag (Add, Subtract or take no action) is pre-defined and forms part of a repeated series.

Each accumulator has its own pre-defined, repeated series. The repeated series for each of the accumulators is identical except one is shifted by a quarter of a cycle with respect to the other.

According to a second aspect of the present invention there is provided an apparatus for detecting defects using eddy currents, the apparatus comprising:

a detector for detecting induced eddy currents in a test material;

a converter for converting the detected signal into integer values; and

a controller for adding or subtracting the generated integer values to or from each of two accumulators, so that the accumulators produce values indicative of whether or not a defect is present.

Brief Description of the Drawings

Embodiments of the present invention will now be described, by way of example only, with reference to the accompanying drawings, in which:

Figure 1 illustrates amplitude and phase discrimination for a prior art instrument;

Figure 2 illustrates an example of an embodiment of the present invention;

Figure 3 illustrates a more detailed example of an embodiment of the present invention;

Figures 4a and 4b show a table and corresponding waveform of a first set of sampling positions;

Figures 5a and 5b show a second table and corresponding waveform for a second set of sampling intervals;

Figures 6a and 6b show a third table and corresponding waveform for a third set of sampling intervals;

Figure 7 illustrates conversion from real and imaginary components to amplitude and phase values; and

Figures 8a, 8b, 9a and 9b show histograms comparing results from an embodiment of the present invention compared to a conventional instrument.

Detailed Description of the Invention

Figure 2 shows an eddy current instrument 10 embodying the present invention. In this example a drive signal is synthesized from one or more sinusoidal waves generated by an oscillator 20. The digitally synthesized drive signal is passed to a digital to analog converter and low pass filter 30 and used to excite eddy currents in a test piece via a suitable probe 40.

Induced eddy currents from the test piece are then detected using a sensing device. The sensing device may comprise sensing the current in the exciting coil or coils or may be a secondary magnetic field sensing device, such as one or more coils, GMR or Hall effect sensors where the sensing device may be incorporated in the exciting probe 40 or can be separate from it.

The sensed signal is then conditioned by being passed through a suitable signal conditioner 50. The signal conditioner 50 typically performs one or more of amplification, pre-filtering and in some cases where high defect detectivity is required, subtraction of a reference signal.

The conditioned signal is then converted into an integer value, in this example using an analog to digital (A/D) converter 60. The waveform generator 20, analog to digital converter 60 and subsequent de-modulation using controller 90 may each be driven by the same clock signal to ensure that they are synchronised.

The integer values generated by the analog to digital converter 60 are added to or subtracted from 70,80 each of two accumulators 71,81 controlled by the controller 90. Each accumulator 71,81 is arranged to provide a rolling average of a predetermined number of integer numbers generated by the analog to digital converter 60. The controller 90 determines and controls whether the generated integer numbers are added to or subtracted from the running total of each accumulator 71, 81 or whether no action is taken with regard to a particular generated integer number. The controller 90 is arranged such that one accumulator 71 is arranged to provide an output value proportional to the real component of the sensed signal and the other accumulator 81 is arranged to provide a value proportional to the imaginary component of the sensed signal. A master clock (not shown) ensures that the waveform generation 20, analog to digital conversion 60 and subsequent de-modulation 70,71,80,81,90 are synchronised with each other.

If the drive signal contains more than one frequency component, then the circuit 10 may be duplicated for each of the frequency components and the controller 90 arranged to control the addition, subtraction or no action according to the selected frequency component.

The real and imaginary components for each drive signal frequency can be displayed as complex impedance planes, as a function of time or as a function

of position for an operator to detect defects, when in use. The ability to detect defects may be enhanced by subtracting reference values obtained from measurements made on a defect free part of the test piece or by way of suitable calibration.

If required, phase and amplitude data for each of the drive signal frequencies can be calculated from the real and imaginary components for suitable presentation to an operator.

Whether the controller 90 adds, subtracts or takes no action regarding a generated integer value with respect to each of the accumulators 71,81 is discussed in more detail later. Each generated integer value is added to or subtracted from each accumulator according to the status of the accumulators flag. The status of this flag (Add, Subtract or take no action) is pre-defined and forms part of a repeated series. Each accumulator 71,81 has its own pre-defined, repeated series. The repeated series for each of the accumulators is identical except the series for accumulator 81 is shifted by a quarter of a cyle with respect to the series for accumulator 71.

Figure 3 shows a preferred example of the controller 90, the accumulators 71,81 and the data buffer 91. Each of the real and imaginary components is obtained by adding or subtracting data received from the analog to digital converter 60 to the real accumulator 71 and imaginary accumulator 81 according to the status of a respective "real flag" and "imaginary flag". The status of each flag (add, subtract or take no action) is generated by suitable logic. This logic sets flags to add, subtract or take no action in accordance with a flag buffer 72,82 which stores the sequence of add, subtract or take no action flags forming a cycle for each accumulator 71,81.

Control logic within the controller 90 sets flags within each of the flag buffers 72,82 to add when a generated integer value is to be added to an accumulator 71,81, to subtract when a generated integer value is to be subtracted from an accumulator 71,81 or is set such that neither addition nor subtraction takes place.

Each accumulator 71,81 generates a rolling average over a predetermined number of generated integer values or measurement points. The precise number of generated integer values selected for the rolling average depends upon a number of factors including but not limited to the frequency of the probe drive signal, clock frequency and the level of noise rejection required. For example, if the rolling average is arranged to use 200 generated integer values, circular flag buffers 72,82 each able to store 200 add, subtract, or "no action" flags are provided and a circular byte buffer 91 with 200 memory locations is provided to store the generated integer values. As each generated integer value from the analog to digital converter 60 is added to or subtracted from each accumulator 71,81, it is also stored in the byte buffer 91 and the buffer pointer 92 is incremented to the next location. A second pointer 93, one memory location ahead points to the tail end value, and this value is removed from each accumulator 71,81. Removal involves performing the opposite operation from that done originally i.e. if the generated integer value was originally added to the accumulator 71,81, it is now subtracted. If the value was originally subtracted from the accumulator 71,81, it is now added. If no action was taken, then no action is taken to reverse it. In order to do this, the add, subtract and "no action" flags are stored in the circular flag buffers 72,82 which are similar to the byte buffer 91 used to store the generated integer values. Instead of using flag buffers 72,82 the add, subtract and "take no action" flags may be regenerated using suitable counters (not shown) which may be preferred as it uses less logic, reducing hardware costs and power consumption.

Figures 4a, 4b, 5a, 5b, 6a and 6b illustrate how the addition, subtraction and "no action" flags are determined. As explained above, each flag buffer 72,82 contains a cycle of addition and subtraction and possibly "no action" flags. Each cycle comprises at least one series of one or more additions and at least one series of one or more subtractions, possibly also with "no action" flags. Each generated integer value is added to or subtracted from each accumulator 71,81 to form a running average. The repeated series for each of the accumulators is identical except the series for accumulator 81 is shifted

by a quarter of a cycle with respect to the series for accumulator 71. This is illustrated in the examples below.

Figure 4b illustrates a "real" sinusoidal signal and an "imaginary" sinusoidal signal. As can be seen the real sinusoidal signal is displaced from the imaginary sinusoidal cycle by a quarter of a cycle or 90°. Sample points corresponding to the point at which integer values are generated by the analog to digital converter 60 may be selected at any convenient interval. In the example of Figure 4a and Figure 4b generated integer values are sampled at 45°, 135°, 225° and 315°. As can be seen, the real and imaginary flags are selected to be "add" or "subtract" dependent upon whether the corresponding real and imaginary sinusoidal signals are positive or negative at that particular sampling angle.

Figures 5a and 5b illustrates the same number of sampling points as in Figures 4a and 4b, except in this example samples are taken at 0°, 90°, 180° and 270°. As can be seen, samples taken when the real or imaginary sinusoidal signal crosses the horizontal axis, do not generate either an addition or subtraction flag. In this situation a "no action taken" flag (0 in the table of Figure 5a) is instead generated signifying that the particular generated integer value from the analog to digital converter 60 that is generated at this sample point is neither added to nor subtracted from the accumulator.

Figures 6a and 6b provide still more sampled values producing even more precise and accurate results.

At the foot of each table in Figures 4a, 5a and 6a is provided a correction factor. This can be used to compute the true real and imaginary components of the signal by dividing by the number of samples and then multiplying by the correction factor. The correction factor for the real component is obtained by summing the absolute sine values corresponding to the position of the measurement points in a single sinusoidal cycle and dividing by the number of points. The correction factor for the imaginary component is obtained by summing the absolute cosine values corresponding to the measurement

points in a single sinusoidal cycle and dividing by the number of points. In most cases the real and imaginary values generated are used directly by an operator to detect defects, generally by presenting these values on a viewing screen. However, the amplitude and phase of the sensed signal may be determined from the real and imaginary components as illustrated in Figure 7. Since the real component 100 and imaginary component 110 are orthogonal vectors, the resultant amplitude 120 may be calculated by determining the square root of the sum of the square of the real component 100 and the imaginary component 110 by applying the Pythagoras rule. The phase angle 130 of the sensed signal is determined by calculating the arctangent of the imaginary component 110 divided by the real component 100.

Although any number of sample points may be taken in each sinusoidal cycle of the drive signal, it has been found that using an integer number of sample points in each cycle of the drive signal and an integer number of sinusoidal cycles averaged by the accumulator produces superior results. It has been found preferable to use an integer number of sample points especially when less samples are taken per sinusoidal cycle of the drive signal.

As explained above it is preferable that the analog to digital converter 60 is synchronized with the drive waveform 20 to provide consistent results.

As explained above, in some situations it is preferable to take measurements with multiple simultaneous drive frequencies. In this situation, the real and imaginary components for each of the drive frequencies may be extracted. When multiple simultaneous drive frequencies are used, the frequencies are preferably selected such that the higher frequencies are not odd integer multiples of lower frequencies i.e. not 1:3, 1:5 etc. Avoiding odd integer multiples of lower frequencies has been found to provide superior results. This is believed to be a consequence of Fourier harmonics. When using multiple drive frequencies it has been found that superior results are obtained when the same number of integer values are generated for each drive frequency and that the number of values represents an integer number of sinusoidal cycles in each case.

Figures 8a and 8b illustrate a comparison of the measurement of phase using a method in accordance with the present invention (Figure 8a) compared to a measurement from the same sample using a conventional method. Likewise, Figure 9a shows the results of the measurement of amplitude using a method in accordance with an embodiment of the present invention whilst Figure 9b shows the amplitude results from the same sample using a conventional method. As can be seen, the quality of the results is equivalent. However, the simplicity of the method of examples of the present invention enables it to be performed at a faster rate and enables it to be carried out on hardware using less power hungry and lower cost logic and is therefore suitable for use with battery power operation.

It has been found that superior results are obtained when results are balanced. Balancing is a process in which the signal from a part of the test piece without a defect is subtracted from the measurements. This difference signal can then be amplified, making better use of the analog to digital converter 60 and thus improving detectivity. In practical terms, balancing can be achieved by using an appropriate differential probe or by injection of a balance signal into the signal conditioning electronics 50. Alternatively, the signal may be balanced by digital subtraction of the output from the analog to digital converter 60.

Many variations may be made to the examples described above whilst still falling within the scope of the present invention. For example, instead of the flag buffers 72,82 shown in Figure 3, other logic or suitable counters may be used.

CLAIMS:

1. A method of detecting defects using eddy currents, the method comprising:

exciting eddy currents in a test material using an eddy current probe driven by a drive signal;

detecting induced eddy currents in the test material;

converting the detected signal into integer values using an analog to digital converter; and

adding or subtracting the generated integer values to or from each of two accumulators, or taking no action, so that one accumulator produces a value proportional to one component of the detected signal and the other produces a value proportional to another component of the detected signal and using these values to detect the presence of a defect.

2. A method according to claim 1, wherein each generated integer value is added to or subtracted from each accumulator according to the status of the accumulators flag, the status of this flag (Add, Subtract or take no action) being pre-defined and forming part of a repeated series.

3. A method according to claim 2, wherein each accumulator has its own pre-defined, repeated series of flags, the repeated series for each of the accumulators being identical except one is shifted by a quarter of a cycle with respect to the other.

4. A method according to any one of the preceding claims, wherein an integer number of integer valves are generated by the analog to digital converter in each sinusoidal cycle of the drive signal.

5. A method according to any one of the preceding claims, wherein the accumulators generate a rolling average over an integer number of sinusoidal cycles of the drive signal.

6. A method according to any one of the preceding claims, wherein one accumulator produces a value proportional to the real component of the detected signal and the other accumulator produces a value proportional to the imaginary component of the detected signal.

7. A method according to any one of the preceding claims, wherein the analog to digital converter is driven by a clock which is synchronised with the drive signal.

8. A method according to any one of the preceding claims, wherein eddy currents are excited in a test material using an eddy current probe driven at a plurality of simultaneous drive frequencies.

9. A method according to claim 8, wherein higher frequencies are selected such that they are not odd integer multiples of lower frequencies.

10. A method according to any one of the preceding claims, wherein eddy currents are excited in a test material using an eddy current probe driven at a plurality of sequential drive frequencies.

11. An apparatus for detecting defects using eddy currents, the apparatus comprising:

a detector for detecting induced eddy currents in a test material;

an analog to digital converter for converting the detected signal into integer values; and

a controller for adding or subtracting the generated integer values to or from each of two accumulators, or taking no action, so that one accumulator produces a value proportional to one component of the detected signal and the other produces a value proportional to another component of the detected signal and using these values to detect the presence of a defect.

12. An apparatus according to claim 11, wherein the controller is arranged to add, subtract or take no action with respect to each generated integer value

according to the status of each accumulator's flag, the status of each flag being pre-defined and forming part of a repeated series.

13. An apparatus according to claim 12, wherein each accumulator has its own pre-defined repeated series of flags, the repeated series of flags for each of the accumulators being identical except one is shifted by a quarter of a cycle with respect to the other.