

ABSTRACT

A memory device may include a first data line driver circuit that generates a first reference voltage set based on a first code and a second code associated with a first data line, and determines bit values of the first input data received through the first data line, based on the first reference voltage set. A second data line driver circuit may similarly generate a second reference voltage set. The reference voltages may have levels based on a decision feedback equalization (DFE) technique to reduce bit errors otherwise caused by inter symbol interference.

FIG. 1