DUAL STRESS MEMORY TECHNIQUE METHOD AND RELATED STRUCTURE

BACKGROUND OF THE INVENTION

1. TECHNICAL FIELD

The invention relates generally to stress memory techniques, and more particularly, to a method of providing a dual stress memory technique and related structure.

2. BACKGROUND ART

The application of stresses to field effect transistors (FETs) is known to improve their performance. When applied in a longitudinal direction (*i.e.*, in the direction of current flow), tensile stress is known to enhance electron mobility (or n-channel FET (nFET) drive currents) while compressive stress is known to enhance hole mobility (or p-channel FET (pFET) drive currents).

One manner of providing this stress is referred to as stress memorization technique (SMT), which includes applying an intrinsically stressed material (e.g., silicon nitride) over a channel region and annealing to have the stress memorized in, for example, the gate polysilicon or the diffusion regions. The stressed material is then removed. The stress, however, remains and improves electron or hole mobility, which improves overall performance. The anneal is typically provided as part of a dopant activation anneal.

One problem with SMT is that it is applicable only to n-type field effect transistors (nFETs). In particular, while a compressively stressed silicon nitride layer can be formed over a pFET to impart a compressive stress, the stress is removed for the most part by the subsequent and requisite dopant activation anneal. That is, most of the compressive stress is not memorized in the pFET.

In view of the foregoing, there is a need in the art to provide SMT for both nFETs and pFETs.

SUMMARY OF THE INVENTION

A method for providing a dual stress memory technique in a semiconductor device including an nFET and a pFET and a related structure are disclosed. One embodiment of the method includes forming a tensile stress layer over the nFET and a compressive stress layer over the pFET, annealing to memorize stress in the semiconductor device and removing the stress layers. The compressive stress layer may include a high stress silicon nitride deposited using a high density plasma (HDP) deposition method. The annealing step may include using a temperature of approximately 400-1200 °C. The high stress compressive silicon nitride and/or the anneal temperatures ensure that the compressive stress memorization is retained in the pFET.

A first aspect of the invention provides a method of providing a dual stress memory technique in a semiconductor device including an nFET and a pFET, the method comprising the steps of: forming a first stress layer over the semiconductor device; forming an etch stop layer over the first stress layer; removing the first stress layer and the etch stop layer over a first one of the nFET and the pFET; forming a second stress layer over the semiconductor device, wherein a stress layer over the pFET includes a compressive stress silicon nitride; annealing to memorize stress in the semiconductor device; and removing the first and second stress layer and the etch stop layer.

A second aspect of the invention provides a method of providing a dual stress memory technique for a semiconductor device including an nFET and a pFET, the method comprising the steps of: forming a tensile stress layer over the nFET and a compressive stress layer over the pFET, wherein the compressive stress layer include a high stress film that retains at least partial compressive stress during a subsequent anneal; annealing to memorize stress in the semiconductor device; and removing the compressive and tensile stress layers.

A third aspect of the invention provides a semiconductor device comprising: an nFET having a tensile stress memorized into a part thereof; and a pFET having a compressive stress memorized into a part thereof.

The illustrative aspects of the present invention are designed to solve the problems herein described and other problems not discussed, which are discoverable by a skilled artisan.

BRIEF DESCRIPTION OF THE DRAWINGS

These and other features of this invention will be more readily understood from the following detailed description of the various aspects of the invention taken in conjunction with the accompanying drawings that depict various embodiments of the invention, in which:

FIG. 1 shows a preliminary structure for one embodiment of a method according to the invention.

FIGS. 2-7 show a method according to one embodiment of the invention.

It is noted that the drawings of the invention are not to scale. The drawings are intended to depict only typical aspects of the invention, and therefore should not be considered as limiting the scope of the invention. In the drawings, like numbering represents like elements between the drawings.

DETAILED DESCRIPTION

Turning to the drawings, FIG. 1 shows a preliminary structure for one embodiment of a method of providing a dual stress memory technique (SMT) for a semiconductor device 100. The preliminary structure includes a substrate 102 having an n-type field effect transistor (nFET) 104 and a p-type field effect transistor (pFET) 106 formed thereon. As shown, semiconductor device 100 has completed initial processing such as conventional shallow trench isolation (STI) 110

formation, well implants, gate dielectric 112 formation, gate conductor 114 formation, and extension/halo/source/drain implants for diffusions 116.

Referring to FIG. 2, in one embodiment of the method, a first step includes forming a tensile stress layer 120 over nFET 104 and a compressive stress layer 122 over pFET 106. Both tensile stress layer 120 and compressive stress layer 122 may include intrinsically stressed silicon nitride (Si_3N_4). In one preferred embodiment, however, compressive stress layer 122 includes a high density plasma (HDP) silicon nitride (Si_3N_4), i.e., a silicon nitride formed using a high density plasma deposition process. In one preferred embodiment, the compressive stress layer forming step includes performing a HDP deposition of silicon nitride using the following conditions: approximately 50mTorr of pressure, approximately 200 standard cubic centimeters (sccm) of argon (Ar), approximately 100 sccm of silane (SiH_4), approximately 300sccm of nitrogen (N_2), approximately 0-1500 W of radio frequency (RF) bias power and approximately 2000W-4500W of RF source power. Compressive stress layer 122 thus includes a high stress silicon nitride that enables provision of the dual SMT because it allows retention of compressive stress (full or partial) such that the stress is memorized in parts of pFET 106 during the subsequent anneal step, described below.

The forming step may be provided in any number of fashions, only two illustrative embodiments of which will be described herein. FIGS. 3-6 show the two illustrative embodiments. A first optional preliminary step includes, as shown in FIG. 3, forming an etch stop layer 118, e.g., of silicon dioxide (SiO_2), (shown in phantom in FIG. 3 only). Next, a first sub-step, shown in FIG. 3, includes forming a first stress layer 130 over semiconductor device 100. As will be described below, first stress layer 130 may be either tensile stress layer 120 (FIG. 2) or compressive stress layer 122 (FIG. 2). As shown in FIG. 3, however, first stress layer 130 includes an intrinsically tensilely stressed silicon nitride. A second sub-step, also shown in FIG. 3, includes forming an etch

stop layer 132 over first stress layer 130. Etch stop layer 132 may include any now known or later developed etch stop material such as silicon dioxide (SiO_2). Next, as also shown in FIG. 3, first stress layer 130 and etch stop layer 132 are removed over a first one of nFET 104 and pFET 106 (pFET 106 as shown) to expose one of the FETs. The etching 138 may include use of a patterned mask 136 (shown in phantom) and any conventional dry etching chemistry for the materials used. FIG. 4 shows the resulting structure including exposed pFET 106.

Next, as shown in FIG. 5, a second stress layer 140 is formed over semiconductor device 100. As shown, second stress layer 140 is formed over pFET 106 and, hence, includes the above-described high density, compressive stress silicon nitride. In one alternative embodiment, a next step may include removing second stress layer 140 over nFET 104 prior to the annealing step, described below. The removing step may include use of a patterned mask 146 (shown in phantom) and any conventional dry etching 144 for the materials used. FIG. 6 shows the resulting structure. Where second stress layer 140 is not removed, it should be recognized that some degradation of stress imparted by first stress layer 130 may be present, but that this degradation is minimal.

In an alternative embodiment, the above-described steps may be switched. That is, the forming step may include forming a compressive stress layer 122 over semiconductor device 100, forming an etch stop layer 132 over the compressive stress layer, removing compressive stress layer 122 and etch stop layer 132 over nFET 104, and forming a tensile stress layer 120 over semiconductor device 100. As in the above-described embodiment, tensile stress layer 120 may be optionally removed over pFET 106 prior to the annealing step, described below. Where tensile stress layer 120 is not removed, it should be recognized that some degradation of stress imparted by compressive stress layer 122 may be present, but that this degradation is minimal.

FIG. 6 also shows a second step according to one embodiment of the method, which includes annealing 150 to memorize stress in semiconductor device 100. Annealing 150 preferably

includes using a temperature of no less than approximately 400 °C and no greater than approximately 1200 °C. The anneal temperature is optimized so that device 100 will be able to memorize the stress from stress layers 120, 122, and not lose the compressive stress on parts of pFET 106, which would result in a neutral or tensile stress thereon. For example, one conventional plasma-enhanced chemical vapor deposited (PECVD) compressive silicon nitride, which is formed with approximately - 1.8 GPa/cm^2 of stress drops to approximately 0.04 GPa/cm^2, i.e., a tensile stress, after anneal. In contrast, one embodiment an HDP compressive stress silicon nitride according to the invention is formed with approximately - 3.0 GPa/cm^2, which results in a stress of no less than - 100 MPa/cm^2, thus retaining a compressive stress. In one embodiment, the compressive stress may be in the range of approximately - 1 GPa/cm^2.

FIG. 7 shows a third step including removing stress layers 120, 122 and etch stop layer 132. This removing step 148 may include a wet or dry etch, or combination of them; for example, a wet or dry etch to remove etch stop layer 132 and then a wet strip using hot phosphorous acid to remove silicon nitride stress layers. FIG. 7 also shows a semiconductor device 200 according to the invention including an nFET 204 having a tensile stress 260 memorized into a part thereof, e.g., gate conductor 214 and/or diffusion region 216, and a pFET 206 having a compressive stress 262 memorized into a part thereof, e.g., gate conductor 220 and/or diffusion region 222.

The foregoing description of various aspects of the invention has been presented for purposes of illustration and description. It is not intended to be exhaustive or to limit the invention to the precise form disclosed, and obviously, many modifications and variations are possible. Such modifications and variations that may be apparent to a person skilled in the art are intended to be included within the scope of the invention as defined by the accompanying claims.

CLAIMS

What is claimed is:

1. A method of providing a dual stress memory technique in a semiconductor device including an nFET and a pFET, the method comprising the steps of:

forming a first stress layer over the semiconductor device;

forming an etch stop layer over the first stress layer;

removing the first stress layer and the etch stop layer over a first one of the nFET and the pFET;

forming a second stress layer over the semiconductor device, wherein a stress layer over the pFET includes a compressive stress silicon nitride;

annealing to memorize stress in the semiconductor device; and

removing the first and second stress layer and the etch stop layer.

2. The method of claim 1, wherein the compressive stress silicon nitride includes a high density plasma (HDP) silicon nitride.

3. The method of claim 1, further comprising the step of depositing an additional etch stop layer prior to the first stress layer forming step.

4. The method of claim 1, wherein the compressive stress silicon nitride has a stress of no less than - 100 MPa/cm^2 after the annealing step.

5. The method of claim 1, wherein the annealing step includes using a temperature of no less than approximately 400 °C and no greater than approximately 1200 °C.

6. The method of claim 1, further comprising the step of removing the second stress layer over the other one of the nFET and the pFET prior to the annealing step.

7. The method of claim 1, wherein the first one of the nFET and the pFET includes the nFET and the first stress layer includes an intrinsically tensilely stressed material, and the second stress layer includes the compressively stress silicon nitride.

8. The method of claim 1, wherein each stress layer includes silicon nitride.

9. The method of claim 1, wherein the etch stop layer includes silicon dioxide.

10. A method of providing a dual stress memory technique for a semiconductor device including an nFET and a pFET, the method comprising the steps of:

forming a tensile stress layer over the nFET and a compressive stress layer over the pFET, wherein the compressive stress layer include a high stress film that retains at least partial compressive stress during a subsequent anneal;

annealing to memorize stress in the semiconductor device; and

removing the compressive and tensile stress layers.

11. The method of claim 10, wherein the compressive stress layer forming step includes performing a high density plasma (HDP) deposition of silicon nitride using the following conditions: approximately 50mTorr of pressure, approximately 200 standard cubic centimeters (sccm) argon (Ar), approximately 100 sccm of silane (SiH_4), approximately 300 sccm of nitrogen

(N_2), approximately 0-1500 W of radio frequency (RF) bias power and approximately 2000W-4500W of RF source power.

12. The method of claim 10, wherein the annealing step includes using a temperature of no less than approximately 400 °C and no greater than approximately 1200 °C.

13. The method of claim 10, wherein each stress layer includes silicon nitride.

14. The method of claim 10, wherein the forming step includes:

forming the tensile stress layer over the semiconductor device;

forming an etch stop layer over the tensile stress layer;

removing the tensile stress layer and the etch stop layer over the pFET; and

forming the compressive stress layer over the semiconductor device.

15. The method of claim 14, further comprising the step of removing the compressive stress layer over the nFET prior to the annealing step.

16. The method of claim 14, wherein the etch stop layer includes silicon dioxide.

17. The method of claim 10, wherein the forming step includes:

forming the compressive stress layer over the semiconductor device;

forming an etch stop layer over the compressive stress layer;

removing the compressive stress layer and the etch stop layer over the nFET;

forming the tensile stress layer over the semiconductor device.

18. The method of claim 17, further comprising the step of removing the tensile stress layer over the pFET prior to the annealing step.

19. A semiconductor device comprising:

an nFET having a tensile stress memorized into a part thereof; and

a pFET having a compressive stress memorized into a part thereof.

20. The structure of claim 19, a pFET having a compressive stress memorized through a compressive high density plasma (HDP) silicon nitride layer.