nitride masking step. Although the presence of e.g. an AlGaN buffer layer may provide some compressive stress which counteracts tensile stress caused by CTE mismatch after cooling from the deposition temperature, this counteracting stress is not sufficient for a complete compensation. As a consequence, the deformation of the layered semiconductor wafer after cooling from the deposition temperature remains an issue.

Therefore, embodiments of the claimed invention seek to provide a proper solution to this problem.

According to an aspect, there is provided a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the stack of layers comprising a) an AlN nucleation layer which has a thickness of not less than 20 nm and not more than 500 nm and covers the top surface of the silicon single crystal substrate, wherein the top surface of the silicon single crystal substrate has a crystal lattice orientation which is off-oriented with respect to the {111}-plane, the normal to the top surface being inclined with respect to the <111>-direction toward the [11-2]-direction, the [1-21]-direction, or the [-211]-direction by an angle θ of not less than 0.3° and not more than 6°, the azimuthal tolerance of the inclination being ±0.1°; and b) an AlGaN buffer layer which covers the AlN nucleation layer and comprises one or more $Al_xGa_{1-x}N$ layers, wherein $0<x<1$, and wherein a top surface of the AlGaN buffer layer is a Group-III polar nitride surface.

According to another aspect, there is provided a method for producing a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the method comprising: a) providing a silicon single crystal substrate having a top surface, the top surface of the silicon single crystal substrate having a crystal lattice orientation which is off-oriented with respect to the {111}-plane, a normal to the top surface being inclined with respect to the <111>-direction toward the [11-2]-

direction, the [1-21]-direction, or the [-211]-direction by an angle θ of not less than 0.3° and not more than 6°, the azimuthal tolerance of the inclination being ±0.1°; b) depositing on the top surface of the silicon single crystal substrate an AlN nucleation layer which has a thickness of not less than 20 nm and not more than 500 nm and covers the top surface of the silicon single crystal substrate; and c) depositing an AlGaN buffer layer which covers the AlN nucleation layer and comprises one or more $Al_xGa_{1-x}N$ layers, wherein $0<x<1$, and wherein a top surface of the AlGaN buffer layer is a Group-III polar nitride surface.

An embodiment is directed to a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the stack of layers comprising an AlN nucleation layer which covers the top surface of the silicon single crystal substrate, wherein the top surface of the silicon single crystal substrate has a crystal lattice orientation which is off-oriented with respect to the {111}-plane, the normal to the top surface being inclined with respect to the <111>-direction toward the <11-2>-direction by an inclination angle θ of not less than 0.3° and not more than 6°, the azimuthal tolerance of the inclination being ± 0.1°; and an AlGaN buffer layer which covers the AlN nucleation layer and comprises one or more $Al_xGa_{1-x}N$ layers, wherein $0 < x < 1$.

In addition, another embodiment is directed to a method for producing a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the method comprising providing the silicon single crystal substrate having a top surface, the top surface of the silicon single crystal substrate having a crystal lattice orientation which is off-oriented with respect to the {111}-plane, the normal to the top

Claims

1. A semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the stack of layers comprising
a) an AlN nucleation layer which has a thickness of not less than 20 nm and not more than 500 nm and covers the top surface of the silicon single crystal substrate, wherein the top surface of the silicon single crystal substrate has a crystal lattice orientation which is off-oriented with respect to the {111}-plane, the normal to the top surface being inclined with respect to the <111>-direction toward the [11-2]-direction, the [1-21]-direction, or the [-211]-direction by an angle θ of not less than 0.3° and not more than 6°, the azimuthal tolerance of the inclination being ±0.1°; and
b) an AlGaN buffer layer which covers the AlN nucleation layer and comprises one or more $Al_xGa_{1-x}N$ layers, wherein $0<x<1$, and wherein a top surface of the AlGaN buffer layer is a Group-III polar nitride surface.

2. The semiconductor wafer of claim 1, wherein the AlGaN buffer layer comprises one or more AlN layers.

3. The semiconductor wafer of claim 1, wherein the AlGaN buffer layer comprises one or more AlN layers.

4. The semiconductor wafer of claim 1, wherein the AlGaN buffer layer comprises one or more GaN layers.

5. The semiconductor wafer of claim 1, wherein the stack of layers comprises one or more device forming layers covering the AlGaN buffer layer and having a composition of a binary, ternary or quaternary Group III-nitride containing at least one of the elements Al, Ga and In.

6. The semiconductor wafer of claim 1, wherein the silicon single

crystal substrate is a silicon single crystal wafer having a diameter of 150 mm or more.

7. The semiconductor wafer of claim 2, wherein the AlGaN buffer layer comprises one or more GaN layers.

8. The semiconductor wafer of claim 2, wherein the stack of layers comprises one or more device forming layers covering the AlGaN buffer layer and having a composition of a binary, ternary or quaternary Group III-nitride containing at least one of the elements Al, Ga and In.

9. The semiconductor wafer of claim 4, wherein the stack of layers comprises one or more device forming layers covering the AlGaN buffer layer and having a composition of a binary, ternary or quaternary Group III-nitride containing at least one of the elements Al, Ga and In.

10. A method for producing a semiconductor wafer comprising a silicon single crystal substrate having a top surface and a stack of layers covering the top surface, the method comprising:
a) providing a silicon single crystal substrate having a top surface, the top surface of the silicon single crystal substrate having a crystal lattice orientation which is off-oriented with respect to the {111}-plane, a normal to the top surface being inclined with respect to the <111>-direction toward the [11-2]-direction, the [1-21]-direction, or the [-211]-direction by an angle θ of not less than 0.3° and not more than 6°, the azimuthal tolerance of the inclination being ±0.1°;
b) depositing on the top surface of the silicon single crystal substrate an AlN nucleation layer which has a thickness of not less than 20 nm and not more than 500 nm and covers the top surface of the silicon single crystal substrate; and
c) depositing an AlGaN buffer layer which covers the AlN nucleation layer and comprises one or more $Al_xGa_{1-x}N$ layers, wherein $0<x<1$, and

wherein a top surface of the AlGaN buffer layer is a Group-III polar nitride surface.

11. The method of claim 10, further comprising depositing one or more device forming layers which cover the AlGaN buffer layer and have a composition of a binary, ternary or quaternary Group III-nitride containing at least one of the elements Al, Ga and In.

12. The method of claim 11, wherein the deposition method comprises metal-organic chemical vapor deposition (MOCVD).