WAFER LEVEL PACKAGE FOR SEMICONDUCTOR DEVICES

Abstract

The conventional practice of device assembly is to follow few packaging steps such as Die attach / wire bond / mold method. or Flip chip assembly method. Most conventionally assembled packages are quite reliable compared to flip chip packages. But does not allow small form factors when compared to Flip chip assembled packaging method. Flip chips are fabricated on wafer level. However, the flip chip bond pad pitches are smaller and does not match the pitch requirements of current substrate boards. Thus necessitating additional process developments for achieving reliable products. Use of flip chip on mother boards is still in question mark due to sound reliability of the product.

Chip Scale Packages (CSP) have emerged in the recent past to support the product miniaturizations that are in high demand by current consumer markets. However existing manufacturing processes for Chip Scale Packages are mostly single chip assembly type or wafer level chip scale packages that are highly priced. Also the number of Input / Output on CSP are limited and it is becoming difficult to achieve higher I/O count in current CSP manufacturing processes. Therefore developing a high pin count combined with low cost / high performance wafer level package has become a reality today. Many semiconductor industry around the globe are working aggressively in developing these wafer level packages to meet the semiconductor assembly and packaging industry road map requirements.

This invention approach is expected to meet such a requirement of miniaturized product, as it offers high I/O, combined with reduced cost at very small form factor that utilizes lesser board areas in SMT assembly and eliminates the time consuming underfill processes.

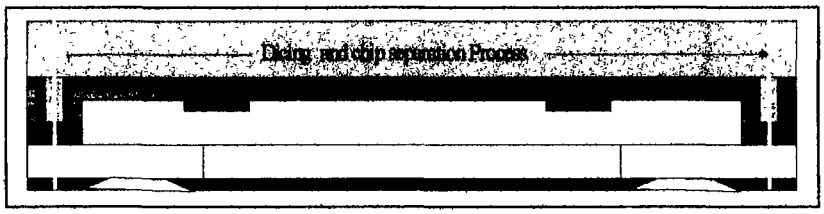


Figure: Wafer Level Package

162162

G00001

Absara Micro Systems Confidential