

SRAM-TYPE MEMORY CELL**ABSTRACT**

The invention relates to an SRAM-type memory cell comprising:

- a semiconductor on insulator substrate comprising a thin film (1) of semiconductor material separated from a base substrate (2) by an insulating (BOX) layer;
- six transistors (T1-T6), comprising two access transistors (T1, T4), two conduction transistors (T2, T5) and two charge transistors (T3, T6) arranged so as to form with said conduction transistors (T2, T5) two back-coupled inverters,

characterized in that each of the transistors (T1-T6) has a back control gate (BG1, BG2) formed in the base substrate (2) below the channel and able to be biased in order to modulate the threshold voltage of the transistor, a first back gate line connecting the back control gates of the access transistors to a first potential and a second back gate line connecting the back control gates of the conduction transistors and charge transistors to a second potential, the first and second potentials being modulated according to the type of cell control operation.

Figure 1