159159

METHOD OF FORMING EPITAXIAL METAL DISILICIDE FOR A SEMICONDUCTOR DEVICE

G00002

Technical Field

This invention relates to a semiconductor device and, in particular, to a method of forming a metal disilicide (eg. cobalt disilicide) on a substrate of such a semiconductor device.

Background of the Invention

Various metallisation, interconnect and polycrystalline silicide (polycide) formation processes are known and used in the fabrication of semiconductor devices. As semiconductor devices become smaller, the contact resistances of the gate and source/drain regions are increased. There is a need for low resistivity contact materials with high thermal and chemical stability that will form uniform, smooth interfaces with the substrate.

Metal silicides are particularly important in this regard. For example, polycrystalline tungsten silicide and titanium silicide are well established contact materials. In the deep sub-micron regime, however, titanium silicide is less desirable since the transformation to the low resistivity C54 phase is found to be linewidth-dependent. Also, the roughness of the silicon:silicide interface may also begin to exceed allowable tolerances.

Cobalt disilicide exhibits low resistivity as well as a small lattice mismatch with Si (ie. about 1.2%), and there is therefore the possibility of growing epitaxial layers with low interfacial defect densities. The use of cobalt is also compatible with modern microelectronic device processing technologies. Nickel is another metal which has potential for use in this regard (eg. with the formation of nickel silicides).

Various silicidation methods using cobalt are known. One of the simplest methods involves the deposition of a layer of cobalt onto the Si wafer followed by annealing. However, a simple postjunction silicidation (PJS) does not lead to the formation of epitaxial $CoSi_2$, with the exception of silicidation of the Si(111) surface. The process also typically causes the formation of several cobalt-rich intermediate phases. Polycrystalline cobalt disilicide has several undesirable

features in relation to semiconductor devices, including lack of uniformity of the cobalt discilicide layer, which results in nonuniform contact resistance and plate resistance.

Epitaxial $CoSi_2$ offers the prospect of increased thermal and chemical stability, and lower interfacial roughness. Several means have been suggested for forming epitaxial cobalt disilicide on silicon (001) substrates, for the manufacture of semiconductor devices.

One method involves the formation of a thin layer of titanium between the silicon substrate and the cobalt layer, followed by annealing (known as titanium interlayer-mediated epitaxy).

Another example, disclosed in US Patent No 5,567,652, is a method of forming epitaxial cobalt disilicide by first forming a silicon oxide film on the surface of the silicon substrate, followed by the deposition of a titanium film, followed finally by a cobalt film. After heat treatment an epitaxial cobalt disilicide film is formed on the substrate.

US Patent No 6,077,750 describes the formation of a buffer layer of silicon oxide (SiOx) on the silicon substrate. (Alternatively, silicon fluoride (SiF_x) or silicon carbide (SiC_x) may be used.) The oxide layer is formed by boiling the silicon substrate in a series of oxidising and reducing solutions. A layer of cobalt is then deposited on the buffer layer and an annealing process is applied to form epitaxial $CoSi_2$.

The present invention is directed towards an alternative method for forming epitaxial cobalt disilicide on a silicon substrate.

Summary of the Invention

According to a first embodiment of this invention there is provided a method of forming an epitaxial metal silicide on a silicon substrate including the steps of:

- depositing on a silicon substrate a diffusion membrane of silicon nitride;
- depositing on the diffusion membrane a layer of metal; and
- annealing the layered substrate at an elevated temperature;

wherein the metal is selected from cobalt and nickel.

It is preferred that the metal used in this method is cobalt. The use of the diffusion membrane of silicon nitride seems to inhibit the formation of cobalt-rich intermediate phases and results in the formation of epitaxial cobalt disilicide.

The diffusion membrane should be sufficiently thin so as to allow metal (eg. cobalt) from the metal layer to diffuse through the membrane at the elevated temperature. The thickness of the diffusion membrane is typically between about 5 angstroms and 50 angstroms. It is particularly preferred that the thickness of the diffusion membrane is between about 10 angstroms and 40 angstroms.

The thickness of the metal (eg. cobalt) layer is typically between about 10 angstroms and 130 angstroms. It is particularly preferred that the thickness of this layer is between about 30 angstroms and 80 angstroms.

The annealing step is preferably effected at a temperature greater than 300°C. It is particularly preferred that the annealing temperature be between about 400°C and 1000°C.

The diffusion membrane may be deposited by means selected from sputtering, chemical vapour deposition and exposure of the substrate to an ammonia atmosphere. It is particularly preferred that the diffusion membrane be deposited by exposure to an ammonia atmosphere consisting of an ammonia flow. Plasma enhanced techniques may be employed to deposit the silicon nitride. Pure nitrogen may also be used.

The diffusion membrane may be deposited at an elevated temperature. Temperatures of between 250°C and 400°C are typically employed. However, if the membrane is deposited by sputtering techniques, elevated temperatures are generally not desirable.

The metal (eg. cobalt) layer may be deposited by means selected from electron beam evaporation, sputtering and chemical vapour deposition.

The silicon substrate typically includes a silicon wafer formed of Si(001).

The epitaxial metal silicide (eg. cobalt disilicide) layer formed as a result of the method described above may be used as a smooth, low resistance contact layer at the source and drain regions of a semiconductor device.

If thicker layers of epitaxial $CoSi_2$ are desired, a variety of techniques for increasing the thickness of this layer are contemplated as useful. For instance, after the annealing step, another layer of cobalt may be deposited and annealed (in much the same way as described above). For such additional layers of cobalt

deposited, it is not necessary to precede this with the deposition of a layer of silicon nitride.

The method of this invention may offer particular advantages in light of current consideration and research being done in relation to the use of alternating thin layers of oxides and nitrides (eg. silicon oxide and silicon nitride) as part of a multi-layered stack of oxide and nitride layers for the gate dielectric in future semiconductor devices. As the gate dielectric typically adjoins the region in which epitaxial cobalt disilicide is desired, the use of the method of the present invention may be more convenient than other known methods. It is therefore proposed that, during the fabrication of the oxide-nitride multi-layered stack, the method of the present invention be incorporated so that the nitride layer may be used to form epitaxial cobalt disilicide at the source and drain contacts. For example, when fabricating such a device, the first nitride layer of the multi-layered stack may be a thin layer which extends over the source and drain contact regions. One or more other layers may be added to the stack region. A layer of cobalt may then be applied which covers both the stack region as well as the nitride-coated source and drain contact regions. Upon annealing, epitaxial cobalt disilicide is formed at the source and drain contact regions.

Brief Description of the Drawings

Figure 1 is a schematic representation of a portion of a semiconductor device showing the application of a silicon nitride layer and a cobalt layer prior to the annealing step of the method of this invention.

Figure 2 is a schematic representation of the portion of the semiconductor device of Figure 1 after the annealing step of the method of this invention.

Figures 3 a) to j) are cross-sectional views showing the formation of epitaxial cobalt disilicide at the source and drain contacts of a semiconductor device, in accordance with a preferred embodiment of this invention, during the formation of an oxide-nitride multi-layered stack on the semiconductor device.

As shown in the schematic representation of Figure 1, the method of this invention involves a silicon substrate 10 onto which is deposited a thin layer of silicon nitride 20. On top of this, a thin layer of metallic cobalt 30 is deposited. The layered substrate undergoes annealing at elevated temperatures (typically in excess of 300°C). This causes cobalt from the cobalt layer 30 to diffuse through the silicon nitride layer 20 and to react with the silicon substrate 10. This reaction causes the formation of a layer of epitaxial cobalt disilicide 40 on the surface of

the silicon substrate 10. A residual layer 45 may form above the cobalt disilicide layer 40. This residual layer typically contains residual silicon nitride (and other constituents that may have been present in the annealing ambient). It may also contain some residual cobalt.

A particularly preferred application of the method of this invention is shown in Figures 3 a) to j). In this application, an oxide-nitride multi-layer stack is formed on a silicon substrate 10. Alongside this multi-layer stack, epitaxial cobalt disilicide is formed at the source and drain contacts.

In this application, shallow trench isolation (STI) regions 50 are located near the lateral sides of the device. A layer of oxide 60 (eg. silicon oxide) is deposited on the upper surface 15 of the silicon substrate 10. A central oxide region 65 of the oxide layer is masked and side regions of the oxide layer are etched exposed leaving lateral portions 16, 17 of the upper surface 15. A layer of nitride 70 (eg. silicon nitride) is deposited over the lateral portions 16, 17 of the upper surface 15 and the central oxide region 65.

A layer of polysilicon is then placed over the nitride layer 70. Portions of the polysilicon layer which overlie the lateral portions 16, 17 are removed (for instance, by etching) thereby leaving a layer of polysilicon 75 over the gate region.

A dopant (such as boron fluoride) may then be ion implanted through the nitride layer 70 and subsequently activated by annealing to form p+/n+ shallow junctions. This results in two lightly doped drains (LDD's) 78 being formed between the gate region and the STI regions 50. The layered substrate may then be annealed to electrically activate the implanted impurities.

The remaining edges of the polysilicon layer 75 may be bounded by spacing elements 80. The spacing elements 80 extend through the nitride layer 70 so that they are seated upon the upper surface 15 of the substrate 10. Shallow junctions 79 are then formed in the regions of the LDD's 78.

A layer of cobalt 90 is then deposited over the top of the layered substrate. The layered substrate then undergoes annealing at an elevated temperature, which is typically above 400°C. This forms a layer of polycrystalline cobalt silicide 95 at the gate contact (ie. above the polysilicon layer 75). At the same time, epitaxial cobalt disilicide 100 is formed at the source contact 105 and the drain contact 110 (ie. above the shallow junctions 79).

An etch back procedure is then performed to remove the remaining cobalt of the cobalt layer 90, thereby leaving the layers of polycrystalline cobalt silicide

95 and epitaxial cobalt disilicide 100. The remaining silicon nitride of the silicon nitride layer 70 is also etched back. This etching results in the desired multi-layered gate being formed on the substrate between the source contact and the drain contact.

Example:

By way of example, the method of this invention has been performed with a Si(001) substrate. The substrate was exposed to an ammonia flow, at a pressure of 10E - 6 Torr for 3 hours at 900°C in an ultra-high vacuum (UHV) growth chamber. This formed a thin layer of silicon nitride on the substrate.

A film of cobalt (30 angstroms thickness) was deposited on the nitride surface, at room temperature, by electron beam evaporation of a Co rod.

The layered substrate was then heated to 600°C in the UHV chamber and formation of epitaxial cobalt disilicide ($CoSi_2$) was observed.

As will be apparent to those skilled in the art, the present invention has been described with particular reference to various preferred embodiments of the invention. The invention is not to be understood to be limited to these preferred embodiments. Various modifications of the disclosed embodiments, as well as other embodiments of the invention, will be apparent to persons skilled in the art.

Claims

The claims defining this invention are as follows:

1. A method of forming an epitaxial metal silicide on a silicon substrate including the steps of:

   - depositing on a silicon substrate a diffusion membrane of silicon nitride;
   - depositing on the diffusion membrane a layer of metal; and
   - annealing the layered substrate at an elevated temperature;

   wherein the metal is selected from cobalt and nickel.

2. The method of claim 1, wherein the metal is cobalt and the metal silicide formed is cobalt disilicide.

3. The method of claim 1 or claim 2, wherein the diffusion membrane is sufficiently thin so as to allow metal from the metal layer to diffuse through the membrane at the elevated temperature.

4. The method of claim 3, wherein the thickness of the diffusion membrane is between about 5 and 50 angstroms.

5. The method of claim 4, wherein the thickness of the diffusion membrane is between about 10 and 40 angstroms.

6. The method of any one of claims 1 to 5, wherein the thickness of the metal layer is between about 10 and 130 angstroms.

7. The method of claim 6, wherein the thickness of the metal layer is between about 30 and 80 angstroms.

8. The method of any one of claims 1 to 7, wherein the annealing is effected at a temperature greater than 300°C.

9. The method of claim 8, wherein the annealing is effected at a temperature between about 400°C and 1,000°C.

10. The method of any one of claims 1 to 9, wherein the diffusion membrane is deposited by means selected from sputtering, chemical vapour deposition and exposing the substrate to an ammonia atmosphere.

11. The method of claim 10, wherein the diffusion membrane is deposited by exposing the substrate to an ammonia atmosphere being an ammonia flow.

12. The method of claim 10 or claim 11, wherein the diffusion membrane is deposited at an elevated temperature.

13. The method of any one of claims 1 to 12, wherein the metal layer is deposited by means selected from electron beam evaporation, sputtering and chemical vapour deposition.

14. The method of any one of claims 1 to 13, wherein the silicon substrate is a silicon wafer formed of Si(001).

15. A method of forming a semiconductor device having a multi-layered stack wherein, when a silicon nitride layer is deposited as part of the stack, the layer extends over a source contact region and a drain contact region of the device and said method includes the steps of:

- depositing a layer of metal on the silicon nitride layer, and
- annealing the layered substrate at an elevated temperature;

wherein the metal is selected from cobalt and nickel.

16. The method of claim 15, wherein the metal is cobalt.

17. The method of claim 15 or claim 16, wherein the silicon nitride layer is sufficiently thin so as to allow metal from the metal layer to diffuse through the membrane at the elevated temperature.

18. The method of claim 17, wherein the thickness of the silicon nitride layer is between about 5 angstroms and 150 angstroms.

19. The method of claim 18, wherein the thickness of the silicon nitride layer is between about 10 angstroms and 50 angstroms.

20. The method of any one of claims 15 to 19, wherein the thickness of the metal layer is between about 10 angstroms and 130 angstroms.

21. The method of claim 20, wherein the thickness of the metal layer is between about 30 angstroms and 80 angstroms.

22. The method of any one of claims 15 to 21, wherein the annealing is effected at a temperature greater than 300°C.

23. The method of claim 22, wherein the annealing is effected at a temperature between about 400°C and 1,000°C.

24. A method of forming a semiconductor device substantially as hereinbefore described with reference to any one or more of Figures 1, 2 and 3.

25. A semiconductor device made according to the method of any one of claims 15 to 24.

26. A semiconductor device made according to a process which includes the method of forming epitaxial cobalt disilicide on a silicon substrate according to any one of claims 1 to 14.