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"A SWITCHING CIRCUIT".

The present invention relates to a switching circuit.

A composite technique has been developed to form different kinds of elements in a single semiconductor substrate, to obtain a semiconductor integrated circuit having diverse functions and a high degree of integration.

For instance, a circuit technique for combining bipolar transistors with insulated gate-type field-effect transistors (hereinafter referred to as MOSFET's) has been disclosed in Japanese Patent Publication No. 43997/1972 and in Japanese Patent Laid-Open No. 26181/1977.

Fig. 1 of the accompanying drawings, shows a switching circuit which we have developed and in which a bipolar transistor and an insulated gate-type field effect transistor are combined. The circuit shown in Fig. 1 is an input buffer circuit (switching circuit) for, for example, a Bi-CMOS (bipolar/CMOS mixed type) gate array. The circuit consists of two bipolar transistors Q1, Q2 that constitute an output stage, a CMOS inverter 12 which drives the bipolar transistor Q1 in an inverted manner, and a buffer

amplifier (voltage follower) 14 which drives the other bipolar transistor Q2 in a non-inverted manner.

This circuit operates as described below. A logic signal applied to an input terminal IN comprises two branches. One part of the input is phase inverted by the CMOS inverter 12 and is input to the

base of the transistor Q1 of the output stage. The other part of the input is converted into a low impedance by the buffer amplifier 14 and is input in phase to the base of the other bipolar transistor

Q2 of the output stage. Therefore, the two bipolar transistors Q1, Q2 in the output stage are rendered conductive and are driven in a complementary manner.

When one transistor Q1 is ON (conductive) and the other transistor Q2 is OFF (nonconductive), a changing current is supplied to the load Co through the transistor Q1. When one transistor Q1 is OFF and the other transistor Q2 is ON, the electric charge stored in the load Co is discharged through the other transistor Q2; the capacitive load Co is driven.

The switching circuit has the following features

(a) The CMOS inverter 12 and the buffer amplifier circuit 14 have nearly the same signal transmission speed; hence, the bases of the two transistors Q1,

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Q2 are driven substantially at the same time in an opposite phase relation. Therefore, the two transistors Q1, Q2 are turned on simultaneously for a short time, making it possible to decrease the through current.

5 (b) The two transistors Q1, Q2, which are of the npn-type, can be used to constitute the output stage. When a semiconductor integrated circuit is constructed, therefore, a high cut-off frequency f_T can be easily obtained to realize a high operation speed.

10 (c) When the bipolar transistor Q1 in the output stage is turned off, the electric charge accumulated in the base thereof can be quickly extracted through a MOSFET M2 of the CMOS inverter 12. When the other bipolar transistor Q2 in the output stage is turned
15 off, the electric charge accumulated in the base thereof can be quickly extracted by a low-impedance output of the buffer amplifier circuit 14 constituting a voltage follower. That is, the two bipolar transistors Q1, Q2 in the output stage, respectively, have paths for effectively extracting
20 the electric charge accumulated in the bases, and whereby the switching time from ON to OFF is conspicuously shortened.

(d) Since a power source terminal p1 of the buffer amplifier 14 is connected to the output terminal OUT,
25 the discharging current of the capacitive load C_o con-

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connected to the output terminal OUT flows not only to the other transistor Q2 in the output stage but also to the buffer amplifier 14 as an operation current from the first power source terminal p1. At the moment
5 when the logic state of the buffer output OUT changes from "H" (high logic level) to "L" (low logic level), the electric charge stored in the load Co is allowed to discharge through the transistor Q2 and buffer
amplifier 14. Therefore, the driving power is greatly
10 reinforced for the capacitive load Co, especially at the moment of breaking.

(e) Further, since the CMOS inverter 12 and the buffer
amplifier 14 have high input impedances, there is ob-
tained a high input impedance as viewed from the input
15 side.

(f) The first power source terminal p1 of the buffer
amplifier 14 is connected not to the power source V_{DD}
but to the collector (output terminal OUT) of the
transistor Q2 of the output stage, and the base poten-
20 tial of the transistor Q2 is not higher than the col-
lector potential thereof. Therefore, the transistor
Q2 is not saturated.

The switching circuit exhibits excellent features
as described above. Further study of the problem
25 has enabled us to realize the switching circuit

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in the form of an integrated circuit. We have found that in designing constants for the circuit, many contrivances are necessary to satisfy the high-speed characteristics and the low power consumption that are strictly necessary for the switching circuit.

It is an object of the present invention to provide a novel switching circuit having high performance, that can be suitably realized in the form of a semiconductor integrated circuit.

10 According to the present invention there is provided a switching circuit including:

(i) first and second bipolar transistors having collector-emitter paths which are connected in series across a first operation potential point and a second operation potential point to provide an output signal for said switching circuit at an output terminal coupled between the respective collector-emitter paths of said bipolar transistors;

(ii) a CMOS inverter circuit connected between an input terminal of said switching circuit and the base of the first bipolar transistor; and

(iii) a source follower circuit connected between the input terminal and the base of the second bipolar transistor; wherein:-

25 (a) the CMOS inverter circuit has a first MOSFET of a first conductivity type and a second MOSFET of a second conductivity type;

(b) the source follower circuit has a third MOSFET of the second conductivity type and resistance means;

(c) the second and third MOSFETs have a substantially equal logic threshold voltage in the absence of substrate effect;

(d) the resistance means has a predetermined resistance such that the turn-on and turn-off times of the second bipolar transistor are shorter than a predetermined value;

(e) the first and second MOSFETs have predetermined logic threshold voltages in the absence of substrate effect, and channel conductances such that the CMOS inverter will have a desired logic threshold voltage;

15 and

(f) the channel conductance of the third MOSFET is so set that the logic threshold voltage of the source follower circuit is substantially equal to the desired logic threshold voltage of the CMOS inverter circuit.

20 inverter circuit.

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With the structure of the above switching circuit,
a high-speed operation is obtained which permits
little through current to flow without increasing
the complexity of the process of integrated circuit
5 manufacture.

The present invention will now described in greater
detail by way of example with reference to the remaining
figures of the accompanying drawings, wherein:

Figure 2 is a circuit diagram of a first embodiment
10 of a switching circuit, the circuit configuration of
which is substantially equivalent to the circuit shown
in Fig. 8 of our European Specification No. 0099100.

Figure 3 is a graph showing the relation between the resistance of the resistor R and the threshold voltage V_{LT2} of the source follower circuit;

Figure 4 is a graph showing the relation
5 between the resistance of the resistor R and the turn-on and turn-off times of the bipolar transistor Q2;

Figure 5 is a circuit diagram illustrating a second embodiment of the switching circuit;

10 Figure 6 is a circuit diagram illustrating a third embodiment of the switching circuit; and

Figure 7 is a circuit diagram illustrating a fourth embodiment of the switching circuit.

The present invention was achieved
15 through the study of how to reduce the through current of the switching circuit, how to increase the signal transmission speed, and how to realize the switching circuit in the form of a semiconductor integrated circuit.

20 Therefore, the progress of study by us will first be described below, and the features of

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the present invention will then be described.

The circuit shown in Fig. 2 was studied by us through the process as mentioned below.

I. Consideration of logic threshold voltage V_{LT1} of the CMOS inverter 12:

The substrate effect takes place if the source S of NMOS-FET M_2 is connected to the base of the transistor Q_2 as indicated by a solid line. Here, the term "substrate effect" means that if the source potential so changes as to become higher than or lower than earth potential while the potential of the silicon substrate has been fixed at earth potential, the practical threshold voltage of the MOSFET changes depending upon the change in the source potential.

If the substrate effect is taken into consideration, therefore, the threshold voltage V_{thN} of NMOSFET M_2 in practice is given by the following well known equation:

$$\begin{aligned} V_{thN} &= V_{thNO} + \Delta V_{th} \\ &= V_{thNO} + K(\sqrt{2\phi_F - V_{BS}} - \sqrt{2\phi_F}) \\ &= V_{thNO} + K(\sqrt{2\phi_F + V_{BE}} - \sqrt{2\phi_F}) \quad \dots\dots (1) \end{aligned}$$

where V_{thNO} denotes threshold voltage when there is no substrate effect,

ΔV_{th} denotes shifted amount caused by the substrate effect,

K denotes a constant,

$2\phi_F$ denotes voltage that is twice as great as the Fermi potential ϕ_F ,

V_{BS} denotes voltage across the substrate and the source of the NMOSFET M_2 , and

V_{BE} denotes voltage across the base and the emitter of the transistor Q_2 .

Next,

$$\alpha = \sqrt{\frac{\beta_P}{\beta_N}} = \sqrt{\frac{\beta_{PO} \cdot \frac{W_P}{L_P}}{\beta_{NO} \cdot \frac{W_N}{L_N}}}$$

is defined below.

In the above equation, β_P and β_N denote conductance (constant) of the p-channel MOSFET and conductance of the n-channel MOSFET, respectively, and β_{PO} and β_{NO} denote values of β_P and β_N , respectively, when $W/L = 1$.

Then, a logic threshold voltage V_{LT1} of the CMOS inverter 12 is given by,

$$\begin{aligned} V_{LT1} &= \frac{\alpha(V_{DD} + V_{thPO}) + V_{thN} + V_{BE}}{1 + \alpha} \\ &= \frac{\alpha(V_{DD} + V_{thPO}) + V_{thNO} + K(\sqrt{2\phi_F + V_{BE}} - \sqrt{2\phi_F}) + V_{BE}}{1 + \alpha} \end{aligned} \quad \dots(2)$$

where V_{DD} is power source voltage.

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Generally, α is set to a suitable value to so design the circuit that $V_{LT1} \approx \frac{1}{2}V_{DD}$. Here, the threshold voltage V_{LT1} of the CMOS inverter stands for a gate voltage applied to the CMOS inverter when there flows an electric current substantially equally into the PMOSFET M_1 and the NMOSFET M_2 that constitute the CMOS inverter.

II. Consideration of the logic threshold voltage

V_{LT2} of the NMOS source follower circuit:

It is considered that the logic threshold voltage V_{LT2} for turning the NMOSFET M_3 and the transistor Q_2 from off to on, is

$$V_{LT2} \approx V_{thN} + V_{BE}$$

$$\approx V_{thNO} + V_{BE} \quad \dots (3)$$

III. Consideration of through currents of the transistors

Q_1, Q_2 :

To prevent the flow of through currents of the transistors Q_1, Q_2 , the relation $V_{LT1} \approx V_{LT2}$ must hold true. If $V_{DD} = 5$ volts, $V_{LT1} \approx 2.5$ volts. In order for the logic threshold voltage V_{LT2} to be 2.5 volts when $V_{BE} = 0.6$ volt, it is necessary to implant impurity ions into the channel region of the NMOSFET

M_3 , so that V_{thNO} will become 1.9 volts. Here, V_{thPO} of M_1 is -0.6 volt and V_{thNO} of M_2 is +0.6 volt.

To set the threshold voltage V_{thNO} of NMOSFET M_3 to 1.9 volts, therefore, the individual MOSFET's, M_2 and M_3 must be formed through individual processes, or must be formed through processes that are partly common to each other; then, the desired threshold voltages of each of the MOSFET's must be obtained through additional processes.

IV. Consideration of the NMOS source follower M_3 and the logic threshold voltage V_{LT2} of the transistor Q_2 :

We have carried out a further study concerning the logic threshold voltage V_{LT2} , and have found the fact that the logic threshold voltage V_{LT2} is not simply found from the equation (3) above but varies with the resistance of the resistor R as well as β_{NO} of NMOSFET M_3 and W_N/L_N of NMOSFET M_3 , as shown in Fig. 3.

The reason why the logic threshold voltage V_{LT2} varies according to the relation shown in Fig. 3 will be analyzed below.

Here, if $\beta_N = \beta_{NO} \frac{W_N}{L_N}$, the current that flows through the drain-source path of the NMOSFET M_3 is:

$$I_{DS} = \frac{\beta_N}{2} (V_{GS} - V_{thN})^2 \quad \dots\dots (4)$$

where V_{GS} denotes the voltage across the gate

and the source of NMOSFET M_3 .

Input voltage V_{IN} at the input terminal IN is:

$$V_{IN} = V_{GS} + R \cdot I_{DS} \quad \dots\dots (5)$$

The transistor Q_2 is rendered conductive when
5 the voltage drop $R \cdot I_{DS}$ of the resistor R satisfies
the following equation:

$$V_{BEQ_2} = R \cdot I_{DS} \quad \dots\dots (6)$$

From equations (5), (6), there is obtained,

$$V_{GS} = V_{IN} - V_{BE} \quad \dots\dots (7)$$

10 From equations (4), (7), there is further obtained,

$$I_{DS} = \frac{\beta_N}{2} (V_{IN} - V_{BE} - V_{thN})^2 \quad \dots\dots (8)$$

If both sides of the equation (8) are multiplied
by R, and if $V_{BE} = R \cdot I_{DS}$ is taken into consideration,
there is obtained the following equation:

$$15 \quad V_{BE} = R \cdot I_{DS} = \frac{\beta_N \cdot R}{2} (V_{IN} - V_{BE} - V_{thN})^2 \quad \dots\dots (9)$$

By modifying equation (9), there is obtained,

$$\begin{aligned} \frac{2V_{BE}}{\beta_N \cdot R} &= V_{IN}^2 + V_{BE}^2 + V_{thN}^2 - 2V_{IN} \cdot V_{BE} \\ &\quad + 2V_{BE} \cdot V_{thN} - 2V_{thN} \cdot V_{IN} \quad \dots (10) \end{aligned}$$

By modifying equation (10), there is further obtained,

$$V_{IN}^2 - 2(V_{BE} + V_{thN}) \cdot V_{IN} + (V_{BE} + V_{thN})^2 - \frac{2V_{BE}}{\beta_N \cdot R} = 0 \quad \dots (11)$$

If V_{IN} is solved,

$$V_{LT2} = V_{IN} = \frac{2(V_{BE} + V_{thN}) \pm \sqrt{4(V_{BE} + V_{thN})^2 - 4\left\{(V_{BE} + V_{thN})^2 - \frac{2V_{BE}}{\beta_N \cdot R}\right\}}}{2}$$

$$= V_{BE} + V_{thN} + \sqrt{\frac{2V_{BE}}{\beta_{NO} \cdot \frac{W_N}{L_N} \cdot R}} \quad \dots (12)$$

From equation (12), it will be understood that the logic threshold voltage V_{LT2} also varies depending upon β_{NO} , W_N/L_N and R .

Fig. 3 shows the relation between the resistance of the resistor R and the threshold voltage V_{LT2} of the NMOSFET M_3 relying upon the results measured according to the present invention, wherein a solid line represents the relation when $W_N/L_N = 10\mu m/2\mu m$, a dot-dash chain line represents the relation when $W_N/L_N = 20/2$, and a two-dot chain line represents the relation when $W_N/L_N = 40/2$.

V. Consideration of the relation between the resistance of the resistor R and turn-on time t_{ON} and turn-off time t_{OFF} of the transistor Q_2 :

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Fig. 4 shows the relation between the resistance of the resistor R and t_{ON} , t_{OFF} , that is practically examined.

In Fig. 4, the solid line represents the turn-on time t_{ON} , and a dotted line represents the turn-off time t_{OFF} .

The following facts will be understood from Fig. 4.

(1) To set t_{ON} and t_{OFF} to be shorter than 2 nsec., the resistance must be selected to be $1K\Omega < R < 30K\Omega$

(range A).

(2) To set t_{ON} and t_{OFF} to be shorter than 1.5 nsec., the resistance must be selected to be $3K\Omega < R < 20K\Omega$

(range B).

(3) To set t_{ON} and t_{OFF} to be shorter than 1.25 nsec., the resistance must be selected to be $4K\Omega < R < 16K\Omega$

(range C).

In the foregoing were mentioned the results studied by us. The specific construction of the circuit shown in Fig. 2 will now be described in greater detail.

In Fig. 2, the source S of the n-channel MOSFET M_2 may be either earthed as indicated by a dotted line or be connected to the base of the transistor Q_2 as indicated by a solid line. When the source of the

NMOSFET M_2 is connected to the base of the transistor Q_2 , however, it becomes difficult to design the threshold voltage V_{LT1} of the CMOS inverter. When the source of the NMOSFET M_2 is earthed. it is easy to design the threshold voltage V_{LT1} .

The circuit of Fig. 2 is designed in four steps:

Step 1: The threshold voltage V_{thNO} of NMOSFET M_2 is set to be substantially equal to the threshold voltage V_{thNO} of NMOSFET M_3 . For instance, NMOSFET M_2 , M_3 are formed on the same chip by the same manufacturing process.

Step 2: The resistance R is set to lie within a predetermined range to set t_{ON} and t_{OFF} of the transistor Q_2 to be shorter than a predetermined value. For instance, to set t_{ON} , t_{OFF} to be shorter than 2 nsec., the resistance R is selected to lie within the aforementioned range A.

Step 3: Design the threshold voltage V_{LT1} of the CMOS inverter which consists of PMOSFET M_1 and NMOSFET M_2 . That is, when the source of the NMOSFET M_2 has been earthed, the constant of the parameter is determined as:

$$V_{LT1} = \frac{\alpha(V_{DD} + V_{thPO}) + V_{thNO}}{1 + \alpha} \approx \frac{1}{2} V_{DD}$$



When the source of the NMOSFET M_2 has been connected to the base of the transistor Q_2 , the threshold voltage should be designed in accordance with the equation (2) mentioned earlier.

Step 4: Resistance R over the range mentioned in Step 2 is used so that the threshold voltage V_{LT2} of the NMOSFET M_3 will approach the threshold voltage V_{LT1} that is set in Step 3, and values β_{NO} , W_N/L_N are set in accordance with the equation (12), such that $V_{LT1} \approx V_{LT2}$. Here, however, β_{NO} serves as a constant that does not change once the manufacturing process is determined. In practice, therefore, $V_{LT1} \approx V_{LT2}$ is accomplished by changing W_N/L_N of NMOSFET M_3 .

Described below is a specific example when the above-mentioned design procedure is followed (the source of NMOSFET M_2 is earthed in Fig. 2).

Step 1: Set V_{thNO} of NMOSFET's M_2 and M_3 to be equal to each other.

Step 2: Set the resistance R to be $8K\Omega$ so that the turn-on and turn-off times of the transistor Q_2 will be shorter than 1.25 nsec.

Step 3: Set the value W_p/L_p of PMOSFET M_1 constituting the CMOS inverter to be 30/2, and set the value W_N/L_N of NMOSFET M_2 to be 10/2.

Here, $\beta_{PO} = 10 \times 10^{-6} \frac{[U]}{[V]}$

$$\beta_{NO} = 30 \times 10^{-6} \frac{[U]}{[V]}$$

$$\alpha = \sqrt{\frac{10 \times 30/2}{30 \times 10/2}} = \sqrt{1} = 1$$

$$V_{DD} = 5 \text{ volts}$$

5 Therefore,

$$\begin{aligned} V_{LT1} &= \frac{\alpha (V_{DD} + V_{thPO}) + V_{thNO}}{1 + \alpha} \\ &= \frac{5 + (-0.6) + 0.6}{2} = 2.5 \text{ (V)} \end{aligned}$$

10 Step 4: From the equation (12), there is obtained,

$$V_{LT2} - V_{BE} - V_{thN} = \sqrt{\frac{2V_{BE}}{\beta_{NO} \frac{W_N}{L_N} \cdot R}} \quad \dots (13)$$

Since $V_{LT1} = 2.5 \text{ V} \approx V_{LT2}$, if

$$V_{LT2} = 2.5 \text{ V}$$

15 $V_{BE} = 0.6 \text{ V}$

$$V_{thN} = 0.6 \text{ V}$$

are inserted into the equation (13), there is obtained,

$$(1.3)^2 = \frac{1.2 [V]}{30 \times 10^{-6} \frac{[U]}{[V]} \cdot \frac{W_N}{L_N} \cdot 8 \times 10^3 (\Omega)} \quad \dots (14)$$



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If W_N/L_N is found from the equation (14), we obtain $W_N/L_N \approx 5/2$. That is, the value W_N/L_N of NMOSFET M_3 should be set to 5/2.

5 The above-mentioned structure makes it possible to obtain the following effects in addition to the effects mentioned in relation to the known switching shown in Figure 1.

10 (a) The threshold voltage V_{thNO} (when there is no substrate effect) of NMOSFET M_2 constituting the CMOS inverter 12 is set to be substantially equal to the threshold voltage V_{thNO} (when there is no substrate effect) of NMOSFET M_3 . This means that the NMOSFET's M_2 and M_3 can be formed simultaneously in the semiconductor substrate through the same
15 manufacturing process, thereby simplifying the manufacture of integrated circuits.

(b) Resistance of the resistor R is so determined that the bipolar transistor Q_2 in the output stage exhibits turn-on time and turn-off time of desired
20 values (high speeds). Therefore, the high switching speed of the transistor Q_2 is correctly determined.

(c) Value W_N/L_N of the NMOSFET M_3 is so adjusted that the logic threshold voltage V_{LT2} of NMOSFET M_3 approaches the logic threshold voltage V_{LT1} of the
25 CMOS inverter. Therefore, the two transistors Q_1

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and Q_2 in the output stage are driven at nearly the same timing in a complementary manner, making it possible to minimize the through current that flows instantaneously through the transistors Q_1, Q_2 .

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Fig. 5 shows the structure of a switching circuit according to a second embodiment of the present invention. What makes this embodiment different from the circuit structure of embodiment 1 is that the resistor
10 R in this embodiment is formed by utilizing the resistance of a MOSFET M_4 while it is conductive.

Similar to embodiment 1, the circuit in this embodiment is designed in five steps.

Step 1: The threshold voltage V_{th0} of NMOSFET M_2 is
15 set to be substantially equal to the threshold voltage V_{th0} of NMOSFET M_3 .

Step 2: To set t_{ON} of the transistor Q_2 (time required for turning Q_2 from off to on) to be shorter than a predetermined value, the resistance R of NMOSFET
20 M_4 while it is conductive is set to lie within a predetermined range.

To set t_{ON} to be shorter than 2 nsec., R must be greater than 1K Ω .

To set t_{ON} to be shorter than 1.5 nsec., R must
25 be greater than 3 K Ω .

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To set t_{ON} to be shorter than 1.25 nsec., R must be greater than $4K\Omega$.

Step 3: In order to set t_{OFF} required for turning the transistor Q_2 from on to off to be shorter than a predetermined value, the resistance R of NMOSFET M_4 when it is turned from off to on is set to lie within a predetermined range, the NMOSFET M_4 being driven by a current that flows through a path consisting of input terminal IN, PMOSFET M_1 , and transistor Q_1 .

To set t_{OFF} to be shorter than 2 nsec., $R \leq 30 K\Omega$.

To set t_{OFF} to be shorter than 1.5 nsec., $R < 20K\Omega$.

To set t_{OFF} to be shorter than 1.25 nsec., $R < 16K\Omega$.

Step 4: Design the threshold voltage V_{LT1} of the CMOS inverter consisting of M_1 and M_2 . When the source of NMOSFET M_2 is earthed, design the threshold voltage according to the following equation,

$$V_{LT1} = \frac{\alpha(V_{DD} + V_{thPO}) + V_{thNO}}{1 + \alpha} = \frac{1}{2} V_{DD}$$

When the source of NMOSFET M_2 is connected to the base of the transistor Q_2 , design the threshold voltage according to the aforementioned equation (2).

Step 5: Use the resistance R of NMOSFET M_4 over the ranges of Steps 2 and 3, so that V_{LT2} will approach

V_{LT1} that has been set in Step 4, and set β_{NO} and W_N/L_N in accordance with the equation (12) to accomplish the relation $V_{LT1} = V_{LT2}$.

Fig. 6 is a diagram showing a switching circuit according to a third embodiment of the present invention.

The feature of this circuit resides in the provision of a collector-earthed pnp-type bipolar transistor Q_3 in the input portion.

If the circuit is based on the prerequisite that an input signal (high level $V_{1H} = 2.0$ V, threshold level $V_{Ith} = 1.3$ V, low level $V_{1L} = 0.8$ V) of the TTL level is applied to the input terminal IN, the threshold voltage V_{Ith} of the transistor Q_3 must be set to 1.3 volts. In this case, the design should be carried out according to Steps 1 to 4, such that $V_{LT1} = V_{LT2} = V_{Ith} + V_{BE} = 1.3V + 0.6V = 1.9$ volts.

Fig. 7 is a diagram showing a switching circuit having a NOR logic function according to a fourth embodiment of the present invention. As shown in Fig. 7, the switching circuit is provided with a NOR logic function relying upon a plurality of MOSFET's $M1A$, $M1B$, $M2A$, $M2B$, $M3A$ and $M3B$.

The design procedure is the same as the one described above.

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CLAIMS:-

1. A switching circuit including:

(i) first and second bipolar transistors having collector-emitter paths which are connected in series across a first operation potential point and a second operation potential point to provide an output signal for said switching circuit at an output terminal coupled between the respective collector-emitter paths of said bipolar transistors;

(ii) a CMOS inverter circuit connected between an input terminal of said switching circuit and the base of the first bipolar transistor; and

(iii) a source follower circuit connected between the input terminal and the base of the second bipolar transistor; wherein:-

(a) the CMOS inverter circuit has a first MOSFET of a first conductivity type and a second MOSFET of a second conductivity type;

(b) the source follower circuit has a third MOSFET of the second conductivity type and resistance means;

(c) the second and third MOSFETs have a substantially equal logic threshold voltage in the absence of substrate effect;

(d) the resistance means has a predetermined resistance such that the turn-on and turn-off times of the second bipolar transistor are shorter than a predetermined value;



(e) the first and second MOSFETs have predetermined logic threshold voltages in the absence of substrate effect, and channel conductances such that said CMOS inverter will have a desired logic threshold voltage; and

(f) the channel conductance of said third MOSFET is so set that the logic threshold voltage of said source follower circuit will be substantially equal to said desired logic threshold of the CMOS inverter circuit.

2. A switching circuit according to claim 1, wherein said resistance means consists of a fourth MOSFET, the gate thereof being controlled by the level of an output signal produced by the switching circuit.

3. A switching circuit according to claim 1, wherein the emitter of a collector-earthed pnp-type transistor is connected to the input terminal, so that an input signal is applied to the base of the pnp-type transistor.

4. A switching circuit according to any one of the preceding claims, wherein the switching circuit is provided with a logic function.

5. A switching circuit according to claim 1, wherein said first and second MOSFETs are coupled to



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have their gates both connected to said input terminal
and their source-drain paths connected in series
between said first and second operation potentials.



6. A switching circuit according to claim 1, wherein said third MOSFET has its gate connected to the input terminal, wherein said resistance means is coupled to the source of the third MOSFET and wherein
5 the base of said second bipolar transistor is connected to the junction between the source of the third MOSFET and the resistance means.

7. A switching circuit according to claim 5, wherein said third MOSFET has its gate connected to the input
10 terminal, wherein said resistance means is connected to the source of the third MOSFET and wherein the base of said second bipolar transistor is connected to the junction between the source of the third MOSFET and the resistance means.

15 8. A switching circuit according to claim 1, wherein said third MOSFET has its gate connected to the input terminal, wherein said resistance means is coupled to the source of the third MOSFET, wherein the base of said second bipolar transistor is coupled to
20 the junction between the source of the third MOSFET and the resistance means, and wherein said first and second MOSFETs are connected so that their gates are both connected to the input terminal and their source-drain paths connected in series between the first operating
25 point and the junction between the source of the third MOSFET, the resistance means and the base of the second bipolar transistor.





9. A switching circuit according to claim 1,
wherein a plurality of said first MOSFETs, a plurality
of said second MOSFETs and a plurality of said third
MOSFETs are provided, wherein a first input terminal
5 for receiving a first input signal is connected to provide
said first input signal to predetermined ones of the
first, second and third MOSFETs while a second input
terminal for receiving a second input signal is connected
to provide said second input signal to predetermined
10 ones of said first, second and third MOSFETs, and wherein
said plurality of first, second and third MOSFETs are
arranged to provide a logic function output for said
first and second input signals.

10. A switching circuit according to claim 9,
15 wherein said plurality of first MOSFETs are arranged
in series with one another, and wherein said plurality
of second MOSFETs and said plurality of third MOSFETs
are arranged in parallel to one another so that said
switching circuit provides a NOR logic function output
20 for said first and second input.

11. A switching circuit constructed and arranged
to operate substantially as herin described with reference
to and as illustrated in Fig. 2, or Fig. 5, or Fig. 6,
or Fig. 7 of the accompanying drawings.

