WHAT IS CLAIMED IS:

1. A semiconductor memory device comprising:

a cell array including a first row block and a second row block;

a bit line sense amplifier block configured to sense data stored in a selected one of the first row block and the second row block, the bit line sense amplifier block comprising a plurality of bit line sense amplifiers;

a local sense amplifier configured to latch the sensed data transferred from the bit line sense amplifier block; and

a switch configured to connect the local sense amplifier to a selected one of a first global data line and a second global data line in response to a select signal,

wherein the second row block is located at a first edge of the cell array, and

wherein the switch connects the local sense amplifier with the first global data line when the first row block is activated and connects the local sense amplifier with the second global data line when the second row block is activated.

2. The semiconductor memory device of claim 1, wherein each of the bit line sense amplifiers are connected to a corresponding bit line arranged in the first row block and a corresponding bit line arranged in the second row block.

3. The semiconductor memory device of claim 1 or claim 2, further comprising:

a third row block that is activated simultaneously with the second row block;

a second bit line sense amplifier block configured to sense second data stored in the third row block, the second bit line sense amplifier block comprising a plurality of second bit line sense amplifiers; and

a second local sense amplifier configured to output the second data transferred from the second bit line sense amplifier block to the first global data line.

4. The semiconductor memory device of claim 3, wherein the third row block is located at a second edge of the cell array opposite to the first edge of the cell array.

5. The semiconductor memory device of claim 1, wherein the select signal is generated in response to activation of word line of the second row block such that the switch is connected with the local sense amplifier and the second global data line.

6. The semiconductor memory device of any one of claims 1 to 5, further comprising:

a row decoder configured to generate the select signal in response to a received row address.

7. The semiconductor memory device of any one of claims 1 to 6,

wherein the cell array is formed by a number of row blocks that are separated from each other by bit line sense amplifier blocks, and

wherein the number of row blocks is an even number.

8. The semiconductor memory device of any one of claims 1 to 7, wherein each of the plurality of bit line sense amplifiers of the bit line sense amplifier block is connected to two bit lines to form an open bit line structure.

9. A semiconductor memory device which includes a first global data line and a second global data line, comprising:

a first edge row block forming one end of a cell array;

a second edge row block forming an opposite end of the cell array;

a first inner row block interposed between the first edge row block and the second edge row block;

a first local sense amplifier configured to output first data sensed from the first edge row block to the first global data line;

a second local sense amplifier configured to output second data sensed from the second edge row block to an edge global data line;

a third local sense amplifier configured to output third data sensed from the first inner row block to the second global data line;

a multiplexer configured to selectively connect two of the first global data line, the second global data line, and the edge global data line with an input/output sense amplifier in response to a select signal;

a first bit line sense amplifier configured to sense the first edge row block and to provide a result sensed from the first edge row block as the first data to the first local sense amplifier; and

a second bit line sense amplifier configured to sense the second edge row block and to provide a result sensed from the second edge row block as the second data to the second local sense amplifier.

10. The semiconductor memory device of claim 9, further comprising:

a row decoder configured to generate the select signal in response to a row address.

11. The semiconductor memory device of claim 9 or claim 10, wherein the multiplexer is configured to connect the first global data line and the second global data line with the input/output sense amplifier in response to a selection of the first inner row block.

12. The semiconductor memory device of claim 9 or claim 10, wherein the multiplexer is configured to connect the first global data line and the edge global data line with the input/output sense amplifier in response to the first edge row block or the second edge row block being selected.

13. The semiconductor memory device of any one of claims 9 to 12, further comprising:

a row decoder configured to select the first edge row block and the second edge row block at the same time.

14. The semiconductor memory device of any one of claims 9 to 13,

wherein the first bit line sense amplifier and the second bit line sense amplifier are each connected to two corresponding bit lines in an open bit line structure.

15. The semiconductor memory device of any one of claims 9 to 14, wherein the multiplexer is formed in a peripheral area of the cell array.

16. A data path configuration method of a semiconductor memory device comprising:

receiving an address for selecting at least one of a plurality of row blocks included in a cell array;

determining whether the address corresponds to an edge row block among the plurality of row blocks of the cell array; and

connecting a local sense amplifier corresponding to the selected at least one row block to an even global data line or an odd global data line depending on the determination result,

wherein a bit line sense amplifier is included in the cell array and is connected to bit lines.

17. The data path configuration method of claim 16,

wherein the edge row block corresponds to at least one of a first edge row block and a second edge row block placed at opposite sides of the cell array, and

wherein the first edge row block and the second edge row block are selected.

18. The data path configuration method of claim 17,

wherein connecting a local sense amplifier comprises connecting a first local sense amplifier having access to the first edge row block to the even global data line, and connecting a second local sense amplifier having access to the second edge row block to the odd global data line.

19. The data path configuration method of any one of claims 16 to 18, wherein the bit line sense amplifier is connected to the bit lines with an open bit line structure.

20. The data path configuration method of any one of claims 16 to 19,

wherein the cell array is formed by a number of row blocks that are separated from each other by bit line sense amplifier blocks,

wherein the number of row blocks is an even number.