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(54) IMPROVEMENTS IN OR RELATING TO SEMICONDUCTOR CIRCUITS

(71) We, WESTERN ELECTRIC COMPANY, INCORPORATED, of 195, Broadway, New York City, New York State, United States of America, a Corporation organised and existing under the laws of the State of New York, United States of America, do hereby declare the invention for which we pray that a patent may be granted to us, and the method by which it is to be performed, to be particularly described in and by the following statement:—

This invention relates to semiconductor circuits.

Integrated circuits are being made and sold in substantial numbers at present and are expected to be used more extensively in the future as their size and cost decrease. As a general rule, the cost of fabricating an integrated circuit varies directly with the semiconductor chip area occupied by the circuit. Any reduction of the area occupied by an integrated circuit is therefore advantageous both because the smaller circuit occupies less space wherever it is ultimately used and its cost is lower.

A known integrated circuit static shift register stage using insulated-gate field-effect transistor (IGFET) devices includes a pair of interconnected IGFET amplifiers. A power supply is connected to the pair of IGFET amplifiers by way of the semiconductor substrate and a metallized lead which extends across the semiconductor chip to all stages of the shift register. The power supply applies bias potential to the amplifiers by way of the substrate, and the metallized lead provides a ground return path from the amplifiers back to the power supply. Within the stage, the IGFET amplifiers are interconnected so that a data input signal is transferred from an input terminal to an output terminal in two steps. In the first step, the data input signal is transferred from the input terminal to a first IGFET amplifier.

[Price 25p]

During the second step, the data signal is transferred from the first IGFET amplifier to a second IGFET amplifier. An output terminal is connected to the second IGFET amplifier for indicating which one of two stable operating conditions of the second IGFET amplifier exists at any time. The indicated operating condition reflects the state of a data bit stored therein.

The two transfer steps are controlled by two alternatively timed clock-drive phases. The first clock-drive phase transfers the data input signal from the input terminal to the first IGFET amplifier. The second clock-drive phase transfers the data signal from the first IGFET amplifier to the second IGFET amplifier. After the data signal is transferred to the second IGFET amplifier, a feedback path between the output terminal and the first IGFET amplifier is activated in response to the first clock-drive phase for holding the first and second IGFET amplifiers in their existing operating conditions until the next shift cycle commences. These two clock-drive phases are applied to the IGFET amplifiers by way of two additional metallized leads, which also extend across the semiconductor chip to all stages of the shift register.

This known IGFET static shift register stage therefore requires three metallized leads extending across the entire semiconductor chip. Each of these three leads occupies a significant portion of the semiconductor chip area utilized for the shift register.

According to this invention a semiconductor circuit includes a plurality of transistor shift register stages connected in tandem, a first metallised conductor connected in common to all said stages for applying a first clock-drive phase thereto, and a second metallised conductor connected in common to all said stages for

applying a second clock-drive phase there-
to substantially out of phase with said first
clock-drive phase, each of said stages being
such and being so-connected to said con-
ductors that, in operation, each of said
conductors serves to alternatively provide
its respective clock-drive phase to said
stages and a return path from said stages
to ground.

- 10 Each of said stages may include a pair
of insulated gate field effect transistors
cross-coupled through a pair of cross-
coupling devices, a pair of load devices
each coupled to a different one of said pair
15 of transistors, said first conductor being
for applying said first clock-drive phase to
control conduction through said pair of
cross-coupling devices and through said
pair of load devices, an input device, and
20 a third load device coupled to one of said
pair of transistors, said second conductor
being for applying said second clock-drive
phase to control conduction through said
input device and said third load device.
- 25 Each of said stages may include first
second, third, fourth fifth, sixth, seventh
and eighth transistor devices each having
source, gate and drain electrodes, means
for connecting the source electrodes of
30 said first and second devices to a reference
potential source, means connecting the
drain electrode of said first device to the
source electrode of said third device, means
connecting the drain electrode of said third
35 device to the gate electrode of said second
device, means connecting the drain electrode
of said second device to the source electrode
of said fourth device, means connecting the
drain electrode of said fourth device to the
40 gate electrode of said first device, means
connecting the source electrode of said
fifth device to the drain electrode of said
first device, means connecting the source
electrode of said sixth device to the drain
45 electrode of said second device, means con-
nected to said first conductor and inter-
connecting the gate electrodes of said third
and fourth devices with the gate and drain
electrodes of said fifth and sixth devices,
50 means connecting the drain electrode of
said seventh device to the gate electrode
of said first device, means connecting the
source electrode of said eighth device to
the drain electrode of said second device,
55 and means connected to said second con-
ductor and interconnecting the gate elec-
trode of said seventh device with the gate
and drain electrodes of said eighth device.

The circuit may include a first clock-
drive phase providing means coupled to
60 said first conductor, and a second clock-
drive phase providing means coupled to
said second conductor, said second clock-
drive phase being substantially out of phase
65 with said first clock-drive phase.

The circuit may be fabricated in integ-
rated circuit form wherein said stages
share a common substrate.

Preferably each said device is an
insulated gate field effect transistor device.

The invention will now be described by
way of example with reference to the ac-
companying drawing in which:

FIG. 1 is a schematic diagram of an
embodiment of a shift register stage in
75 accordance with the invention;

FIG. 2 is a timing diagram of clock-
drive phases for controlling the stage shown
in FIG. 1;

FIG. 3 is a block diagram of a shift
80 register in accordance with the invention;

FIG. 4 is a block diagram of another
shift register in accordance with the in-
vention; and

FIG. 5 is a cross-sectional view of an
IGFET device.

Referring now to FIG. 1, a static IGFET
shift register stage 10, which is but one
of several stages fabricated on one semi-
conductor chip, includes eight IGFET
90 devices which are interconnected to receive
signals at an input terminal 12 and produce
output signals at an output terminal 14.

Each of the IGFET devices of FIG. 1 is
a P-channel enhancement-mode IGFET
95 wherein conduction is accomplished by
majority carriers. Each device has a gate,
a source, and a drain electrode. By apply-
ing to the gate electrode of any device a
negative potential with respect to the
100 potential of its source electrode, P-type
majority carriers are generated in a channel
extending from the source to the drain
electrodes. The channel from source to
drain is a continuous conductive path for
105 majority carriers which are swept from the
source to the drain by a drain potential
which is negative with respect to the source
electrode potential.

Operation of the stage may be better
110 understood if it is appreciated that each
IGFET device will conduct from source to
drain when a potential, exceeding a known
threshold and of negative polarity with
respect to the potential of the source elec-
115 trode of the same transistor, is applied to
the gate electrode. Conversely, each tran-
sistor will be cut off when the source elec-
trode voltage is applied to the gate elec-
trode.

Other types of IGFET devices, such as
N-channel enhancement-mode IGFET
devices, can be used in a circuit like the
circuit of FIG. 1 if appropriate changes in
the polarities are made.

The shift register stage includes two
transistors 16 and 18 which are cross-
coupled drain to gate for bistable circuit
operation. A bias potential is applied to
the source electrodes of the transistors 16
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and 18 by way of a semiconductor substrate 15 that is connected to a positive power supply terminal 19, of a conventional direct current power supply that has its other terminal grounded.

The substrate 15 is shown in FIGS. 1 and 3 as a dotted line to indicate that it extends from the terminal 19 of the power supply across the semiconductor chip 40 to every stage of the shift register. This substrate is shorted to the source electrodes of the transistors 16 and 18 by way of a metallic connection that is deposited continuously across the source electrode and the substrate.

In a manner that is known in the art, the transistors 16 and 18 are cross-coupled by way of the source-to-drain paths of another two transistors 20 and 21. The source and drain electrodes, respectively, of the transistor 20 are connected to the drain electrode of transistor 16 and to the gate electrode of the transistor 18. The source and drain electrodes, respectively, of the transistor 21 are connected to the drain electrode of the transistor 18 and to the gate electrode of the transistor 16. Gate electrodes of both transistors 20 and 21 are connected to a clock-drive phase I.

Two additional transistors 22 and 23 are arranged as load devices for the transistors 16 and 18. Source electrodes of the transistors 22 and 23, respectively, are connected to the drain electrodes of the transistors 16 and 18, and their gate and drain electrodes are connected in common to the gate electrodes of the transistors 20 and 21 and to the clock-drive phase I. In FIG. 1 and FIG. 3, a lead 25 connects the clock-drive phase I to the transistors 20, 21, 22, and 23 and is shown partly dotted to indicate that it also extends across the entire semiconductor chip to connect with similar transistors of other shift register stages.

In the input portion of the circuit of FIG. 1, a transistor 30 has its source-to-drain conduction path interposed between the terminal 12 and the gate electrode of the transistor 16. A clock-drive phase II applies control signals to a gate electrode of transistor 30 for controlling conduction there-through. The transistor 30 is made to conduct readily only at times that information is to be shifted into the stage shown in FIG. 1 and thus operates as an input gate which isolates the illustrated stage from changes of input signals except at predetermined times. Another transistor gate, not shown because it is located in the input portion of the next subsequent stage of the shift register, operates in a similar fashion in response to the clock-drive phase II and serves to transfer information signals from the output terminal 14 of the

illustrated stage to the next subsequent stage of the shift register concurrently with the receipt of information through the transistor 30 into the stage of FIG. 1.

In the output portion of the circuit of FIG. 1, a transistor 32 is connected as a third load device with its source electrode connected to the drain electrode of the transistor 18. Drain and gate electrodes of the transistor 32 are connected to the clock-drive phase II, which controls conduction through the transistor 32.

In FIG. 1 and FIG. 3, a lead 35 connects the clock-drive phase II to the transistors 30 and 32 and is shown partly dotted to indicate that the lead 35 also extends across the semiconductor chip to connect with similar transistors of every stage of the shift register. Preferably leads 25 and 35 are fabricated as metallized conductors affixed to the chip.

FIG. 2 shows the timing of the clock-drive phases I and II. These clock-drive phases are substantially out of phase with each other so that phase I is at ground potential when phase II is at a positive potential V_{DD} , and vice versa. For example, phase I ordinarily is at ground potential but rises to the positive potential V_{DD} at the time T_1 and returns to ground immediately after time T_2 . On the other hand, phase II ordinarily is held at the positive potential V_{DD} but falls to ground immediately after time T_1 and returns to the positive potential V_{DD} at the time T_2 . The difference between the potential V_{DD} and ground exceeds the threshold voltages of the devices 16, 18, 20, 21, 22, 23, 30, and 32.

The ground of the clock-drive phases I and II is returned to the grounded terminal of the power supply by way of a lead 37, as shown in FIG. 3.

In the operation of the stage of FIG. 1, an output signal from the preceding stage, not shown, is applied to the input terminal 12 as an input signal and is coupled through the transistor 30 to the gate electrode of transistor 16 when the clock-drive phase II is at ground potential during the interval between times T_1 and T_2 . During that interval, the potential of the input signal from the preceding stage is coupled through the transistor 30 to the gate electrode of the transistor 16 for controlling conduction there-through. The input signal from the preceding stage is either near ground potential or near the positive potential V_{DD} .

As previously mentioned, the clock-drive phases I and II are substantially out of phase with each other so that during the interval between the times T_1 and T_2 , phase I is positive and therefore disables conduction through the transistors 20 and

21. The positive potential of the clock-drive phase I also prevents conduction through the load transistors 22 and 23 during that same interval.

5 If a near ground potential input signal is applied to the terminal 12 during the interval between the times T_1 and T_2 , the transistor 16 is enabled to conduct. After the transistor 16 is enabled to conduct, the
10 clock-drive phase II returns to its positive potential level at the time T_2 and the clock-drive phase I returns to ground. As a result, the input gate transistor 30 is cut off once again, and the transistors 20, 21,
15 22, and 23 are enabled to conduct. Conduction through the transistor 18 increases because the ground potential input signal is stored in its gate-to-source capacitance and the load device 22 now is enabled to
20 conduct current. As a result of the conduction through the transistor 16, the potential on its drain electrode increases substantially to the positive potential V_{DD} of the supply terminal 19 and is coupled
25 through the enabled transistor 20 to the gate electrode of transistor 18.

In response to this positive potential V_{DD} , the transistor 18 is disabled from conducting, and its drain electrode is held
30 at ground by the ground potential of the clock-drive phase I, which is coupled thereto through the enabled transistor 23. In turn, this ground potential on the drain electrode of transistor 18 is coupled
35 through the enabled transistor 21 to the gate electrode of the transistor 16 for latching the latter in its conducting state.

If at the time T_1 the signal on the input terminal 12 were near the positive potential
40 V_{DD} rather than near ground, then the transistor 16 is disabled from conducting during the interval between times T_1 and T_2 . In such a circumstance, the transistor 18 becomes biased to conduct as soon as the
45 clock-drive phase II goes positive at time T_2 and the positive potential V_{DD} of the supply terminal 19 is coupled to its drain electrode. This positive potential is coupled back through the enabled transistor 21 to
50 the gate electrode of the transistor 16 for holding the latter disabled.

The drain electrode of the transistor 18 is directly connected to the output terminal 14 and therethrough to an input terminal
55 of the next subsequent shift register stage, not shown. Whatever potential is produced at the drain electrode of the transistor 18 is transferred to the input terminal of the next subsequent shift register stage when
60 the clock-drive phase II goes to ground, such as immediately after the time T_1 shown in FIG. 2. At such time, the input transistor gate of the next subsequent stage is enabled to couple the potential from the
65 output terminal 14 to a gate electrode of

a transistor corresponding to the transistor 16.

When the clock-drive phase II goes to ground immediately after the time T_1 , the transistor 32 also is enabled to conduct.
70 Because transistor 32 conducts while information is being transferred between register stages, it operates as a load device in place of transistor 23, which is disabled by the clock-drive phase I at the time T_1 .
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Thus, two alternative routes are established between the drain electrode of transistor 18 and ground. One route to ground is through the load transistor 23 to the clock-drive phase I and is active from immediately after the time T_2 until the time
80 T_1 , while the clock-drive phase I is at ground potential. The second route to ground is through the load transistor 32 to the clock-drive phase II, which is at
85 ground potential from immediately after the time T_1 until the time T_2 . Since the two clock-drive phases are substantially out of phase with each other, the drain electrode of the transistor 18 has a return path
90 to ground substantially all of the time. These two alternative return paths to ground require no lead across the entire semiconductor chip other than the previously mentioned pair of leads 25 and 35
95 connecting the clock-drive phases I and II to all of the stages of the shift register.

Whilst in previous shift registers a similar pair of leads for connecting the clock-drive phases I and II to all of the stages extended across the entire semiconductor chip, it was also necessary to provide an additional lead across the entire chip to serve as a separate return path from the stages to ground.
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The present invention eliminates the need for the separate ground return lead by providing alternative paths from the drain electrode of the transistor 18 to the ground potential occurring in the clock-drive phases I and II. Elimination of this additional lead reduces the chip area required by the circuit and may decrease the cost of fabricating the semiconductor chip.
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Referring now to FIG. 4, there is shown an IGFET shift register which operates like the shift register of FIG. 3 in response to the clock-drive phases I and II of FIG. 2 but without any separate direct current
120 power supply connected to the substrate of the semiconductor chip 40. Circuit elements in FIG. 4 having counterparts in FIG. 3 have like references.

The power supply is eliminated from the circuit of FIG. 4 because the clock-drive phases I and II provide not only a ground return path but also to apply the positive potential V_{DD} to the substrate of the semiconductor chip. Once again the clock-
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drive phases I and II are substantially out of phase with each other, as a result of which one or the other of the clock-drive phases is at the high potential V_{DD} all of the time.

- 5 The potential V_{DD} is coupled through a drain diffusion to the substrate in every cell of the shift register.

For instance, refer to FIG. 1 where the clock-drive phase I is shown connected to the drain electrodes of the transistors 22 and 23 and where the clock-drive phase II is shown connected to the drain electrode of the transistor 32. Each of these drain electrodes provides a path for coupling the potential V_{DD} to the substrate of the semiconductor chip 40.

The coupling of the potential V_{DD} to the substrate may be better understood by reference to FIG. 5 wherein the metallic lead 25 is shown in contact with a drain diffusion 42 of the transistor 22. In FIG. 5 circuit elements having counterparts in FIG. 1 are identified by like references.

The drain diffusion 42 and a source diffusion 43 are P-type diffusions in an N-type substrate 44. A metallic gate electrode 46 is affixed to an insulating layer 47 disposed on the surface of the substrate 44 and the diffusions 42 and 43.

30 When the clock-drive phase I of FIG. 1 goes to the positive potential V_{DD} , the pn junction between the drain diffusion 42 and the substrate 44 is forward biased into conduction. As a result, the substrate is raised to a potential that is approximately one diode junction drop below the positive potential V_{DD} . The potential, at which the substrate is held, is coupled to the source electrodes of the transistors 16 and 18 of FIG. 1 by means of the previously mentioned metallic connections between those source electrodes and the semiconductor substrate.

When the clock-drive phase I goes to ground, the pn junction between the diffusion 42 and the substrate 44 is reverse biased and cut off. As a result the ground potential of the clock-drive phase I has no effect on the substrate potential which is then determined by the clock-drive phase II.

The coupling of the potential V_{DD} to the substrate 44 as just described is similar for both clock-drive phases I and II. The phases I and II are both connected to at least one drain electrode in each stage of the shift register. Since the clock-drive phases I and II are out of phase with each other, the substrate 44 of the semiconductor chip 40 is maintained near the potential V_{DD} all of the time.

The potential V_{DD} must be greater than the threshold potential of the IGFET devices plus one pn junction potential drop to ensure that the circuit operates satis-

factorily without a separate direct current power supply.

WHAT WE CLAIM IS:—

1. A semiconductor circuit including a plurality of transistor shift register stages connected in tandem, a first metallised conductor connected in common to all said stages for applying a first clock-drive phase thereto, and a second metallised conductor connected in common to all said stages for applying a second clock-drive phase thereto substantially out of phase with said first clock-drive phase, each of said stages being such and being so connected to said conductors that, in operation, each of said conductors serves to alternately provide its respective clock-drive phase to said stages and a return path from said stages to ground.

2. A circuit as claimed in claim 1 wherein each of said stages includes a pair of insulated gate field effect transistors cross-coupled through a pair of cross-coupling devices, a pair of load devices each coupled to a different one of said pair of transistors, said first conductor being for applying said first clock-drive phase to control conduction through said pair of cross-coupling devices and through said pair of load devices, an input device, and a third load device coupled to one of said pair of transistors, said second conductor being for applying said second clock-drive phase to control conduction through said input device and said third load device.

3. A circuit as claimed in claim 1 wherein each of said stages includes first, second, third, fourth, fifth, sixth, seventh, and eighth transistor devices each having source, gate and drain electrodes, means for connecting the source electrodes of said first and second devices to a reference potential source, means connecting the drain electrode of said first device to the source electrode of said third device, means connecting the drain electrode of said third device to the gate electrode of said second device, means connecting the drain electrode of said second device to the source electrode of said fourth device, means connecting the drain electrode of said fourth device to the gate electrode of said first device, means connecting the source electrode of said fifth device to the drain electrode of said first device, means connecting the source electrode of said sixth device to the drain electrode of said second device, means connected to said first conductor and interconnecting the gate electrodes of said third and fourth devices with the gate and drain electrodes of said fifth and sixth devices, means connecting the drain electrode of said seventh device to the gate

drive phases I and II are substantially out of phase with each other, as a result of which one or the other of the clock-drive phases is at the high potential V_{DD} all of the time.

5 The potential V_{DD} is coupled through a drain diffusion to the substrate in every cell of the shift register.

For instance, refer to FIG. 1 where the clock-drive phase I is shown connected to the drain electrodes of the transistors 22 and 23 and where the clock-drive phase II is shown connected to the drain electrode of the transistor 32. Each of these drain electrodes provides a path for coupling the potential V_{DD} to the substrate of the semiconductor chip 40.

The coupling of the potential V_{DD} to the substrate may be better understood by reference to FIG. 5 wherein the metallic lead 25 is shown in contact with a drain diffusion 42 of the transistor 22. In FIG. 5 circuit elements having counterparts in FIG. 1 are identified by like references.

The drain diffusion 42 and a source diffusion 43 are P-type diffusions in an N-type substrate 44. A metallic gate electrode 46 is affixed to an insulating layer 47 disposed on the surface of the substrate 44 and the diffusions 42 and 43.

30 When the clock-drive phase I of FIG. 1 goes to the positive potential V_{DD} , the pn junction between the drain diffusion 42 and the substrate 44 is forward biased into conduction. As a result, the substrate is raised to a potential that is approximately one diode junction drop below the positive potential V_{DD} . The potential, at which the substrate is held, is coupled to the source electrodes of the transistors 16 and 18 of FIG. 1 by means of the previously mentioned metallic connections between those source electrodes and the semiconductor substrate.

45 When the clock-drive phase I goes to ground, the pn junction between the diffusion 42 and the substrate 44 is reverse biased and cut off. As a result the ground potential of the clock-drive phase I has no effect on the substrate potential which is then determined by the clock-drive phase II.

The coupling of the potential V_{DD} to the substrate 44 as just described is similar for both clock-drive phases I and II. The phases I and II are both connected to at least one drain electrode in each stage of the shift register. Since the clock-drive phases I and II are out of phase with each other, the substrate 44 of the semiconductor chip 40 is maintained near the potential V_{DD} all of the time.

The potential V_{DD} must be greater than the threshold potential of the IGFET devices plus one pn junction potential drop to ensure that the circuit operates satis-

factorily without a separate direct current power supply.

WHAT WE CLAIM IS:—

1. A semiconductor circuit including a plurality of transistor shift register stages connected in tandem, a first metallised conductor connected in common to all said stages for applying a first clock-drive phase thereto, and a second metallised conductor connected in common to all said stages for applying a second clock-drive phase thereto substantially out of phase with said first clock-drive phase, each of said stages being such and being so connected to said conductors that, in operation, each of said conductors serves to alternately provide its respective clock-drive phase to said stages and a return path from said stages to ground.

2. A circuit as claimed in claim 1 wherein each of said stages includes a pair of insulated gate field effect transistors cross-coupled through a pair of cross-coupling devices, a pair of load devices each coupled to a different one of said pair of transistors, said first conductor being for applying said first clock-drive phase to control conduction through said pair of cross-coupling devices and through said pair of load devices, an input device, and a third load device coupled to one of said pair of transistors, said second conductor being for applying said second clock-drive phase to control conduction through said input device and said third load device.

3. A circuit as claimed in claim 1 wherein each of said stages includes first, second, third, fourth, fifth, sixth, seventh, and eighth transistor devices each having source, gate and drain electrodes, means for connecting the source electrodes of said first and second devices to a reference potential source, means connecting the drain electrode of said first device to the source electrode of said third device, means connecting the drain electrode of said third device to the gate electrode of said second device, means connecting the drain electrode of said second device to the source electrode of said fourth device, means connecting the drain electrode of said fourth device to the gate electrode of said first device, means connecting the source electrode of said fifth device to the drain electrode of said first device, means connecting the source electrode of said sixth device to the drain electrode of said second device, means connected to said first conductor and interconnecting the gate electrodes of said third and fourth devices with the gate and drain electrodes of said fifth and sixth devices, means connecting the drain electrode of said seventh device to the gate



- electrode of said first device, means connecting the source electrode of said eighth device to the drain electrode of said second device, and means connected to said second conductor and interconnecting the gate electrode of said seventh device with the gate and drain electrodes of said eighth device.
4. A circuit as claimed in any one of claims 1 to 3 including a first clock-drive phase providing means coupled to said first conductor, and a second clock-drive phase providing means coupled to said second conductor, said second clock-drive phase being substantially out of phase with said first clock-drive phase.
5. A circuit as claimed in any one preceding claim wherein said stages share a common substrate.
6. A circuit as claimed in claim 2 or 3 wherein each said device is an insulated gate field effect transistor device.
7. A semiconductor circuit arranged and adapted to operate substantially as herein described with reference to FIGS. 1 to 3, or with reference to FIGS. 1 to 3 as modified by FIGS. 4 and 5 of the accompanying drawing.
8. A shift register stage substantially as herein described with reference to FIG. 1 of the accompanying drawing.

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