

CLAIMS

1. An apparatus (200) configured for bit packing data having various bit widths in a computer system, the apparatus comprising:

a first plurality of bit locations (202) in the computer system, each bit location of the first plurality of bit locations comprising a register (304) with a predetermined number of bit slots (206) and each bit slot of the predetermined number of bit slots configured to temporarily store a respective bit of a predetermined number of bits of data, the predetermined number of bits corresponding to one of a number of different data bit widths; and

a fixed bit packing network (208) configured to pack the predetermined number of bits from the first plurality of bit locations (202) to a second plurality of bit locations (210) in the computer system, wherein the fixed bit packing network is configured to pack the predetermined number of bits by routing all bits of the predetermined number of bits stored in a same particular bit slot position (320) in the predetermined number of bit slots within each respective bit location of the first plurality of bit locations (202) to bit slots (322) of a register (306) of a particular bit location of the second plurality of bit locations (210) to form bit bundles (328) in respective ones of the second plurality of bit locations (210),

wherein the fixed bit packing network (208) includes fixed point-to-point connections between the bit slots in the first plurality of bit locations (202) and the bit slots in the second plurality of bit locations (210), and is configured to

accommodate each of the number of different data bit widths input to the first plurality of bit locations, and

pack data from the first plurality of bit locations into the second plurality of bit locations.

2. The apparatus (200) of claim 1, further comprising:

the second plurality of bit locations (202) contained within a memory device, wherein the memory device is further configured to store the bit bundles (328).

3. The apparatus (200) of claim 2, wherein the second plurality of bit locations (210) comprises a plurality of memory cells in the memory device.

4. The apparatus (200) of claim 3, wherein the number of bits in a bit bundle (328) corresponds to a memory data word size of the memory device.

5. The apparatus (200) of claim 1, wherein the fixed bit packing network (208) comprises a portion of one of a computation datapath network or a memory datapath.
6. The apparatus (200) of claim 1, wherein the bits in the first plurality of bit locations (202) are generated by a single-instruction, multiple data, SIMD, unit having a number of lanes.
7. The apparatus (200) of claim 6, wherein each bit bundle (328) has a size that is a multiple of the number of lanes of the SIMD unit.
8. The apparatus (200) of claim 1, wherein the apparatus is further operable for an unpacking operation wherein bit bundles (328) in the plurality of second bit locations (210) are unpacked to the plurality of first bit locations by reverse operation of the fixed bit packing network (208).
9. A method (700) of operating a computational circuitry, comprising:
 - storing (702) one or more bits in at least one of a first plurality of bit locations (202), each bit location of the first plurality of bit locations comprising a register (304) with a predetermined number of bit slots (206) and each bit slot of the predetermined number of bit slots configured to temporarily store a respective bit of a predetermined number of bits of data, the predetermined number of bits corresponding to one of a number of different data bit widths; and
 - packing (704) bits to a second plurality of bit locations (210), the packing utilizing a fixed bit packing network (208) configured to pack the predetermined number of bits from the first plurality of bit locations (202) to the second plurality of bit locations (210), wherein the fixed bit packing network (208) is configured to pack the predetermined number of bits by routing all bits of the predetermined number of bits stored in a same particular bit slot position (320) in the predetermined number of bit slots within each respective bit location of the first plurality of bit locations (202) to bit slots of a particular register (306) of a bit location of the second plurality of bit locations (210) to form bit bundles (328) in respective ones of the second plurality of bit locations (210),
 - wherein the fixed bit packing network (208) includes fixed point-to-point connections between the bit slots in the first plurality of bit locations (202) and the bit slots in the second plurality of bit locations (210), and is configured to

accommodate each of the number of different data bit widths input to the first plurality of bit locations, and

pack data from the first plurality of bit locations into the second plurality of bit locations.

10. The method (700) of claim 9, further comprising:
storing the bit bundles (328) in a memory device, wherein the second plurality of bit locations are contained within the memory device.
11. The method (700) of claim 10, wherein the number of bits in a bit bundle corresponds to a memory data word size of the memory device.
12. The method (700) of claim 9, wherein the fixed bit packing network (208) comprises a portion of one of a computation datapath network or a memory datapath.
13. The method (700) of claim 9, wherein the predetermined number of bits of the data in the first plurality of bit locations are received from a SIMD unit having a number of lanes.
14. The method (700) of claim 13, wherein each bit bundle has a size that is a multiple of the number of lanes of the SIMD unit.
15. The method (700) of claim 9, further comprising executing an unpacking operation wherein bit bundles in the plurality of second bit locations are unpacked to the plurality of first bit locations by reverse operation of the fixed bit packing network.