

Method for producing multicrystalline silicon

The invention relates to a process for producing multicrystalline silicon.

5 Multicrystalline silicon is used to manufacture solar cells for the photovoltaics sector. In the case of multicrystalline silicon the crystal has different crystal orientations. By contrast, in the case of monocrystalline silicon the entire crystal has the same crystal orientation.

10 The feedstock for producing single-crystal or multicrystalline silicon is polycrystalline silicon.

The polycrystalline silicon is typically produced by the Siemens process. This comprises heating thin filament rods (slim rods) of silicon by direct passage of current
15 in a bell-shaped reactor (Siemens reactor) and introducing a reaction gas comprising a silicon-containing component and hydrogen.

An alternative to this is the production of granular polycrystalline silicon in a fluidized/moving bed reactor. This is achieved by fluidizing silicon particles using a
20 gas current in a fluidized bed, this bed being heated to high temperatures via a heating apparatus. Addition of a silicon-containing reaction gas brings about a deposition reaction on the hot particle surface. Elemental silicon is thus deposited on the silicon particles and the individual particles increase in diameter.

25 The silicon-containing component of the reaction gas is generally monosilane or a halosilane of general composition $\text{SiH}_n\text{X}_{4-n}$ ($n=0, 1, 2, 3$; $\text{X} = \text{Cl}, \text{Br}, \text{I}$). Said component is preferably a chlorosilane or a chlorosilane mixture, particularly preferably trichlorosilane. A mixture of SiH_4 or SiHCl_3 (trichlorosilane, TCS) with hydrogen is predominantly used.

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For applications in the photovoltaics sector this polycrystalline silicon needs to be crystallized in a further step.

Pulling and casting processes are known for the production of single-crystal or multi-crystalline silicon.

Single-crystal silicon may be produced by crucible pulling (Czochralski or CZ process)
5 or by zone melting (float zone or FZ process).

In addition to CZ silicon, directional solidification of silicon is the most common method of crystallizing silicon for the photovoltaics sector.

10 The solidification of the silicon is typically carried out in silicon nitride coated quartz crucibles. The silicon nitride prevents adhesion of the silicon to the crucible. Adhesion can result in cracks in the silicon material and a loss of the crystallized silicon.

Once the crucible is filled with silicon the silicon is heated until it melts. Once
15 completely melted the silicon is solidified from bottom to top. After solidification the crystal is cooled slowly in a controlled fashion. This is intended to avoid stresses in the material. Once cooled the crystal may be deinstalled and subjected to further processing to afford wafers. This typically comprises initially cutting the crystal blocks into smaller blocks/bricks (crude ingots and finished ingots) using an internal diameter
20 saw. The smaller bricks are subsequently cut into wafers using a wire saw.

However, multicrystalline silicon is as yet inferior to the monocrystalline material in terms of cell efficiency on account of crystal defects (grain boundaries, dislocations and impurities) caused by the process.

25 Efforts are therefore ongoing to reduce the electrically recombination-active area fraction of the wafer surface through optimized production processes and technologies in order ultimately to enhance solar cell efficiency.

30 The starting point here is the microstructure at the beginning of the solidification process in immediate proximity to the crucible bottom. The most important microstructure parameters here are grain size, grain size distribution, grain shape,

crystal orientation and the grain boundary relationships between the individual crystallites.

The prior art discloses technical options for generating different initial microstructures
5 at the beginning of the solidification process.

One option that has been pursued is influencing the initial crystal microstructure formation at the crucible bottom by moderating axial heat transfer.

10 US 2011/239933 A1 discloses a process for producing silicon blocks comprising the steps of:

- providing a vessel for receiving a silicon melt, wherein the vessel has a bottom and an inner surface,

- providing a silicon melt in the vessel,

- 15 – removing heat through the bottom of the vessel to cool the silicon melt,

- wherein the heat is removed in such a way that an inhomogeneous temperature distribution is at least temporarily established on the inner surface of the vessel in the region of the bottom. The temperature distribution preferably comprises a temperature range of at least 0.1 K, more particularly at least 1 K, more particularly at least 5 K

20 and not more than 50 K, more particularly not more than 10 K. Temperature differences of from 0.1 to 50 Kelvin in the region of the bottom can influence nucleation and thus bulk crystallization.

Attempts have also been made to influence the initial crystal microstructure by initially
25 charging the crucible with a nucleation promotion layer (for example fine-grained silicon) on which the silicon nucleates.

DE 10 2011 087 759 A1 and SG 190547 A1 claim a process for producing silicon ingots comprising the steps of:

- 30 – providing a container for receiving a silicon melt,

- arranging a fine-grained silicon layer in the container,

- arranging a silicon melt in the container in contact with the fine-grained silicon layer,

- directionally solidifying the silicon melt starting from the fine-grained silicon layer.

The fine-grained silicon layer may be generated by contacting liquid silicon with a substrate which is at a temperature below the melting point of silicon. The substrate is preferably composed of a fine-grained crude material such as silicon, silicon carbide, silicon nitride or graphite having an average grain size in the range from 0.1 mm to 3 mm which is initially charged directly onto the bottom of the container and in particular has a thickness in the range from 1 cm to 5 cm. Also claimed is that the temperature in the fine-grained layer is below the melting point of silicon, that the melting procedure and solidification procedure may be carried out either in the same crucible or in two different crucibles and that the crystallized silicon block is at least 50 cm in height. There is said to be a reduction in the number of grains, from the bottom to the top, of at least 20%, more particularly at least 30%. It is reported that the electrically recombination-active defect fraction remains constant above a certain block height.

US 2013/136918 A1 discloses a process for producing a crystalline silicon block comprising the steps of:

(a) initially charging a nucleation promotion layer onto the bottom of a mold, the mold itself defining a vertical direction;

(b) providing a silicon source on the nucleation promotion layer in the mold;

(c) heating the mold until the silicon source is completely melted to afford a silicon melt;

(d) continuously controlling at least one thermal control parameter in respect of the silicon melt such that a plurality of silicon grains can nucleate out of the silicon melt arranged on the nucleation promotion layer and grow in the vertical direction; and

(e) continuously controlling the at least one thermal control parameter such that the silicon grains can continuously grow in the vertical direction until the entirety of the silicon melt has solidified and the crystalline silicon block is obtained.

Also disclosed is a crystalline silicon block having a lower part and defining a vertical direction, characterized in that the crystalline silicon block comprises a plurality of silicon grains grown in the vertical direction and a nucleation promotion layer on the lower part, wherein the silicon grains that are adjacent to the nucleation promotion layer have an average grain size of less than about 10 mm. Also claimed is that the rate of increase of defect density in the vertical direction of the block is in the range of from 0.01 to 10%/mm. It is reported that the nucleation promotion layer consists of

irregular particles of less than 50 mm in size and is composed of silicon and silicon carbide particles. The nucleation promotion layer may further consist of a plate having a melting point above that of silicon and a roughness of 300 to 1000 μm . It is reported that the crystal material (block and wafer) predominantly exhibits crystal orientations of the silicon grains between (001) and (111) and that the fraction of the silicon grains having the predominant crystal orientations is more than 50 vol%.

The use of extrinsic nucleating agents is also prior art.

DE 10 2011 002 599 A1 and US 2012/175622 A1 disclose a process for producing a silicon ingot comprising the steps of:

- providing a container for receiving a silicon melt,
- providing a temperature control device to control the temperature of the silicon melt in the container,

- arranging in the container crude material comprising silicon and at least one nucleating agent to promote heterogeneous nucleation in the silicon melt, and
- controlling the temperature in the container in such a way that during a particular stage of the process the crude material is present in the container as a silicon melt which in a subsequent stage of the process is directionally solidified,

- wherein the nucleating agent comprises nanoparticles.

The intention here is to influence the initial crystal microstructure through the use of at least one additional nucleating agent for heterogeneous nucleation in the silicon melt.

The additional nucleating agents are charged in proximity to the crucible bottom, preferably in a region where the nucleating agent concentration is higher than the

saturation concentration of the elements concerned. These nucleating agents should have a surface area of at least $2 \text{ m}^2/\text{g}$ and the particles should optionally be getter centers for metal atoms and be composed of at least a fraction of silicon and at least one element selected from carbon, oxygen and nitrogen. 90% of these nucleating particles should have a particle size of not more than $1 \mu\text{m}$. Likewise described is a

silicon ingot having a longitudinal axis, a first end in the direction of the longitudinal axis, a second end in the direction of the longitudinal axis, a length (L) in the direction of the longitudinal axis, a multicrystalline structure and a grain density in the region of the first end of at least 400 dm^{-2} , more particularly at least 600 dm^{-2} , more particularly

at least 800 dm^{-2} . Also disclosed is a silicon wafer of multicrystalline silicon having a wafer surface and having particles, wherein at least 90% of the particles have a diameter of not more than $1 \text{ }\mu\text{m}$ and the particles comprise a fraction of a compound of silicon and at least one element selected from the group of carbon, oxygen and nitrogen. Finally these documents also disclose silicon wafers having an area fraction of at least 80 and up to 95% and a dislocation density of less than 10^5 cm^{-2} .

Influencing initial crystal microstructure formation through the use of special crucible coatings is also prior art.

DE 10 2010 000 687 B4 and SG 172588 A1 disclose a process for producing silicon blocks comprising the steps of providing a crucible for receiving a silicon melt having a bottom and a plurality of side walls connected to the bottom; applying nuclei at least to the inner surface of the bottom of the crucible, wherein the nuclei have a melting point higher than the melting point of silicon; filling the crucible with the silicon melt; solidifying the silicon melt starting at the nuclei and removing the solidified silicon from the crucible.

The process results in an initially fine-grained crystal microstructure. The necessary nuclei density is in the range from 0.001 to $100/\text{cm}^2$ and the nuclei size is in the range from 0.01 to $50\,000 \text{ }\mu\text{m}$. One or more compounds of the elements of main group III, IV or V, but in particular Al_2O_3 , SiC , SiO , SiO_2 , Si_3N_4 , BN , BP , AlAs , AlN or BeO , are cited as materials to be employed.

DE 10 2011 003 578 A1 and US 2011/203517 A1 describe a process for producing silicon blocks comprising the steps of:

- providing a vessel for receiving a silicon melt which comprises on at least part of the inner surface of at least one vessel wall a nucleation-inhibiting surface and at least one nucleation site on the inner surface provided with the nucleation-inhibiting surface,
- arranging a silicon melt in the vessel by pouring in liquid silicon or by melting solid silicon,
- cooling the at least one vessel wall with the nucleation-inhibiting surface to crystallize the silicon melt.

Silicon carbide, graphite, silicon nitride, silicon dioxide, silicon oxynitride and boron nitride are cited as materials to be employed.

US 2014/0186631 A1 describes a nucleating material which is constructed from a nucleation-promoting layer and a diffusion-inhibiting layer and may be made of a very wide variety of barium compounds, oxides, carbides, nitrides etc.

Common to these different processes is the intention to generate the smallest possible electrically recombination-active area fraction on the multicrystalline silicon wafers, particularly for the wafers proximal to the crucible bottom, i.e. at the start of solidification.

However, the processes described in the prior art are technically complex on account of the costly heat transport setup and the relatively lengthy process times, for example during nucleation on crude silicon material. There is also the danger of additional contamination of the silicon when extraneous nucleation promotion layers or extrinsic nucleating agents are initially charged.

The object to be achieved by the invention arose from the problems described. In particular the invention had for its object the provision of multicrystalline silicon having a relatively low electrically recombination-active area fraction and thus a relatively high solar cell efficiency.

The object of the invention is achieved by a process for producing multicrystalline silicon comprising the steps of:

- providing a crucible for receiving a silicon melt which comprises a bottom and an inner surface, wherein at least the bottom of the crucible has a coating comprising one or more compounds selected from the group consisting of Si_3N_4 , oxidized Si_3N_4 and SiO_2 ,
- arranging a silicon layer in the crucible in contact with the coating of the bottom of the crucible,
- arranging polycrystalline silicon in the crucible in contact with the silicon layer,

- heating the crucible until the polycrystalline silicon and the silicon layer are completely melted to afford a silicon melt;
- directionally solidifying the silicon melt to form a multicrystalline silicon block, wherein the silicon layer releases a reducing agent during the heating of the crucible and/or during the melting of the silicon layer.

The silicon layer comprises a crude silicon material conditioned such that it releases a reducing agent. This alters the wetting behavior of the crucible coating toward the silicon melt generated from the polycrystalline silicon. This wetting behavior varies with the oxygen content of the crucible coating. Chemical attack mediated by the reducing agent reduces the oxygen content in the crucible coating thus influencing the wetting properties. This makes it possible to reduce the initial nucleation energy through the change in wetting behavior - from non-wetting to wetting - and thus to generate an initial small-grained microstructure which completely covers the crucible bottom or is localized.

The silicon layer preferably comprises polycrystalline silicon produced by the above-described Siemens process and subsequently comminuted into chunks. A further embodiment concerns granular polycrystalline silicon produced in a fluidized/moving bed reactor. Both the Siemens process and the fluidized bed process employ monosilane or a halosilane as the silicon-containing component of the reaction gas, for example trichlorosilane in admixture with hydrogen. This traps hydrogen and halogens in, for example, the granular silicon particles.

It is preferable when the silicon layer comprises polycrystalline silicon having a hydrogen content of from 0.5 to 40 ppmw, preferably 10 to 40 ppmw.

The hydrogen content of silicon may be measured in a manner analogous to ASTM E 1447 by the "Inert Gas Fusion Thermal Conductivity/Infrared Detection Method".

It is preferable when the silicon layer comprises polycrystalline silicon having a halogen content of from 3 to 90 ppmw, preferably 5 to 40 ppmw.

It is preferable when the silicon layer comprises polycrystalline silicon having a chlorine content of 3 to 90 ppmw, preferably 5 to 40 ppmw.

Contents of halogens/chloride may be determined as per SEMI PV 10, "Test Method
5 for Instrumental Neutron Activation Analysis (INAA) of Silicon" or else by X-ray fluorescence analysis (XRF).

In one embodiment the silicon layer comprises granular polycrystalline silicon having a grain size of from 50 to 4000 μm . Particular preference is given to a grain size of
10 from 50 to 400 μm . The determination of particle size may be carried out using an optical particle sizer. This is done using dynamic image analysis as per ISO/DIS 13322-2.

US 5077028 A, US 2013/295385 A1 and US 2013/280533 A1 disclose how granular
15 polycrystalline silicon having defined hydrogen and/or halogen contents may be produced. It has hitherto been desirable to achieve the lowest possible halogen content to avoid splattering effects or the formation of corrosive gases during crystal pulling.

20 In one embodiment the silicon layer in the crucible is arranged such that it covers at least 30% of the area of the bottom of the crucible. It is preferable when at least 50% of the area of the crucible bottom is covered. In one embodiment the silicon layer covers the entire area of the crucible bottom.

25 The silicon layer preferably has a height of from 50 μm to 100 cm, particularly preferably 50 μm to 10 cm and very particularly preferably 50 μm to 1 cm.

The polycrystalline silicon arranged in the crucible and in contact with the silicon layer which releases a reducing agent may be in the form of chunks (Siemens process) or
30 in the form of granular polycrystalline silicon.

In one embodiment the crucible coating is at least 200 μm , preferably 300-500 μm thick, and the chemical attack mediated by the reducing agent released by the silicon

layer takes place only in the upper part of the crucible coating (50-150 μm thickness). The wetting behavior is altered only in the upper part. Below the chemically attacked upper part of the coating there remains a non-wetting coating which prevents complete penetration of the silicon melt to the crucible bottom.

- 5 It is preferable when the silicon layer is not in contact with the inner surface of the crucible. The distance to the inner surface of the crucible should be at least 1 mm. In one embodiment the distance is at least 1 cm. This prevents the silicon from adhering to the side walls (avoids sticking).
- 10 The directional solidification of the silicon melt preferably forms a multicrystalline silicon block or brick (crude ingot and finished ingot), referred to hereinbelow as a silicon ingot, having an average grain size of less than 12.5 mm^2 , particularly preferably of less than 5 mm^2 and very particularly preferably of less than 2.5 mm^2 in the bottom region of the multicrystalline silicon block/the multicrystalline silicon ingot.
- 15 In the context of the invention the bottom region extends from the bottom of the silicon block/the bottom of the silicon ingot to a height in the block/the ingot of 5 cm (the region 0-5 cm from the bottom).
- 20 The average grain size may be determined using, for example, the GEMINI identification and tracking system from Intego which permits analysis of the crystal structure.

- It is preferable when the multicrystalline silicon block, the multicrystalline silicon ingot and a multicrystalline silicon wafer manufactured therefrom have a maximum average grain size - measured on an area of 156 x 156 mm^2 - of 12.5 mm^2 , particularly preferably 10 mm^2 and very particularly preferably 7 mm^2 .
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- It is preferable when the multicrystalline silicon block, the multicrystalline silicon ingot and a multicrystalline silicon wafer manufactured therefrom have a homogenous grain orientation area distribution. In particular, individual grain orientations should not have an area fraction, measured on an area of 156 x 156 mm^2 of block, ingot or wafer, of more than 50%, particularly preferably more than 25%. Individual grain orientations
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should have an area fraction of less than 25%, particularly preferably of less than 10% and particularly preferably of less than 5%.

5 The multicrystalline silicon block, multicrystalline silicon ingot and multicrystalline silicon wafer manufactured therefrom should have a microstructure with a coefficient of variation of less than 3.

Wafers proximal to the block bottom preferably have an electrically recombination-active area fraction of 0.2-2.5%. Multicrystalline silicon wafers having the lowest
10 electrically recombination-active area fraction from the block top, i.e. toward the end of solidification, preferably have an average grain size of 6 - 11 mm².

The crucible is preferably a quartz crucible having a coating comprising Si₃N₄.

15 The initially charged silicon layer comprises silicon which releases an agent that chemically attacks oxide-containing surfaces.

The initial charging of this silicon layer directly onto the Si₃N₄ coating of the crucible bottom makes it possible to influence the wetting behavior of the crucible coating
20 through release of the agent from the crude material, namely through a chemical reduction of the oxidized crucible coating. The altered oxidation level of the Si₃N₄-based crucible coating also alters the wetting behavior from non-wetting to wetting, in particular at the crucible bottom. An alteration in the wetting behavior also reduces the nucleation energy. Consequently, a small-grained initial grain microstructure can form
25 directly on the now wetting crucible coating.

The advantage of the process according to the invention is that the entire silicon charge (silicon nucleation layer and polycrystalline silicon arranged thereupon) may be melted inside the crucible, that the process is thus less time-consuming and that it
30 is then possible to effect small-grained nucleation on the wetting crucible coating.

The extent of the poor-quality bottom region, formed as a result of solid-state diffusion out of the crucible and the coating, is also reduced.

The initial nucleation during directional solidification of multicrystalline silicon may be controlled by initial charging of a particular crude silicon material in the form of the silicon layer.

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Spatially varying the addition moreover makes it possible to define the spatial structure of the wetting behavior. The initial charge may not only be effected over the entire area of the crucible bottom but may also be localized or comprise local variations.

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Examples

The invention shall be elucidated hereinbelow with reference to examples and figures.

15 The crucible may be made of SiO_2 , Si_3N_4 or carbon.

The coating may be constructed from Si_3N_4 particles which in turn have an oxidized surface. It is also possible to combine different crucible coatings: one crucible coating may retard or completely prevent the chemical attack induced by the silicon layer

20 while a second crucible coating may favor the chemical attack.

The silicon layer which is in direct contact with the oxidized Si_3N_4 -based crucible coating may be arranged in the crucible in different ways: it may be initially charged onto the crucible bottom either over the entire area or in localized fashion. As

25 previously mentioned direct contact of the silicon layer that releases a suitable reducing agent with the crucible side walls should be avoided to prevent wetting/infiltration of the crucible coating on the side walls.

The features cited in connection with the abovedescribed embodiments of the process according to the invention may be correspondingly applied to the apparatus according to the invention. Conversely, the features cited in connection with the abovedescribed embodiments of the apparatus according to the invention may be correspondingly applied to the process according to the invention. These and other features of the

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embodiments according to the invention are elucidated in the description of the figures and in the claims. The individual features may be realized either separately or in combination as embodiments of the invention. Said features may further describe advantageous implementations eligible for protection in their own right.

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Brief description of the figures

Fig. 1 shows a cross-section of a coated crucible including the silicon layer and the polycrystalline silicon.

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Fig. 2 shows a cross-section of a coated crucible including the silicon layer and the polycrystalline silicon.

Fig. 3 shows a plan view of a coated crucible including the silicon layer and the polycrystalline silicon.

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Fig. 4 shows a cross-section of a coated crucible including the silicon layer and the polycrystalline silicon.

Fig. 5 shows a cross-section of a crucible coated with two different materials including the silicon layer and the polycrystalline silicon.

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Fig. 6 shows the defect fraction and the average grain size over the height of the crystal block for the example and the comparative example.

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List of reference numerals employed

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|---|---|
| 1 | silicon layer for nucleation |
| 2 | polycrystalline silicon (chunk or granular) |
| 3 | crucible |
| 4 | crucible coating |

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Fig. 1 shows a cross-sectional sketch of a crucible **3** consisting of side walls and a crucible bottom. The sketch shows, from the outside inward, the crucible **3**, the crucible coating **4** and the region filled with the crude silicon material that releases the reducing agent, namely silicon layer **1**, and the region filled with “normal” crude silicon material, namely with polycrystalline silicon **2**. Here, the silicon layer **1** is initially charged onto the entire area of the crucible bottom.

Figs. 2 and 3 show cross-sectional sketches of a crucible **3** consisting of side walls and a crucible bottom. Here, the silicon layer **1** is in each case initially charged onto the area of the crucible bottom in localized fashion.

Fig. 4 shows a cross-sectional sketch of a crucible **3** consisting of side walls and a crucible bottom. Here, the silicon layer **1** is initially charged such that the silicon layer **1** does not come into direct contact with the side walls of the crucible **3**.

Fig. 5 shows a cross-sectional sketch of a crucible **3** consisting of side walls and a crucible bottom. The sketch shows, from the outside inward, the crucible **3**, the crucible coatings **41** and **42** and also the region filled with silicon layer **1** and the region filled with polycrystalline silicon **2**. The crucible coating **41** has the effect that the chemical attack induced by silicon layer **1** is retarded or completely prevented. The crucible coating **42** has the effect that the chemical attack induced by silicon layer **1** is favored.

Example (process A)

The inventive **process A** comprises initially charging granular polycrystalline silicon deposited in a fluidized bed using trichlorosilane and having a grain size of 0 to 4000 µm and a chlorine content of more than 35 ppmw.

Comparative example (process B)

The standard **process B** comprises initially charging chunked polycrystalline silicon produced by the Siemens process and having a grain size of 0 - 15 mm and a chlorine content of less than 1 ppmw onto the crucible bottom.

- 5 **Fig. 6** shows a comparison of the defect fraction and the average grain size over the height of the block for the initial charging onto the crucible bottom of a silicon layer **1** which releases a suitable reducing agent (**process A**) compared to the initial charging onto the crucible bottom of polycrystalline silicon **2** which does not comprise a suitable reducing agent (**process B**).

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It is apparent that both the defect fraction and the average grain size are lower over the entire height of the block in **process A** than in **process B**.

- 15 The description hereinabove of illustrative embodiments is to be understood as being exemplary. The disclosure made thereby enables a person skilled in the art to understand the present invention and the advantages associated therewith and also encompasses alterations and modifications to the described structures and processes obvious to a person skilled in the art. All such alterations and modifications and also equivalents shall therefore be covered by the scope of protection of the claims.

Claims

1. A process for producing multicrystalline silicon comprising the steps of:
 - providing a crucible for receiving a silicon melt which comprises a bottom and
5 an inner surface, wherein at least the bottom of the crucible has a coating comprising one or more compounds selected from the group consisting of Si_3N_4 , oxidized Si_3N_4 and SiO_2 ,
 - arranging a silicon layer in the crucible in contact with the coating of the bottom of the crucible,
 - 10 - arranging polycrystalline silicon in the crucible in contact with the silicon layer,
 - heating the crucible until the polycrystalline silicon and the silicon layer are completely melted to afford a silicon melt;
 - directionally solidifying the silicon melt to form a multicrystalline silicon block, wherein the silicon layer releases a reducing agent during the heating of the
15 crucible and/or during the melting of the silicon layer.
2. The process as claimed in claim 1, wherein the silicon layer comprises polycrystalline silicon having a hydrogen content of from 0.5 to 40 ppmw, preferably 10 to 40 ppmw.
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3. The process as claimed in claim 1, wherein the silicon layer comprises polycrystalline silicon having a halogen content of from 3 to 90 ppmw, preferably 5 to 40 ppmw.
- 25 4. The process as claimed in claim 3, wherein the halogen is chlorine.
5. The process as claimed in any of claims 1 to 4, wherein the multicrystalline silicon block has an electrically recombination-active area fraction of less than 3%.
- 30 6. The process as claimed in any of claims 1 to 5, wherein the initially charged silicon layer comprises granular polycrystalline silicon having a grain size of from 50 to 4000 μm , preferably having a grain size of from 50 to 400 μm .

7. The process as claimed in any of claims 1 to 6, wherein the silicon layer in the crucible is arranged such that it covers at least 30% and preferably at least 50% of the area of the bottom of the crucible.

5 8. The process as claimed in any of claims 1 to 6, wherein the silicon layer has a height of from 50 μm to 100 cm, preferably 50 μm to 10 cm and particularly preferably 50 μm to 1 cm.

9. The process as claimed in any of claims 1 to 8, wherein the silicon layer is not in
10 contact with the inner surface of the crucible.

10. The process as claimed in any of claims 1 to 9, wherein the distance between the silicon layer and the inner surface of the crucible is at least 1 mm, preferably at least 1 cm.

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11. The process as claimed in any of claims 1 to 10, wherein the multicrystalline silicon block has an average grain size of less than 12.5 mm^2 , preferably of less than 5 mm^2 and particularly preferably of less than 2.5 mm^2 in the bottom region of the multicrystalline silicon block, wherein the bottom region extends from the
20 bottom of the silicon block to a height in the silicon block of 5 cm (the region 0-5 cm from the bottom).

12. The process as claimed in any of claims 1 to 11, wherein the multicrystalline silicon block has a maximum average grain size measured on an area of 156 x
25 156 mm^2 of 12.5 mm^2 , preferably 10 mm^2 and particularly preferably 7 mm^2 .

13. The process as claimed in any of claims 1 to 12, wherein individual grain orientations of the multicrystalline silicon block have an area fraction of less than 25%, preferably an area fraction of less than 10% and particularly preferably an
30 area fraction of less than 5%.

14. The process as claimed in any of claims 1 to 12, wherein the multicrystalline silicon block has a microstructure with a coefficient of variation of less than 3.

15. The process as claimed in any of claims 1 to 14, wherein the multicrystalline silicon block is sawn into multicrystalline silicon ingots in a further step.

5 16. The process as claimed in claim 15, wherein multicrystalline silicon ingots are sawn into multicrystalline silicon wafers in a further step.

10 17. A multicrystalline silicon block produced by a process as claimed in any of claims 1 to 14, wherein individual grain orientations have an area fraction of less than 25%, preferably an area fraction of less than 10% and particularly preferably an area fraction of less than 5%.

15 18. The multicrystalline silicon block as claimed in claim 17, wherein said block has a maximum average grain size measured on an area of 156 x 156 mm² of 12.5 mm², preferably 10 mm² and particularly preferably 7 mm².

19. The multicrystalline silicon block as claimed in either of claims 17 and 18, wherein said block has a microstructure with a coefficient of variation of less than 3.

20 20. The multicrystalline silicon block as claimed in any of claims 17 to 19, wherein said block has an average grain size of less than 12.5 mm², preferably of less than 5 mm² and particularly preferably of less than 2.5 mm² in the bottom region of the multicrystalline silicon block, wherein the bottom region extends from the bottom of the silicon block to a height in the silicon block of 5 cm (the region 0-5 cm from the bottom).

25 21. A multicrystalline silicon ingot produced by a process as claimed in claim 15, wherein individual grain orientations have an area fraction of less than 25%, preferably an area fraction of less than 10% and particularly preferably an area fraction of less than 5%.

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22. The multicrystalline silicon ingot as claimed in claim 21, wherein said ingot has a maximum average grain size measured on an area of $156 \times 156 \text{ mm}^2$ of 12.5 mm^2 , preferably 10 mm^2 and particularly preferably 7 mm^2 .

5 23. The multicrystalline silicon ingot as claimed in either of claims 21 and 22, wherein said ingot has a microstructure with a coefficient of variation of less than 3.

24. The multicrystalline silicon ingot as claimed in any of claims 21 to 23, wherein said ingot has an average grain size of less than 12.5 mm^2 , preferably of less than 5 mm^2 and particularly preferably of less than 2.5 mm^2 in the bottom region of the multicrystalline silicon ingot, wherein the bottom region extends from the bottom of the silicon ingot to a height in the silicon ingot of 5 cm (the region 0-5 cm from the bottom).

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15 25. A multicrystalline silicon wafer produced by a process as claimed in claim 16, wherein individual grain orientations have an area fraction of less than 25%, preferably an area fraction of less than 10% and particularly preferably an area fraction of less than 5%.

20 26. The multicrystalline silicon wafer as claimed in claim 25, wherein said wafer has a maximum average grain size measured on an area of $156 \times 156 \text{ mm}^2$ of 12.5 mm^2 , preferably 10 mm^2 and particularly preferably 7 mm^2 .

25 27. The multicrystalline silicon wafer as claimed in either of claims 25 and 26, wherein said wafer has a microstructure with a coefficient of variation of less than 3.

28. The multicrystalline silicon wafer as claimed in any of claims 25 to 27, wherein said wafer originates from the bottom region of a multicrystalline silicon block or a multicrystalline silicon ingot, wherein the bottom region extends from the bottom of the silicon block or the silicon ingot to a height in the silicon block or the silicon ingot of 5 cm (the region 0-5 cm from the bottom), wherein said wafer has an average grain size of less than 12.5 mm^2 , preferably of less than 5 mm^2 and particularly preferably of less than 2.5 mm^2 .

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