

## **DESCRIPTION**

### **TITLE OF THE INVENTION: SEMICONDUCTOR DEVICE MANUFACTURING METHOD AND SEMICONDUCTOR DEVICE MANUFACTURING SYSTEM**

#### **TECHNICAL FIELD**

[0001] The various aspects and embodiments described herein pertain generally to a semiconductor device manufacturing method and a semiconductor device manufacturing system.

#### **BACKGROUND**

[0002] Patent Document 1 discloses a manufacturing method of a NAND flash memory including a three-dimensional memory cell array in which a plurality of memory cells is three-dimensionally arranged, and a CMOS circuit that controls the memory cell array. The manufacturing method includes bonding a first substrate on which a semiconductor element including the CMOS and the memory cell array has been formed to a second substrate with a separable layer interposed therebetween, and separating the first substrate at the separable layer.

[0003] Patent Document 2 discloses a manufacturing method of a semiconductor device by bonding a semiconductor substrate having memory cells and a semiconductor substrate having a CMOS. The manufacturing method includes filling an insulating film into a non-bonded region at an outer peripheral portion of a bonding substrate, followed by back-grinding.

## **PRIOR ART DOCUMENT**

[0004] Patent Document 1: Japanese Patent Laid-open Publication No. 2021-44408

Patent Document 2: Japanese Patent Laid-open Publication No. 2021-48303

## **DISCLOSURE OF THE INVENTION**

### **PROBLEMS TO BE SOLVED BY THE INVENTION**

[0005] The present disclosure provides a technique enabling appropriate separation of a first substrate and a second substrate in a combined substrate in which the first substrate and the second substrate are bonded to each other.

### **MEANS FOR SOLVING THE PROBLEMS**

[0006] In one exemplary embodiment, a semiconductor device manufacturing method includes: performing, in a non-bonded region of a combined substrate which includes a first substrate having a laser absorption layer and a first bonding layer and a second substrate having a second bonding layer and in which the first bonding layer and the second bonding layer are bonded to each other, bevel fill by injecting a filler up to a predetermined second outer peripheral position which is determined based on a first outer peripheral position in the first bonding layer; radiating laser to the laser absorption layer; and separating the first substrate from the second substrate in the combined substrate.

### **EFFECTS OF THE INVENTION**

[0007] According to the present disclosure, it is possible to appropriately separate the first substrate and the second substrate in the combined substrate in which the first substrate and the second substrate are bonded to each other.

## **BRIEF DESCRIPTION OF THE DRAWINGS**

[0008] **FIG. 1** is a flowchart illustrating main processes of a wafer processing.

**FIG. 2** is an explanatory diagram illustrating the main processes of the wafer processing.

**FIG. 3A** to **FIG. 3C** are explanatory diagrams illustrating an operation where a first wafer and a second wafer are bonded to each other.

**FIG. 4** is an explanatory diagram illustrating an example of bevel fill at a non-bonded region.

**FIG. 5** is an explanatory diagram illustrating another example of the bevel fill at the non-bonded region.

**FIG. 6** is an explanatory diagram illustrating that laser light is radiated to a laser absorption layer.

**FIG. 7A** and **FIG. 7B** are explanatory diagrams illustrating that the first wafer and the second wafer are separated from each other.

**FIG. 8** is an explanatory diagram illustrating main processes of preparing the first wafer according to an exemplary embodiment.

**FIG. 9** is a flowchart illustrating the main processes of preparing the first wafer according to an exemplary embodiment.

**FIG. 10A** to **FIG. 10C** are explanatory diagrams illustrating some of the processes for preparing the first wafer according to the exemplary embodiment.

**FIG. 11** is a flowchart illustrating the main processes of preparing the first wafer according to an exemplary embodiment.

**FIG. 12** is an explanatory diagram illustrating some of the processes for preparing the first wafer according to the exemplary embodiment.

**FIG. 13** is a plan view illustrating a schematic configuration of a wafer processing apparatus according to the exemplary embodiment.

**FIG. 14** is a plan view illustrating a schematic configuration of an interface modifying apparatus according to the exemplary embodiment.

**FIG. 15** is a side view illustrating the schematic configuration of the interface modifying apparatus according to the exemplary embodiment.

**FIG. 16** is an explanatory diagram schematically illustrating bevel fill according to a first exemplary embodiment.

**FIG. 17** is an explanatory diagram schematically illustrating the bevel fill according to the first exemplary embodiment.

**FIG. 18** is an explanatory diagram illustrating an exemplary operation of the bevel fill according to the first exemplary embodiment.

**FIG. 19** is an explanatory diagram illustrating an exemplary operation of the bevel fill according to the first exemplary embodiment.

**FIG. 20** is an explanatory diagram schematically illustrating the bevel fill according to a second exemplary embodiment.

**FIG. 21** is an explanatory diagram schematically illustrating formation of a separation starting point according to the second exemplary embodiment.

**FIG. 22** is an explanatory diagram schematically illustrating the formation of the separation starting point according to the second exemplary embodiment.

**FIG. 23** is an explanatory diagram illustrating an exemplary operation of bevel fill and separation according to the second exemplary embodiment.

**FIG. 24** is an explanatory diagram schematically illustrating formation of a separation starting point according to a third exemplary embodiment.

**FIG. 25A** to **FIG. 25C** are explanatory diagrams illustrating a wafer processing according to a comparative example.

## **DETAILED DESCRIPTION**

**[0009]** In a manufacturing process of a semiconductor device, in a combined wafer in which two sheets of semiconductor substrates (hereinafter, referred to as “wafers”) are bonded to each other, a device layer formed on a front surface of a first wafer is transferred to a second wafer. When the device layer is transferred from the first wafer to the second wafer, laser light is radiated to a separation layer included in the first wafer to reduce a bonding force between the first wafer and the second wafer and separate the first wafer from the second wafer. The separated first wafer is reused and then bonded to a subsequent second wafer.

**[0010]** At an outer peripheral portion of a combined wafer T, a non-bonded region B in which bevel portions of a first wafer W and a second wafer S are not bonded to each other may be formed (see **FIG. 2**). The present inventors have diligently studied and found that during the separation of the first wafer W, even if the bonding force at the separation layer of the first wafer W is reduced, the separation may preferentially occur in another region near the non-bonded region B, rather than at the separation layer. For example, when an upward force  $F_{up}$  is applied

to an outer peripheral portion  $W_e$  of the first wafer  $W$  as shown in **FIG. 25A**, a portion of a bevel of the first wafer  $W$ , corresponding to the non-bonded region  $B$ , may be separated from the combined wafer  $T$  while still bonded to the first wafer  $W$  as shown in **FIG. 25B**. In another example, as shown in **FIG. 25C**, the separation may progress such that a device region of the second wafer  $S$  (or the first wafer  $W$ ) is torn away from an outer peripheral edge of a bonding surface between the first wafer  $W$  and the second wafer  $S$ , and extends across a front surface of the second wafer  $S$ .

[0011] Although the reason for such inappropriate separation is not clear, it is assumed that a stress, which is concentrated on the separation layer, is also concentrated, besides the separation layer, in a region near the outer peripheral edge of the bonding surface between the first wafer  $W$  and the second wafer  $S$ , and the separation is initiated from this region.

[0012] When a portion of the bevel is lost as shown in the example of **FIG. 25B**, a region, in which a device can be formed, (device-formable region) of the first wafer  $W$  separated from the combined wafer  $T$  becomes limited, which may result in a reduction in productivity. Moreover, in a process in which the bonding and the separation are repeated two or more times, such bevel loss is also repeated, which may lead to a significant reduction in the device-formable region.

[0013] When the separation progresses such that the device region of the second wafer  $S$  (or the first wafer  $W$ ) is torn away as shown in the example of **FIG. 25C**, the productivity may be directly reduced.

[0014] The technique according to the present disclosure enables the appropriate separation of the first substrate and the second substrate in the combined substrate in which the first substrate and the second substrate are bonded to each other. Hereinafter, a manufacturing method of a semiconductor device according to the present exemplary embodiment will be described with reference to the accompanying drawings. Further, in the present specification and

drawings, parts having substantially the same functions and configurations will be assigned same reference numerals, and redundant description thereof will be omitted.

**[0015]** In the manufacturing method of the semiconductor device according to the present exemplary embodiment, the first wafer W as a first substrate is prepared first (see St1 of **FIG. 1**) and the second wafer S as a second substrate is prepared (see St2 of **FIG. 1**). The first wafer W and the second wafer S may be prepared in parallel. Hereinafter, as shown in **FIG. 2** and **FIG. 3A** to **FIG. 3C**, in the first wafer W, a surface bonded to the second wafer S is referred to as a front surface Wa, and a surface opposite to the front surface Wa is referred to as a rear surface Wb. Likewise, in the second wafer S, a surface bonded to the first wafer W is referred to as a front surface Sa, and a surface opposite to the front surface Sa is referred to as a rear surface Sb.

**[0016]** The first wafer W prepared in St1 is, for example, a semiconductor wafer such as a silicon substrate. In an exemplary embodiment, the first wafer W has a substantially circular plate shape. As shown in **FIG. 3A**, a stacked film composed of a plurality of films is formed on the front surface Wa of the first wafer W. The stacked film includes, in order from the front surface Wa side, a laser absorption layer P, an etching stop layer Q, a device layer Dw, and a front surface film Fw. Each of the laser absorption layer P, the etching stop layer Q, the device layer Dw, and the front surface film Fw is formed on the first wafer W by a process including, for example, CVD (Chemical Vapor Deposition) in a film formation apparatus (not shown) or RIE (Reactive Ion Etching) in an etching apparatus (not shown). Further, another desired film may be formed, as a component of the stacked film, between any adjacent layers among the laser absorption layer P, the etching stop layer Q, the device layer Dw, and the front surface film Fw. Details of the formation of the stacked film will be described later.

**[0017]** The device layer Dw according to the present exemplary embodiment includes at least a portion of a memory cell array of a NAND-type flash memory. However, the technique according to the present disclosure is not limited thereto and is also applicable to the manufacture of other semiconductor devices by bonding substrates having other desired devices. In an exemplary embodiment, the device layer Dw includes at least a portion of a memory cell array of a DRAM. In another exemplary embodiment, the device layer Dw includes at least a portion of a peripheral circuit for controlling a memory cell array of a NAND-type flash memory or a DRAM. In some cases, during St1, no device is formed in the device layer Dw, and a device may be formed in a subsequent process. In other words, the device layer Dw may be a device-to-be-formed region in which a device is to be formed in a process subsequent to St1.

**[0018]** Examples of the front surface film Fw include an oxide film (a THOX film, a SiO<sub>2</sub> film, a TEOS film, *etc.*), a SiC film, a SiCN film, or an adhesive. The front surface film Fw of the first wafer W forms a first bonding layer according to the present disclosure.

**[0019]** The laser absorption layer P absorbs laser light (for example, CO<sub>2</sub> laser light) as described below. For example, the laser absorption layer P may be formed of an oxide film (a SiO<sub>2</sub> film or a TEOS film), but is not particularly limited thereto as long as it absorbs laser light.

**[0020]** The etching stop layer Q is configured to allow selective wet etching at a separation surface of the combined wafer T after the separation of the first wafer W. Specifically, when the first wafer W is separated, the laser absorption layer P serves as a main separation surface. Thus, after the separation, a portion of the laser absorption layer P and the etching stop layer Q remain on the first device layer Dw. In this state, the laser absorption layer P is first removed by the selective etching between the laser absorption layer P and the etching stop layer Q. Then, the etching stop layer Q is removed by the selective etching between the etching stop layer Q and the

first device layer Dw. As a result, a total thickness variation TTV of the first device layer Dw after the wet etching can be improved. As a material of the etching stop layer Q, polycrystalline silicon (poly-Si) may be used. However, the material is not particularly limited thereto as long as it ensures the etching selectivity between the etching stop layer Q and the first device layer Dw. Details of the method of forming the etching stop layer Q will be described later.

**[0021]** The second wafer S prepared in St2 is, for example, a semiconductor wafer such as a silicon substrate. In an exemplary embodiment, the second wafer S has a substantially circular plate shape. As shown in **FIG. 3B**, a stacked film Ms is formed on the front surface Sa of the second wafer S. The stacked film Ms includes, in order from the front surface Sa side, a device layer Ds and a front surface film Fs. Each of the device layer Ds and the front surface film Fs is formed on the second wafer S by a process including, for example, CVD in a film formation apparatus (not shown).

**[0022]** The device layer Ds and the front surface film Fs are the same as the device layer Dw and the front surface film Fw, respectively, of the first wafer W. The front surface film Fs of the second wafer S forms a second bonding layer according to the present disclosure. The device layer Ds according to the present exemplary embodiment includes at least a portion of a peripheral circuit for controlling a memory cell array of a NAND-type flash memory. In an exemplary embodiment, when the device layer Dw of the first wafer W includes at least a portion of a memory cell array of a DRAM, the device layer Ds includes at least a portion of a peripheral circuit for controlling the memory cell array. In another exemplary embodiment, when the device layer Dw of the first wafer W includes at least a portion of a peripheral circuit for controlling a memory cell array, the device layer Ds includes at least a portion of a memory cell array of a NAND-type flash memory. In yet another exemplary embodiment, when the device layer Dw of the first wafer W

includes at least a portion of a peripheral circuit for controlling a memory cell array, the device layer Ds includes at least a portion of a memory cell array of a DRAM.

**[0023]** After the first wafer W and the second wafer S are prepared as described above, the first wafer W and the second wafer S are bonded to each other to form a first combined wafer T1 as a combined substrate, as shown in **FIG. 3C** (see St3 of **FIG. 1** and **FIG. 2**). In St3, the front surface film Fw of the first wafer W is bonded to the front surface film Fs of the second wafer S. The method of bonding the first wafer W and the second wafer S is not particularly limited. For example, in a surface modification apparatus (not shown), the front surface films Fw and Fs are modified by plasma processing, and in a surface hydrophilization apparatus (not shown), the front surface films Fw and Fs are hydrophilized by supplying pure water. Then, in a bonding apparatus (not shown), the front surface films Fw and Fs are bonded to each other by van der Waals forces and hydrogen bonds (intermolecular forces).

**[0024]** Thereafter, as shown in **FIG. 4** or **FIG. 5**, bevel fill is performed at a non-bonded region B1 in a peripheral portion of the first combined wafer T1 (see St4 of **FIG. 1** and **FIG. 2**). The bevel fill includes injecting a liquid filler G into a bevel portion including the non-bonded region B1 of the first combined wafer T1. In an exemplary embodiment, the bevel fill includes injecting the liquid filler G into a non-bonded region B, and then, baking (sintering) to solidify the filler G. For example, in a bevel fill apparatus 70 to be described below, the first combined wafer T1 is rotated while the liquid filler G is injected from an injector 9. Thus, the filler G is filled in the non-bonded region B1 along the entire circumference of the first combined wafer T1. As shown in **FIG. 4**, the filler G may be filled only in the non-bonded region B1. Alternatively, as shown in **FIG. 5**, the filler G may be filled in the entire bevel portion including the non-bonded region B1. For example, the first combined wafer T1 filled with the filler G is then sent to a baking apparatus 80 to be described

below, and the filler G is baked. In an exemplary embodiment, the first combined wafer T1 is subsequently sent to a cleaning apparatus 90 to be described below, and any excess filler G attached to unnecessary portions is removed by cleaning.

**[0025]** Then, as shown in **FIG. 6**, laser light L is radiated to the laser absorption layer P (see St5 of **FIG. 1** and **FIG. 2**). In St5, for example, in a laser processing apparatus 50 to be described below, laser light is radiated in a pulse shape to the laser absorption layer P or to an interface between the laser absorption layer P and the etching stop layer Q. The laser light may be determined depending on a material of a laser radiation target such as the laser absorption layer P. In an exemplary embodiment, the laser light is CO<sub>2</sub> laser light having a wavelength of, for example, 8.9  $\mu\text{m}$  to 11  $\mu\text{m}$ . In an exemplary embodiment, the laser light is IR laser light having a wavelength of, for example, 1.5  $\mu\text{m}$  to 2.5  $\mu\text{m}$ . When viewed from the top, the laser light L may be radiated to the entire surface of the laser absorption layer P in a spiral or concentric annular shape. Alternatively, the laser light L may be radiated to the laser absorption layer P in a pulse shape while moving a lens (not shown) provided in the laser radiation apparatus in a linear direction. In this case, for example, a linear moving mechanism (transporter) may be provided to move the lens in a horizontal direction, or the laser light from the lens may be scanned by using a galvanometer scanner (not shown). The laser light L passes through the first wafer W from the rear surface Wb side of the first wafer W and is absorbed by the laser absorption layer P. The laser light L causes a reduction in bonding strength at the laser absorption layer P, at an interface between the laser absorption layer P and the wafer W, or at the interface between the laser absorption layer P and the etching stop layer Q.

**[0026]** In the following description, the interface within the first combined wafer T1 at which the bonding strength is reduced (an inner surface of the laser absorption layer P in the

present exemplary embodiment) may be referred to as a “separation surface.” In the present exemplary embodiment, “reduced bonding strength” means a state in which the bonding strength is reduced compared with that obtained before the radiation of the laser light L, and includes the separation between the laser absorption layer P and the etching stop layer Q.

[0027] Then, as shown in **FIG. 7A** and **FIG. 7B**, the first wafer W is separated from the second wafer S in the first combined wafer T1 (see St6 of **FIG. 1** and **FIG. 2**). In St6, for example, in a separation apparatus 60 to be described below, the first wafer W is separated starting at the laser absorption layer P where the bonding strength is reduced in St5. In the present disclosure, the second wafer S to which at least some of the layers formed on the first wafer W are transferred and from which the first wafer W is separated is referred to as “the second wafer S onto which the layers are transferred,” or simply as “the second wafer S.” In the example of **FIG. 7A** and **FIG. 7B**, a structure onto which the first device layer Dw is transferred together with the front surface films Fw and Fs, and the second device layer Ds is referred to as “the second wafer S onto which the first device layer Dw is transferred,” or simply as “the second wafer S.” The same applies to a second combined wafer T2 to be described below.

[0028] The method of separating the first wafer W is not particularly limited. For example, as shown in **FIG. 7A**, an attraction chuck 210 is configured to attract and hold the rear surface Sb of the second wafer S, and an attraction pad 211 is configured to attract and hold the front surface Wa of the first wafer W. Thereafter, as shown in **FIG. 7B**, while the attraction pad 211 attracts and holds the first wafer W, the attraction pad 211 is raised to separate the first wafer W. In this case, as described above, since the bonding strength is reduced within the laser absorption layer P or at the interface between the laser absorption layer P and the etching stop layer Q by the radiation of the laser light L, the first wafer W can be separated without applying a large load. Further, since

the non-bonded region B1 has undergone the bevel fill, a bonding force is generated in the non-bonded region B1. Thus, the separation at the interface can be ensured. Thus, loss of a portion of the bevel, as shown in the comparative example of **FIG. 25A** to **FIG. 25C**, can be suppressed. As a result, the first device layer Dw transferred to the second wafer S can be enlarged, which can improve the productivity.

**[0029]** Then, in the first combined wafer T1 from which the first wafer W is separated, the separation surface is subjected to a surface treatment (St7 of **FIG. 1** and **FIG. 2**). In St7, for example, the separation surface may be cleaned in the cleaning apparatus 90. Alternatively, the separation surface may be planarized or removed by polishing in a polishing apparatus (not shown) or by etching in an etching apparatus (not shown). Details of the surface treatment according to the present exemplary embodiment will be described later.

**[0030]** In an exemplary embodiment, the surface treatment includes a CMP (Chemical Mechanical Polishing) process. In the CMP process, a polishing pad is brought into contact with the separation surface of the first combined wafer T1, and the surface is polished while a pressure is applied. In this case, the filler G according to the present exemplary embodiment serves to suppress damage to the non-bonded region at the bevel portion of the first combined wafer T1 caused by the applied pressure.

**[0031]** In an exemplary embodiment, a material of the filler G is selected based on its resistance to the laser radiation performed in St5. In this case, when the surface treatment of St7 includes CMP, it is desirable that the filler G also have a resistance to each process included in CMP. In an exemplary embodiment, when the filler G filled in St4 does not have a resistance to a process of CMP, the filler G is removed between the separation of the first wafer W (St6) and the execution of CMP in the surface treatment (St7). In this case, when CMP in the surface treatment St7 is

performed, another filler G having a resistance to each process included in CMP is re-filled in the non-bonded region B1 of the first combined wafer T1. Thus, during subsequent execution of CMP, the re-filled filler G serves to suppress the damage to the non-bonded region B1 as described above. The refilling of this filler G may be performed in the same manner as described above for St4.

**[0032]** Then, in the first combined wafer T1 after the surface treatment, a wiring layer Wr is formed (St8 of **FIG. 1** and **FIG. 2**). The wiring layer Wr may be formed by a known Back End of Line (BEOL) wiring process. Since, in the present exemplary embodiment, a third wafer U to be described below is bonded onto the wiring layer Wr of the first combined wafer T1, St8 is performed to form a front surface film Ft for bonding. In an exemplary embodiment, no other wafers are bonded onto the wiring layer Wr of the first combined wafer T1, and the manufacturing method is ended. In this case, the front surface film Ft for bonding may not be formed on the wiring layer Wr.

**[0033]** Thereafter, the third wafer U is prepared (St9 of **FIG. 1** and **FIG. 2**). In St9, preparation of the third wafer U is performed in the same manner as the preparation of the first wafer W in St1. That is, a stacked film including the laser absorption layer P, the etching stop layer Q, a third device layer Du, and a front surface film Fu is formed on the front surface of the third wafer U. The absorption layer P, the etching stop layer Q, the third device layer Du, and the front surface film Fu in the third wafer U according to the present exemplary embodiment are the same as the absorption layer P, the etching stop layer Q, the first device layer Dw, and the front surface film Fw, respectively, of the first wafer W. In an exemplary embodiment, the third device layer Du of the third wafer U includes a device different from the first device layer Dw of the first wafer W.

**[0034]** Then, as shown in **FIG. 1** and **FIG. 2**, the second wafer S onto which the first device layer Dw is transferred is bonded to the third wafer U to obtain the second combined wafer T2 as

a combined substrate (St10). In St10, bonding between the third wafer U and the second wafer S is performed in the same manner as the bonding between the first wafer W and the second wafer S in St3. Thereafter, the filler G is filled in a non-bonded region B2 of the second combined wafer T2 by bevel fill of the second combined wafer T2 (St11). In an exemplary embodiment, when the filler G filled in the non-bonded region B1 of the first combined wafer T1 in a process prior to St11 has been removed, the filler G is filled in both the non-bonded regions B1 and B2 in St11. Then, the radiation of the laser light L (St12), the separation of the third wafer U (St13), the surface treatment of the second wafer S onto which the third device layer Du is transferred (St14), and the formation of the wiring layer Wr (St15) are sequentially performed. St11 to St15 are the same as St4 to St8, respectively. In the present exemplary embodiment, after the wiring layer Wr is formed in St15, the manufacturing method is ended. In an exemplary embodiment, after the wiring layer Wr is formed in St15, another wafer (not shown) may be further bonded onto the wiring layer Wr of the second combined wafer T2 and the same processes as St3 to St8 may be performed. In the present disclosure, the first combined wafer T1 and the second combined wafer T2 may be collectively referred to as “the combined wafers T1 and T2.”

**[0035]** In the separation of St13, a bonding force is generated in the non-bonded regions B1 and B2 by the bevel fill. Thus, separation at a bonding interface between the second wafer S and the third wafer U can be ensured. Accordingly, even in a process in which the bonding and the separation are repeated two or more times, repetition of the bevel loss can be suppressed and consumption of the device-formable region can be suppressed.

**[0036]** The first wafer W separated in St7 is reused (St20 of **FIG. 1**). When the first wafer W is reused, the laser absorption layer P remaining on the first wafer W may be etched and removed in an etching apparatus (not shown). The etching of the laser absorption layer P may be

performed using dry etching or wet etching. Accordingly, the laser absorption layer P is selectively etchable relative to the front surface Wa of the first wafer W. In an exemplary embodiment, when a sacrificial layer is provided between the laser absorption layer P and the first wafer W, the selective etching is first performed between the laser absorption layer P and the sacrificial layer, and then the selective etching is performed between the sacrificial layer and the front surface Wa of the first wafer W.

**[0037]** After the laser absorption layer P is removed from the first wafer W, the same processing as St1 is subsequently performed on the first wafer W, and a separation layer Mw, the first device layer Dw, and the front surface film Fw are formed on the front surface Wa. In this way, the first wafer W is reused for a subsequent second wafer S. Even though the laser absorption layer P has been removed, the removed first wafer W is a bare wafer with no film on the front surface Wa and thus may be reused as the second wafer S in a subsequent process.

**[0038]** The third wafer U separated in St13 is also reused (St21 of **FIG. 1**). In St21, reuse of the third wafer U is performed in the same manner as the reuse of the first wafer W in St20.

**[0039]** Hereinafter, as a manufacturing method according to an exemplary embodiment, **FIG. 8** illustrates a case where at least a portion of a 3D NAND memory cell array is formed in the device layer Dw of the first wafer W in the preparation of the first wafer W (St1 of **FIG. 1**). The device layer Dw includes a memory hole H formed by the following exemplary method.

**[0040]** Specifically, the preparation of the first wafer W according to the present exemplary embodiment (St1 of **FIG. 1**) includes processes shown in **FIG. 9** and **FIG. 10A** to **FIG. 10C**. **FIG. 10A** to **FIG. 10C** illustrate states of the device layer Dw in main processes. The same applies to preparation of the third wafer U in St9 of **FIG. 1**.

**[0041]** First, the laser absorption layer P is formed on the front surface Wa of the first wafer W (St101 of **FIG. 9** and **FIG. 10A** to **FIG. 10C**). The laser absorption layer P is a desired oxide film (a SiO<sub>2</sub> film or a TEOS film).

**[0042]** Then, the etching stop layer Q is formed on the laser absorption layer P (St102 of **FIG. 9** and **FIG. 10A** to **FIG. 10C**). The etching stop layer Q is formed of polycrystalline silicon.

**[0043]** Thereafter, an etch stop structure ES is provided in a portion of the etching stop layer Q corresponding to a predetermined position where the memory hole H is to be formed (St103 of **FIG. 9**).

**[0044]** In St103, a recess ES' is first formed in the portion of the etching stop layer Q (St103a of **FIG. 10A** to **FIG. 10C**). Thereafter, a pad Pd and an oxide film Ox are deposited in the recess ES' (St103b of **FIG. 10A** to **FIG. 10C**). During High Aspect Ratio (HAR) etching for forming the memory hole H, the pad Pd serves as an etch stop to suppress etching of regions beneath the pad Pd, *e.g.*, the laser absorption layer P and the first wafer W. Examples of materials of the pad Pd include titanium nitride (TiN), tungsten (W), tungsten silicide (WSi<sub>2</sub>), and the like. However, the materials are not limited thereto, and other known materials having the above function may be used.

**[0045]** In an exemplary embodiment, the etch stop structure ES is configured without the pad Pd. In this case, the etching stop layer Q may be configured without the etch stop structure ES. Also, in this case, the etching stop layer Q may be formed with a sufficient film thickness to suppress the etching of the regions beneath the pad Pd during the etching process for forming the memory hole H.

[0046] Then, an alternating layer AL, as a stacked film in which a plurality of oxide films and a plurality of nitride films are alternately stacked, is formed on the etching stop layer Q (St104 of FIG. 9 and FIG. 10A to FIG. 10C).

[0047] Thereafter, a deep hole DH is formed by performing HAR etching to penetrate the alternating layer AL at the predetermined position where the memory hole H is to be formed (St105 of FIG. 9 and FIG. 10A to FIG. 10C). St105 may be performed using known patterning and etching apparatuses. The deep hole DH formed by etching stops at the etch stop structure ES and does not reach the laser absorption layer P and the first wafer W. Accordingly, subsequent separation at the laser absorption layer P can be appropriately performed. Further, the possibility for reuse of the separated first wafer W is enhanced.

[0048] Then, the etch stop structure ES is removed (St106 of FIG. 9 and FIG. 10A to FIG. 10C). The etch stop structure ES may be removed by dry etching.

[0049] Thereafter, in the deep hole DH from which the etch stop structure ES has been removed, the memory hole H is formed (St107 of FIG. 9 and FIG. 10A to FIG. 10C). The memory hole H may be formed by forming various films on a sidewall of the deep hole DH.

[0050] After the memory hole H is formed, the wiring layer Wr and the front surface film Fw are formed as shown in FIG. 10C (St108 of FIG. 9). The wiring layer Wr according to the present exemplary embodiment contains a conductive material that forms a signal network or a power supply network. The front surface film Fw includes a copper pad Cu that is electrically connected to the wiring layer Wr.

[0051] In an exemplary embodiment, a memory hole H having an even higher aspect ratio is obtained by further forming another deep hole DH above the deep hole DH formed in St105 and

St106. Specifically, as shown in **FIG. 11** and **FIG. 12**, after St101 to St106, St110 to St113 are performed and then, St107 and St108 are performed.

**[0052]** After St106, a sacrificial layer SL is first formed in the deep hole DH (St110 of **FIG. 11** and **FIG. 12**).

**[0053]** Then, another alternating layer AL, in which a plurality of oxide films and a plurality of nitride films are alternately stacked, is formed over the deep hole DH filled with the sacrificial layer SL (St111 of **FIG. 11** and **FIG. 12**). This another alternating layer AL is configured to include an etch stop portion EP. During HAR etching of this another alternating layer AL, the etch stop portion EP serves as an etch stop to suppress etching of a region beneath the etch stop portion EP. A material of the etch stop portion EP is not particularly limited as long as it ensures an etching selectivity with respect to the oxide films or the nitride films of this another alternating layer AL.

**[0054]** Thereafter, another deep hole DH is formed by performing HAR etching to penetrate this another alternating layer AL at the predetermined position where the memory hole H is to be formed (St112 of **FIG. 11** and **FIG. 12**). St112 is the same as St105. This another deep hole DH formed by etching stops at the etch stop portion EP.

**[0055]** Then, the etch stop portion EP is removed, and the sacrificial layer SL is also removed (St113 of **FIG. 11** and **FIG. 12**). The etch stop portion EP and the sacrificial layer SL may be removed by dry etching. In St113, the lower deep hole DH formed in St105 and St106 and the upper deep hole DH communicate with each other to thus form a single deep hole.

**[0056]** Thereafter, the memory hole H is formed by forming various films on a sidewall of the communicating deep hole DH in St107. Further, the wiring layer Wr and the front surface film Fw are formed in St108.

[0057] Referring back to **FIG. 8**, when the second wafer S is prepared (St2 of **FIG. 1**), the second wafer S including a peripheral circuit for controlling a memory cell array in the device layer Ds is prepared. The peripheral circuit according to the present exemplary embodiment includes a CMOS (Complementary Metal-Oxide-Semiconductor) and the wiring layer Wr electrically connected to the CMOS. Also, the front surface film Fs of the second wafer S includes the copper pad Cu electrically connected to the wiring layer Wr. The second wafer S in which the peripheral circuit has already been formed may be prepared in St2, or the second wafer S may be prepared by forming the peripheral circuit in St2.

[0058] After the first wafer W and the second wafer S are prepared as described above, they are bonded to obtain the first combined wafer T1 (St3 of **FIG. 1** and **FIG. 8**).

[0059] Then, the bevel fill at the non-bonded region B of the first combined wafer T1 (St4 of **FIG. 1** and **FIG. 8**), the radiation of the laser light L to the laser absorption layer P (St5 of **FIG. 1** and **FIG. 8**), and the separation of the first wafer W (St6 of **FIG. 1** and **FIG. 8**) are sequentially performed.

[0060] Thereafter, the surface treatment is performed on the separation surface of the first combined wafer T1 from which the first wafer W has been separated (St7 of **FIG. 1** and **FIG. 8**). In the surface treatment according to the present exemplary embodiment, the laser absorption layer P remaining on the separation surface of the first combined wafer T1 after the separation of the first wafer W is removed. Then, the etching stop layer Q is removed. The removal of the laser absorption layer P may include, for example, selective etching of the laser absorption layer P with respect to the etching stop layer Q. Further, the removal of the etching stop layer Q may include selective etching of the etching stop layer Q with respect to the device layer Dw of the first wafer W. By performing the surface treatment including the selective etching of the etching stop layer

Q, a total thickness variation TTV of the first combined wafer T1 after the surface treatment can be improved.

**[0061]** On the separation surface of the first combined wafer T1 after the surface treatment according to the present exemplary embodiment, at least a portion of the memory hole H included in the device layer Dw is exposed. Thereafter, the wiring layer Wr electrically connected to the exposed memory hole H is formed (St8 of **FIG. 1** and **FIG. 8**). In an exemplary embodiment, after the surface treatment, a portion of the memory hole H including an impurity-doped conductive polycrystalline silicon film is exposed. In this case, in St8, the wiring layer Wr may be formed to be electrically connected to the polycrystalline silicon film.

**[0062]** Then, in case that the first combined wafer T1 and the third wafer U are bonded to each other, the front surface film Ft for bonding may be formed. Subsequently, by performing bonding to the third wafer U and the like (St9 to St15), the second combined wafer T2 may be formed. In this case, like the first wafer W, the third wafer U may be configured to include at least a portion of a 3D NAND memory cell array.

**[0063]** Hereinafter, the bevel fill according to a first exemplary embodiment will be described. The bevel fill according to the first exemplary embodiment is performed for the combined wafer T, and may be performed for the first combined wafer T1 in St4 or for the second combined wafer T2 in St11 of the above-described exemplary embodiments. In **FIG. 16** to **FIG. 19**, depiction of the etching stop layer Q and the device layer Dw of the first wafer W and the device layer Ds of the second wafer S according to the above-described exemplary embodiment is omitted for convenience of description.

**[0064]** In the bevel fill according to the first exemplary embodiment, as shown in **FIG. 16**, the filler G is filled up to a predetermined second outer peripheral position E2 which is determined

based on a first outer peripheral position E1 in the front surface film Fw of the first wafer W, which serves as a first bonding layer of the combined wafer T, and is located radially inward of the first outer peripheral position E1. When the combined wafer T is viewed in cross section, the first outer peripheral position E1 in the front surface film Fw is the outermost position in a radial direction. When the combined wafer T is viewed in cross section, the second outer peripheral position E2 in the filler G is the outermost position in the radial direction. The same applies to second and third exemplary embodiments to be described below.

**[0065]** In an exemplary embodiment, the filler G may be filled to the second outer peripheral position E2 by controlling a supply rate of the filler G from the injector 9 or a rotation speed of the combined wafer T while rotating the combined wafer T as the liquid filler G is injected from the injector 9. In an exemplary embodiment, the filling of the filler G to the second outer peripheral position E2 may be performed by injecting the filler G into the combined wafer T to a position radially outward of the second outer peripheral position E2 and then removing the filler G back to the second outer peripheral position E2.

**[0066]** In an exemplary embodiment, a third outer peripheral position E3, which is the outermost position in the radial direction at an interface between the front surface film Fw and the filler G, may be determined as follows using a first distance D1 and a second distance D2 when the combined wafer T is viewed in cross section. The first distance D1 is the distance between a separation surface Sf, which is an interface where the bonding strength is reduced by the laser radiation to the laser absorption layer P, and a bonding interface Bf between the first wafer W and the second wafer S. The second distance D2 is the distance between the separation surface Sf and the third outer peripheral position E3. In this case, the third outer peripheral position E3 is determined such that the difference between D1 and D2 is greater than a predetermined threshold

Th. In the example shown in **FIG. 17** according to the present exemplary embodiment, the separation layer Sf is the interface between the laser absorption layer P and the first wafer W. However, the separation surface Sf may also be, for example, an inner surface of the laser absorption layer P or an interface between the laser absorption layer P and the etching stop layer Q according to the above-described exemplary embodiment.

**[0067]** In an exemplary embodiment, the third outer peripheral position E3 may be determined such that  $D1/D2$  is greater than a predetermined threshold Th2.

**[0068]** In the bevel fill according to the first exemplary embodiment, inappropriate separation as described above with reference to **FIG. 25A** to **FIG. 25C** can be suppressed by filling the filler G to the predetermined second outer peripheral position E2 located radially inward of the first outer peripheral position E1.

**[0069]** Although the reason why the inappropriate separation is suppressed by the bevel fill according to the first exemplary embodiment is not clear, the following operation example can be assumed. When the upward force  $F_{up}$  is applied to the outer peripheral portion We of the first wafer W as shown in **FIG. 18**, the stresses  $\sigma_1$  and  $\sigma_2$  are assumed to act near the outermost position of the bonding interface Bf between the first wafer W and the second wafer S, and near the third outer peripheral position E3, respectively. Since the contribution of the stress  $\sigma_2$  to the separation is greater than that of the stress  $\sigma_1$ , it is assumed that a crack Cr originates near the third outer peripheral position E3.

**[0070]** Further, as shown in **FIG. 19**, if the laser absorption layer P is formed extending to the non-bonded region B, the crack Cr originating from the third outer peripheral position E3 may not occur when the upward force  $F_{up}$  is applied to the outer peripheral portion We of the first

wafer W. It is assumed that this is because the separation at the separation layer Sf, which extends to the non-bonded region B, preferentially occurs.

**[0071]** Since the third outer peripheral position E3 is determined such that the difference between D1 and D2 is greater than a predetermined threshold Th, the inappropriate separation as described above can be further suppressed. Although the reason is not clear, the following operation example can be assumed. For the crack Cr shown in **FIG. 18**, it is assumed that a more suitable separation occurs when the crack Cr propagates toward the separation surface Sf. Therefore, it is assumed that since the third outer peripheral position E3 is determined as described above, the distance between the third outer peripheral position E3 and the separation surface Sf can be reduced, which facilitates the propagation of the crack Cr toward the separation surface Sf.

**[0072]** The present inventors have diligently studied and found that the above-described inappropriate separation tends to occur in the first wafer W having a stacked film with the large first distance D1. Herein, it is assumed that the stacked film with the large first distance D1 refers to a case where, as in the first wafer W according to the above-described exemplary embodiment, the device layer Dw is formed by repeating a plurality of processes, and, thus, the thickness of the entire stacked film increases. In particular, when the device layer Dw includes a memory cell array of a NAND-type flash memory, a considerable increase in the thickness of the stacked film including the device layer Dw is observed.

**[0073]** In the bevel fill according to the first exemplary embodiment, the above-described inappropriate separation can be suppressed even when the combined wafer T including the first wafer W having the stacked film with the large first distance D1 is separated.

**[0074]** Hereinafter, the bevel fill and the separation according to the second exemplary embodiment will be described. The bevel fill and the separation according to the second

exemplary embodiment is performed for the combined wafer T, and may be performed for the first combined wafer T1 in St4 and St6 or for the second combined wafer T2 in St11 and St13 of the above-described exemplary embodiment. In **FIG. 20** to **FIG. 23**, depiction of the etching stop layer Q and the device layer Dw of the first wafer W and the device layer Ds of the second wafer S according to the above-described exemplary embodiment is omitted for convenience of description.

**[0075]** In the bevel fill according to the second exemplary embodiment, as shown in **FIG. 20**, the filler G is filled up to the predetermined second outer peripheral position E2 which is determined based on a first outer peripheral position E1 in the front surface film Fw of the first wafer W, which serves as a first bonding layer of the combined wafer T, and is located radially outward of the first outer peripheral position E1.

**[0076]** Then, a separation starting point A is formed in the filler G of the combined wafer T after the bevel fill. The formation of the separation starting point A may be performed using a blade 220 provided in the separation apparatus 60 to be described below. In this case, as shown in **FIG. 21**, the blade 220 is inserted along the circumferential periphery of the filler G. When the blade 220 is further moved in a linear direction indicated by an arrow in **FIG. 21**, the separation starting point A where the strength of the filler G is lost is formed near the insertion position. Further, while the blade 220 remains inserted, the combined wafer T is rotated. Thus, as shown in **FIG. 22**, the separation starting point A is formed along the entire circumference of the combined wafer T when viewed from the top. Alternatively, the separation starting point A may be formed along the entire circumference of the combined wafer T by rotating the blade 220 around the periphery of the combined wafer T.

**[0077]** After the separation starting point A is formed, the first wafer W or the third wafer U is separated from the second wafer S, similarly to St6 and St13 described above according to the above-described exemplary embodiment.

**[0078]** The blade 220 can be moved for insertion into at least one point along the circumferential periphery of the filler G. The blade 220 forms a starting point forming device of the present disclosure.

**[0079]** In an exemplary embodiment, the starting point forming device of the present disclosure includes a moving mechanism 221 that holds the blade 220 to be movable at least in the horizontal direction. Also, the starting point forming device includes a sensor 222 that detects a horizontal position or horizontal pressure of the blade 220 with respect to the filler G in contact with the blade 220. The detected horizontal position or pressure of the blade 220 from the sensor 222 is output to a control device 61. Further, based on the horizontal position or pressure of the blade 220, the control device 61 controls the moving mechanism 221 to adjust the horizontal position of the blade 220 so that the separation starting point A is formed at a desired radial depth in the filler G. In an exemplary embodiment, when the separation starting point A is formed along the entire circumference of the filler G, the control device 61 controls the moving mechanism 221 to adjust the horizontal position of the blade 220 so that the radial depth of the separation starting point A is uniform over the entire circumference.

**[0080]** In an exemplary embodiment, after the separation starting point A is formed along the entire circumference of the interface between the first wafer W and the second wafer S, another separation starting point A may be further formed at one point of the interface. In this case, after the separation starting point A is formed along the entire circumference, a blade 150 is

further inserted toward the center at one point of the interface to form another separation starting point A.

**[0081]** In an exemplary embodiment, the starting point forming device of the present disclosure may include an ultrasonic oscillator (not shown) configured to apply ultrasonic vibration to the blade 220.

**[0082]** The starting point forming device is not limited to the exemplary embodiment including the blade 220, and may employ any configuration capable of forming the separation starting point A along the circumferential periphery of the filler G. For example, the separation apparatus 60 may include an air cutter (not shown) as the starting point forming device. The air cutter supplies air to the interface between the first wafer W and the second wafer S to form the separation starting point A. To facilitate the formation of the separation starting point A, the air may be compressed high-pressure air or heated high-temperature air. Alternatively, a water cutter configured to supply water to the interface between the first wafer W and the second wafer S may be used instead of the air cutter. The water supplied from the water cutter may be pressurized high-pressure water or heated high-temperature water.

**[0083]** Alternatively, the separation apparatus 60 may include a rotary cutter (not shown) as the starting point forming device. The rotary cutter may have a configuration in which the cutter is rotated by a motor (not shown). In this case, the rotary cutter is inserted into the interface between the first wafer W and the second wafer S while being rotated to form the separation starting point A.

**[0084]** Alternatively, the separation apparatus 60 may include a heater (not shown) as the starting point forming device. The heater heats the interface between the first wafer W and the

second wafer S to expand the first wafer W and the second wafer S, and applies a thermal stress to the interface to form the separation starting point A.

**[0085]** As shown in **FIG. 21**, a suction mechanism 230 may be provided below the starting point forming device, such as the blade 220. The suction mechanism 230 is connected to a suction source (not shown) and sucks an atmosphere around the separation starting point A. When the blade 220 is inserted into the filler G to form the separation starting point A, particles or the like may be generated by cutting. The suction mechanism 230 can remove such particles by suction and thus can maintain the interior of the separation apparatus 60 in a clean condition. Moreover, a down flow may be formed inside the separation apparatus 60 during the separation. In this case, the suction mechanism 230 may be provided below the blade 220 to more efficiently remove particles or the like.

**[0086]** In the bevel fill and separation according to the second exemplary embodiment, the filler G may be filled up to the predetermined second outer peripheral position E2 located radially outward of the first outer peripheral position E1, and the separation starting point A may be formed along the entire circumference of the filler G. Thus, the inappropriate separation as described above with reference to **FIG. 25A** to **FIG. 25C** can be suppressed.

**[0087]** Although the reason why the inappropriate separation is suppressed by the bevel fill according to the second exemplary embodiment is not clear, the following operation example can be assumed. The present inventors have diligently studied and found that when the filler G is filled up to the second outer peripheral position E2 located radially outward of the first outer peripheral position E1, the crack Cr may occur at a random position in an interface between the filler G and the front surface film Fw among various positions along the circumference of the combined wafer T during the separation. The crack Cr at the random position may cause the

above-described inappropriate separation. However, in the separation according to the second exemplary embodiment, as shown in **FIG. 23**, when the upward force  $F_{up}$  is applied to the outer peripheral portion  $W_e$  of the first wafer  $W$ , a stress tends to concentrate in a region near the separation starting point  $A$  at the interface between the filler  $G$  and the front surface film  $F_w$ . Thus, it is assumed that the crack  $Cr$  originates from this region. Further, since the separation starting point  $A$  is formed along the entire circumference of the filler  $G$ , the crack  $Cr$  uniformly propagates along the entire circumference. Thus, it is assumed that separation is appropriately performed.

**[0088]** Hereinafter, the bevel fill and the laser radiation according to the third exemplary embodiment will be described. The bevel fill and the laser radiation according to the third exemplary embodiment is performed for the combined wafer  $T$ , and may be performed for the first combined wafer  $T1$  in  $St4$  and  $St5$  or for the second combined wafer  $T2$  in  $St11$  and  $St12$  of the above-described exemplary embodiment. In **FIG. 19**, depiction of the etching stop layer  $Q$  and the device layer  $D_w$  of the first wafer  $W$  and the device layer  $D_s$  of the second wafer  $S$  according to the above-described exemplary embodiment is omitted for convenience of description.

**[0089]** The bevel fill according to the third exemplary embodiment is identical to that of the second exemplary embodiment. As shown in **FIG. 20**, the filler  $G$  is filled up to the predetermined second outer peripheral position  $E2$  which is determined based on the first outer peripheral position  $E1$  of the front surface film  $F_w$  of the first wafer  $W$ , which serves as the first bonding layer of the combined wafer  $T$ , and is located radially outward of the first outer peripheral position  $E1$ .

**[0090]** Then, the separation starting point  $A$  is formed in the filler  $G$  of the combined wafer  $T$  after the bevel fill. As shown in **FIG. 24**, the separation starting point  $A$  is formed by radiating laser light to the filler  $G$ . The laser radiation is the same as the radiation of the laser light  $L$  to the

laser absorption layer P described in St5 of the above-described exemplary embodiment. By radiating the laser light L to the filler G, the separation starting point A where the strength of the filler G is lost is formed. The separation starting point A may be formed along the entire circumference of the filler G in the same manner as in the separation according to the second exemplary embodiment, as shown in **FIG. 22**.

**[0091]** In the bevel fill and the laser radiation according to the third exemplary embodiment, it is possible to obtain the same operations and effects as those achieved in the bevel fill and the separation according to the second exemplary embodiment. That is, as shown in **FIG. 23**, when the upward force  $F_{up}$  is applied to the outer peripheral portion  $W_e$  of the first wafer W, a stress tends to concentrate in a region near the separation starting point A at the interface between the filler G and the front surface film  $F_w$ , and, thus, it is assumed that the crack Cr originates from this region. Further, since the separation starting point A is formed along the entire circumference of the filler G, the crack Cr uniformly propagates along the entire circumference. Thus, it is assumed that separation is appropriately performed. Accordingly, the inappropriate separation as described above with reference to **FIG. 25A** to **FIG. 25C** can be suppressed.

**[0092]** Hereinafter, a wafer processing system 1 will be described as an example of the substrate processing system capable of performing the bonding and the separation of the first substrate and the second substrate in the above-described wafer processing method.

**[0093]** As shown in **FIG. 13**, the wafer processing system 1 has a configuration in which a carry-in/out station 2 and a processing station 3 are connected as one body. In the carry-in/out station 2, a cassette C capable of accommodating therein a plurality of combined wafers T1 and T2 is carried to/from the outside, for example. The processing station 3 is equipped with various types

of processing apparatuses configured to perform required processings on the combined wafers T1 and T2.

**[0094]** The carry-in/out station 2 is equipped with a cassette placement table 10 on which the cassette C capable of accommodating therein the plurality of combined wafers T1 and T2 is placed. Further, a wafer transfer device 20 is provided adjacent to the cassette placement table 10 on the positive X-axis side of the cassette placement table 10. The wafer transfer device 20 is configured to be moved on a transfer path 21 extending in the Y-axis direction to transfer the combined wafers T1 and T2 between the cassette C of the cassette placement table 10 and a transition stage 30 to be described later.

**[0095]** In the carry-in/out station 2, the transition stage 30 configured to deliver the combined wafers T1 and T2 to/from the processing station 3 is provided adjacent to the wafer transfer device 20 on the positive X-axis side of the wafer transfer device 20.

**[0096]** Disposed in the processing station 3 are a wafer transfer device 40, a laser processing apparatus 50, the separation apparatus 60, the bevel fill apparatus 70, a bake apparatus 80, and the cleaning apparatus 90.

**[0097]** The wafer transfer device 40 is provided on the positive X-axis side of the transition stage 30. The wafer transfer device 40 is configured to be movable on a transfer path 41 extending in the X-axis direction to transfer the combined wafers T1 and T2 to/from the transition stage 30 of the carry-in/out station 2, the laser processing apparatus 50, the separation apparatus 60, the bevel fill apparatus 70, the bake apparatus 80, and the cleaning apparatus 90.

**[0098]** The laser processing apparatus 50 is configured to radiate the laser light L1 to the interface between the first wafer W and the second wafer S to form a bonding-force-reduced

region in which the first wafer W and the second wafer S are separated. The laser processing apparatus 50 includes a control device 51 to be described below.

**[0099]** As shown in **FIG. 14** and **FIG. 15**, the laser processing apparatus 50 has a chuck 100 configured to hold the combined wafers T1 and T2 on a top surface thereof. The chuck 100 attracts and holds the rear surface Sb of the second wafer S with the first wafer W positioned on the upper side and the second wafer S positioned on the lower side. The chuck 100 is supported by a slider table 102 with an air bearing 101 therebetween. A rotating mechanism 103 is provided on a bottom surface of the slider table 102. The rotating mechanism 103 has, for example, a motor as a driving source embedded therein. The chuck 100 is configured to be rotatable around a vertical axis by the rotating mechanism 103 via the air bearing 101. The slider table 102 is configured to be movable on a rail 106 extending on a base 105 in the Y-axis direction by a moving mechanism 104 provided on a bottom surface thereof. Further, although not particularly limited, a driving source of the moving mechanism 104 may be, for example, a linear motor.

**[00100]** A laser head 110 is disposed above the chuck 100. The laser head 110 has a lens 111. The lens 111 is configured to radiate the laser light L1 to the laser absorption layer P of the combined wafers T1 and T2 held by the chuck 100. Thus, the first wafer W is separated from the stacked film at the portion radiated with the laser light L1, and the bonding-force-reduced region in which the first wafer W and the second wafer S are separated is formed. The formation position of the bonding-force-reduced region is not particularly limited so long as the separation is caused at the interface between the first wafer W and the second wafer S to reduce the bonding force. That is, the separation between the first wafer W and the second wafer S may occur at an interface between the first wafer W and the stacked film, as shown in the drawing, or at an interface within the stacked films, or at an interface between the second wafer S and the stacked film.

**[00101]** The laser head 110 is supported by a supporting member 112. The laser head 110 is configured to be movable up and down by an elevating mechanism 114 along a rail 113 extending in a vertical direction. Further, the laser head 110 is configured to be movable in the Y-axis direction by a moving mechanism 115. Each of the elevating mechanism 114 and the moving mechanism 115 is supported on a supporting column 116.

**[00102]** Moreover, in the shown example, the chuck 100 is configured to be rotated and horizontally moved relative to the laser head 110 by the rotating mechanism 103 and the moving mechanism 104. However, the laser head 110 may be configured to be rotated and horizontally moved relative to the chuck 100. Alternatively, both the chuck 100 and the laser head 110 may be configured to be rotatable and horizontally movable relative to each other.

**[00103]** The separation apparatus 60 includes the suction chuck 210 and the suction pad 211 as shown in **FIG. 7A**. By the method described above, the first wafer W is separated from the second wafer S starting from the bonding-force-reduced region. In an exemplary embodiment, the separation apparatus 60 includes the blade 220, the movement mechanism 221, and the sensor 222.

**[00104]** The bevel fill apparatus 70 includes the injector 9 as shown in **FIG. 4** or **FIG. 5**, and is configured to inject the filler G into the bevel portion of the combined wafers T1 and T2. For example, the bevel fill apparatus 70 includes a chuck (not shown) identical to the chuck 100. The combined wafers T1 and T2 are held on the chuck 100, and while the combined wafers T1 and T2 are rotated, the filler G is injected from the injector 9 into the bevel portion. Thus, the filler G can be injected into the bevel portion along the entire circumference of the combined wafers T1 and T2. In an exemplary embodiment, the bevel fill apparatus 70 is controlled such that the filler G is injected only into the non-bonded region of the bevel portion of the combined wafers T1 and T2.

**[00105]** The bake apparatus 80 is configured to perform the baking (sintering) of the filler G injected into the bevel portion of the combined wafers T1 and T2.

**[00106]** After the filler G is injected by the bevel fill apparatus 70 or baked by the bake apparatus 80, the cleaning apparatus 90 performs cleaning on the first wafer W and the second wafer S to remove particles on these wafers or the filler G adhering to undesired regions. The cleaning method is not particularly limited.

**[00107]** In an exemplary embodiment, the wafer processing system 1 is divided into a plurality of systems including: one wafer processing system including the laser processing apparatus 50 and the separation apparatus 60; and another wafer processing system including the bevel fill apparatus 70 and the bake apparatus 80. By transferring the wafers W, S and U and the combined wafers T1 and T2 between the plurality of systems, desired processings are performed on each wafer.

**[00108]** The above-described wafer processing system 1 is equipped with the control device 51, the control device 61, and at least one control device 95. The control device 51 is configured to individually control the operation of the laser processing apparatus 50. The control device 61 is configured to individually control the operation of the separation apparatus 60. The control device 95 is configured to oversee the control of a series of wafer processings in the wafer processing system 1.

**[00109]** Each of the control device 51, the control device 61, and the control device 95 processes computer-executable instructions that cause the laser processing apparatus 50, the separation apparatus 60, and the wafer processing system 1 to execute various processes described in the present disclosure. Each of the control device 51, the control device 61, and the control device 95 may be configured to control each component of the laser processing apparatus

50, the separation apparatus 60, and the wafer processing system 1 to execute the various processes described herein. In an exemplary embodiment, a part or all of the control device 51 may be included in the laser processing apparatus 50, a part or all of the control device 61 may be included in the separation apparatus 60, or a part or all of the control device 955 may be included in the wafer processing system 1.

**[00110]** Each of the control device 51, the control device 61, and the control device 95 may include a processor, a storage, and a communication interface. Each of the control device 51, the control device 61, and the control device 95 is implemented by, for example, a computer. The processor may be configured to read from the storage a program which provides a logic or routine making it possible to perform the various control operations, and execute the read program to thereby perform the various control operations. This program may be stored in the storage in advance, or acquired via a medium when necessary. The acquired program is stored in the storage, read from the storage, and executed by the processor. The medium may be various computer-readable storage media or may be a communication line connected to the communication interface. The storage medium may be a transitory one or a non-transitory one. The processor may be a CPU (Central Processing Unit) or may be one or more circuits. The storage may include a RAM (Random Access Memory), a ROM (Read Only Memory), an HDD (Hard Disk Drive), an SSD (Solid State Drive), or a combination thereof. The communication interface may communicate with the laser processing apparatus 50 and the wafer processing system 1 via a communication line such as a LAN (Local Area Network).

**[00111]** In the present exemplary embodiment, the control device 51 is individually provided for the laser processing apparatus 50. However, the control device 51 may be integrally configured with the control device 95. Likewise, although the control device 61 is individually

provided for the separation apparatus 60. However, the control device 61 may be integrally configured with the control device 95. In other words, the operations of the laser processing apparatus 50 and the separation apparatus 60 may be controlled by the control device 95.

**[00112]** The embodiments disclosed herein are illustrative in all aspects and do not limit the present disclosure. The above embodiments can be embodied in various forms. Further, the above-described embodiments may be omitted, substituted, or changed in various forms without departing from the scope and spirit of the appended claims. For example, the constituent elements of the above-described exemplary embodiments may be combined in various ways. From any of these various combinations, functions and effects for the respective constituent elements are naturally obtained, and other functions and other effects obvious to a person with ordinary skill in the art are also obtained from the description of the present specification.

**[00113]** Further, the effects described in the present specification are only explanatory or illustrative and are not limiting. That is, the technique according to the present disclosure may exhibit, together with or instead of the above-described effects, other effects obvious to a person with ordinary skill in the art from the description of the present specification.

## **EXPLANATION OF CODES**

**[00114]** B: Non-bonded region

P: Laser absorption layer

S: Second wafer

T: Combined wafer

W: First wafer

## **WE CLAIM**

[Claim 1] A semiconductor device manufacturing method, comprising:

performing, in a non-bonded region of a combined substrate which includes a first substrate having a laser absorption layer and a first bonding layer and a second substrate having a second bonding layer and in which the first bonding layer and the second bonding layer are bonded to each other, bevel fill by injecting a filler up to a predetermined second outer peripheral position which is determined based on a first outer peripheral position in the first bonding layer;

radiating laser to the laser absorption layer; and

separating the first substrate from the second substrate in the combined substrate.

[Claim 2] The semiconductor device manufacturing method of Claim 1,

wherein the second outer peripheral position is located radially inward of the first outer peripheral position.

[Claim 3] The semiconductor device manufacturing method of Claim 2,

wherein when a distance between a separation surface, which is formed between the first substrate and the second substrate and is formed by radiating the laser, and a bonding interface between the first bonding layer and the second bonding layer is set as a first distance,

when a distance between the separation surface and a third outer peripheral position, which is an outermost position in a radial direction at a contact interface between the first bonding layer and the filler, is set as a second distance, and

the third outer peripheral position is previously determined such that a difference between the first distance and the second distance is greater than a predetermined threshold.

[Claim 4]        The semiconductor device manufacturing method of Claim 1,  
wherein the second outer peripheral position is located radially outward of the first outer  
peripheral position, and

the method includes:

forming, before the separating of the first substrate from the second substrate, a  
separation starting point along an entire circumference of the filler when viewed from top.

[Claim 5]        The semiconductor device manufacturing method of Claim 4,  
wherein the separating of the first substrate from the second substrate includes:  
forming the separation starting point by using a starting point forming device.

[Claim 6]        The semiconductor device manufacturing method of Claim 5,  
wherein the starting point forming device includes a blade, and  
the method includes:  
forming, while the blade remains inserted in the filler, the separation starting point by  
rotating the blade and the combined substrate relative to each other.

[Claim 7]        The semiconductor device manufacturing method of Claim 4, further  
comprising:

forming the separation starting point by radiating laser to the laser absorption layer and  
radiating laser light to the filler.

[Claim 8]        The semiconductor device manufacturing method of Claim 1, further comprising:

forming an etching stop layer on the laser absorption layer; and  
forming a device layer on the etching stop layer.

[Claim 9]        The semiconductor device manufacturing method of Claim 8, further comprising:

forming a wiring layer; and  
forming a front surface film for bonding in the first substrate.

[Claim 10]       The semiconductor device manufacturing method of Claim 8, further comprising:

performing, after the separating of the first substrate from the second substrate, surface treatment of a separation surface of the second substrate onto which the device layer is transferred,  
wherein the etching stop layer is formed of a material that allows selective etching with respect to the separation surface, and  
the surface treatment includes removing the etching stop layer by performing the selective etching between the etching stop layer and the separation surface.

[Claim 11]       The semiconductor device manufacturing method of Claim 10,  
wherein the surface treatment includes exposing at least a portion of the device layer from the separation surface.

[Claim 12] The semiconductor device manufacturing method of Claim 8,

wherein the forming of the device layer includes:

forming a stacked film on the etching stop layer; and

forming a deep hole by etching the stacked film,

the forming of the etching stop layer includes:

forming an etch stop structure at a portion of the etching stop layer corresponding to a predetermined position where the deep hole is to be formed in the device layer, and

the etching for forming the deep hole stops at the etch stop structure.

[Claim 13] The semiconductor device manufacturing method of Claim 12,

wherein the etch stop structure includes a pad formed of one or more materials selected from titanium nitride, tungsten, and tungsten silicide.

[Claim 14] The semiconductor device manufacturing method of Claim 1, further

comprising:

removing, after the separating of the first substrate from the combined substrate, the filler filled in the non-bonded region by the bevel fill.

[Claim 15] The semiconductor device manufacturing method of Claim 14, further

comprising:

performing, after the separating of the first substrate from the combined substrate, surface treatment of a separation surface of the combined substrate from which the first substrate is separated; and

performing, after the removing of the filler and before the performing of the surface treatment of the separation surface, the bevel fill again in the non-bonded region of the combined substrate.

[Claim 16]      The semiconductor device manufacturing method of Claim 8, wherein the device layer includes at least a portion of a memory cell array.

[Claim 17]      The semiconductor device manufacturing method of Claim 16, wherein the second substrate includes another device layer, and the another device layer includes at least a portion of a peripheral circuit for controlling the memory cell array.

[Claim 18]      The semiconductor device manufacturing method of Claim 1, further comprising:

forming a second combined substrate by bonding a third substrate having a laser absorption layer to the combined substrate;

performing the bevel fill again in a non-bonded region of the second combined substrate;

radiating laser to the laser absorption layer of the third substrate; and

separating the third substrate from the second substrate in the second combined substrate.

[Claim 19]      A semiconductor device manufacturing system, comprising:

a laser radiation apparatus configured to radiate laser, after performing, in a non-bonded region of a combined substrate which includes a first substrate having a laser absorption layer and

a first bonding layer and a second substrate having a second bonding layer and in which the first bonding layer and the second bonding layer are bonded to each other, bevel fill by injecting a filler up to a predetermined second outer peripheral position which is determined based on a first outer peripheral position in the first bonding layer, to the laser absorption layer; and

a separation apparatus configured to separate the first substrate from the second substrate in the combined substrate.

[Claim 20] The semiconductor device manufacturing system of Claim 19, further comprising:

a bevel fill apparatus configured to perform the bevel fill in the non-bonded region of the combined substrate.