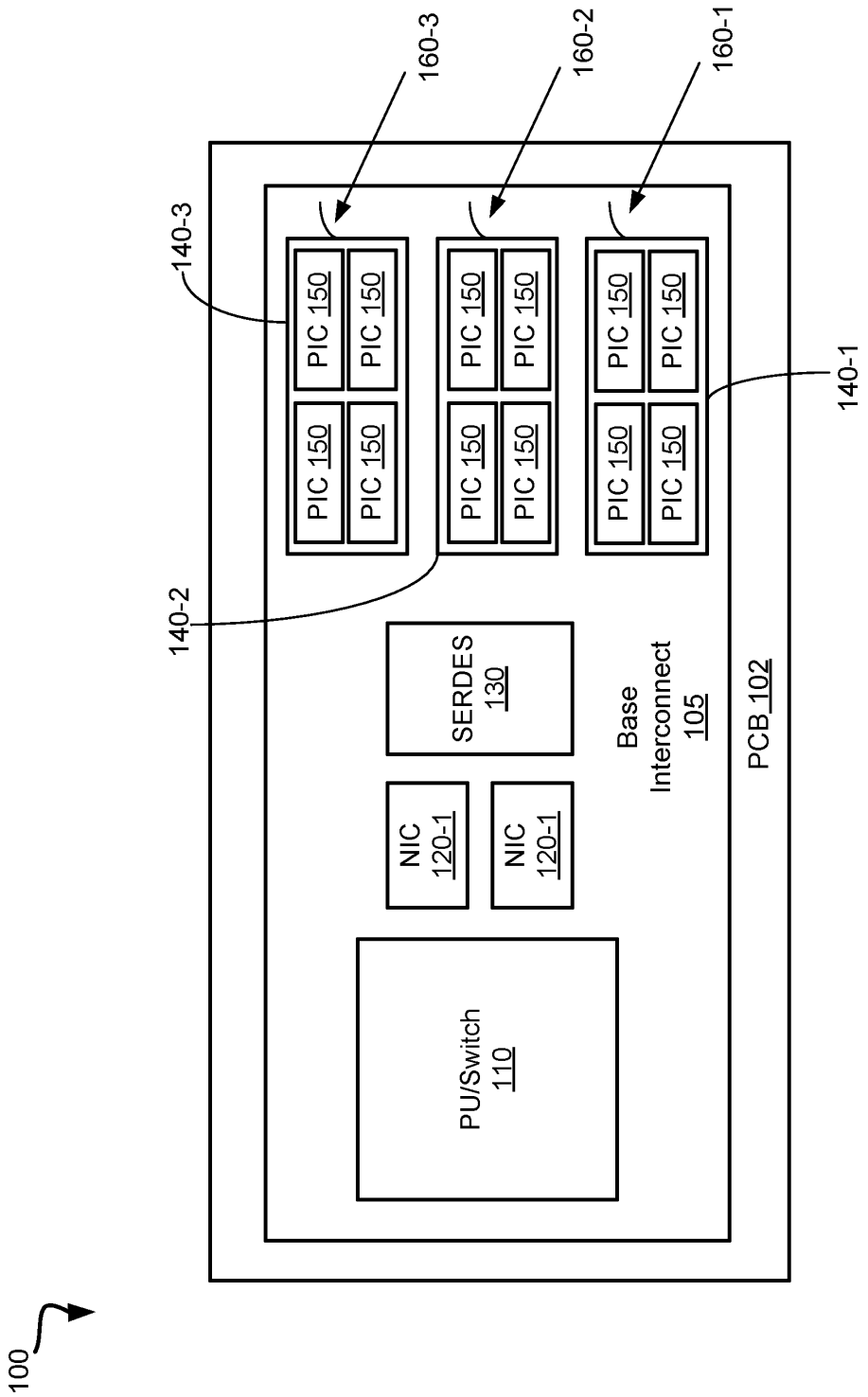
100
PCB 102
PU/Switch 110
NIC 120-1
NIC 120-1
SERDES 130
Base Interconnect 105
PIC 150
140-1
140-2
140-3
160-1
160-2
160-3

FIG. 1A

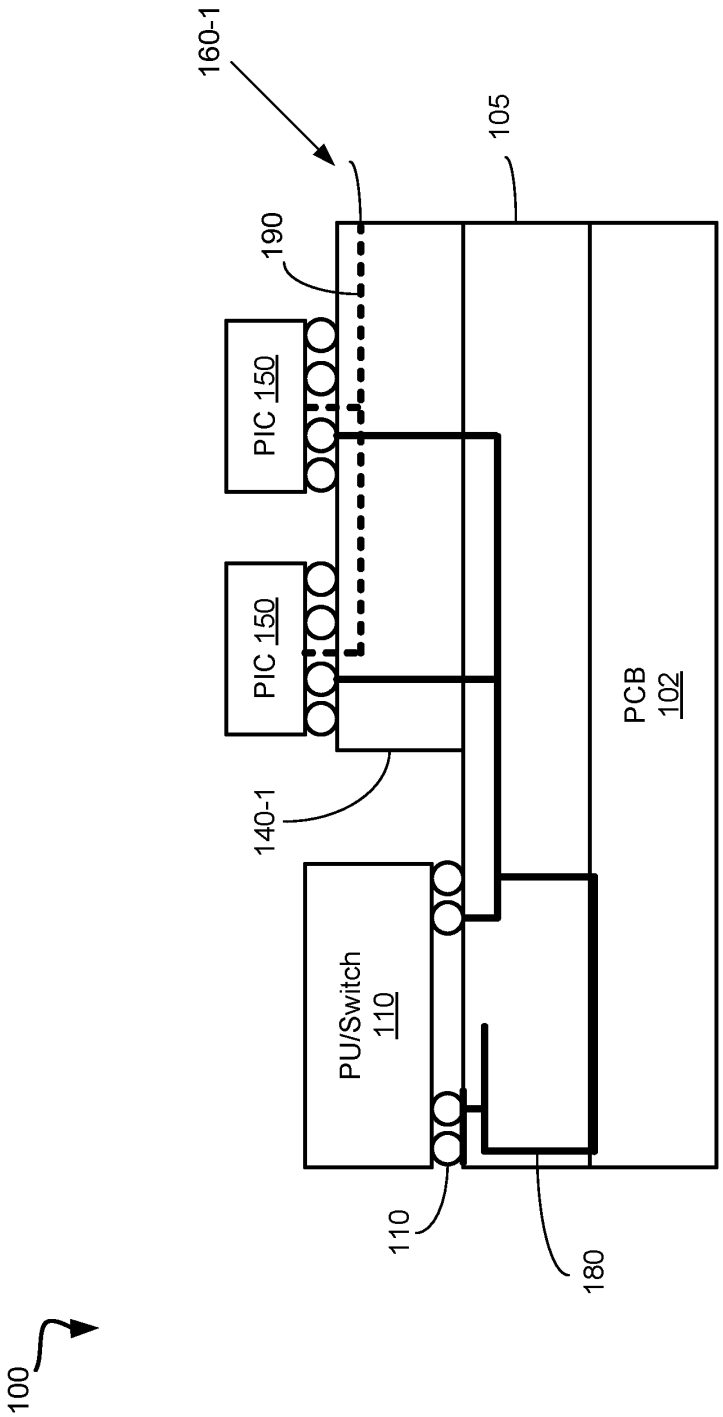
160-1
105
190
PIC 150
PIC 150
140-1
PU/Switch 110
PCB 102
110
180
100

FIG. 1B

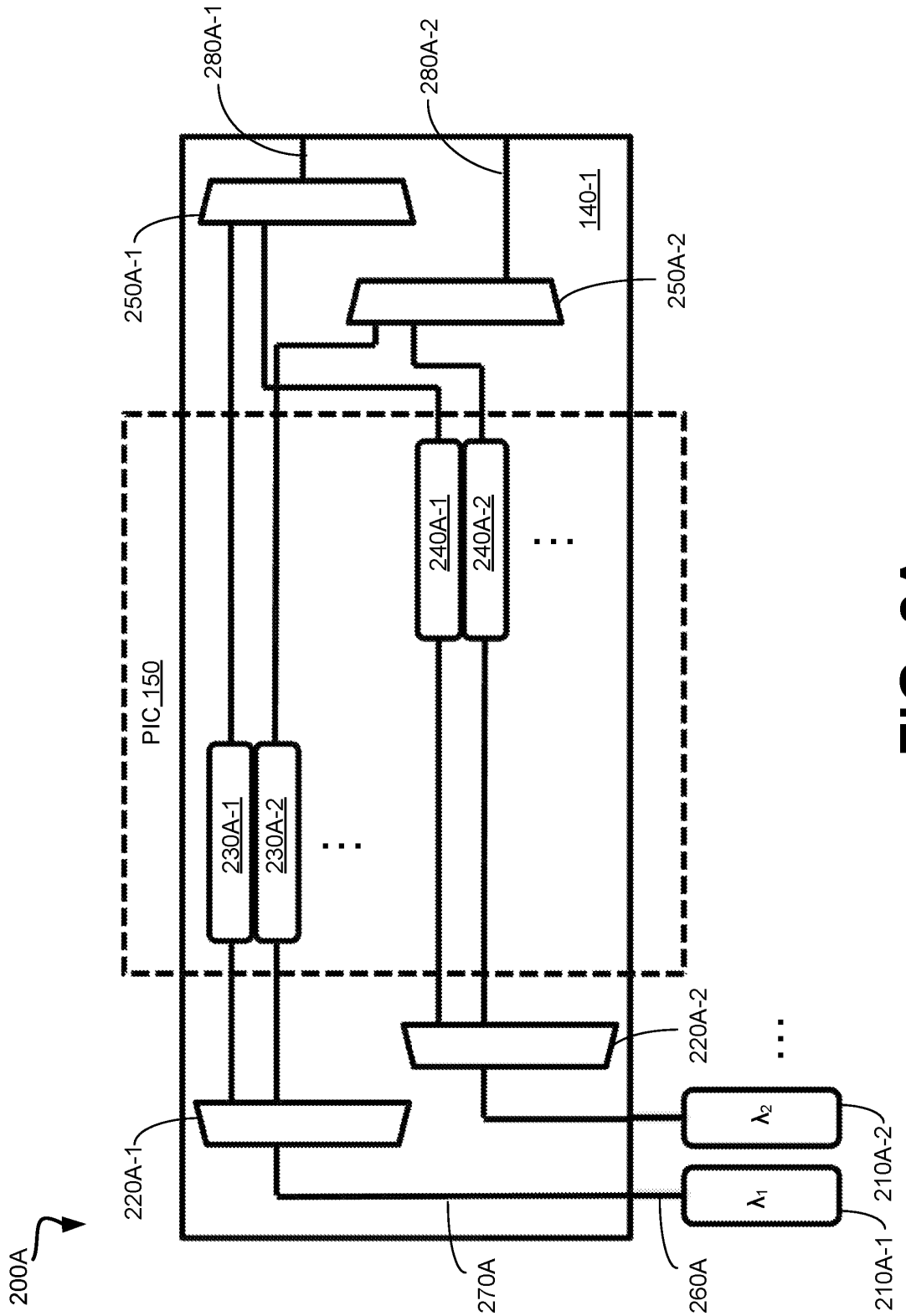
200A
280A-1
280A-2
250A-1
250A-2
140-1
PIC 150
230A-1
230A-2
240A-1
240A-2
220A-1
220A-2
λ_2
λ_1
210A-2
210A-1
270A
260A

FIG. 2A

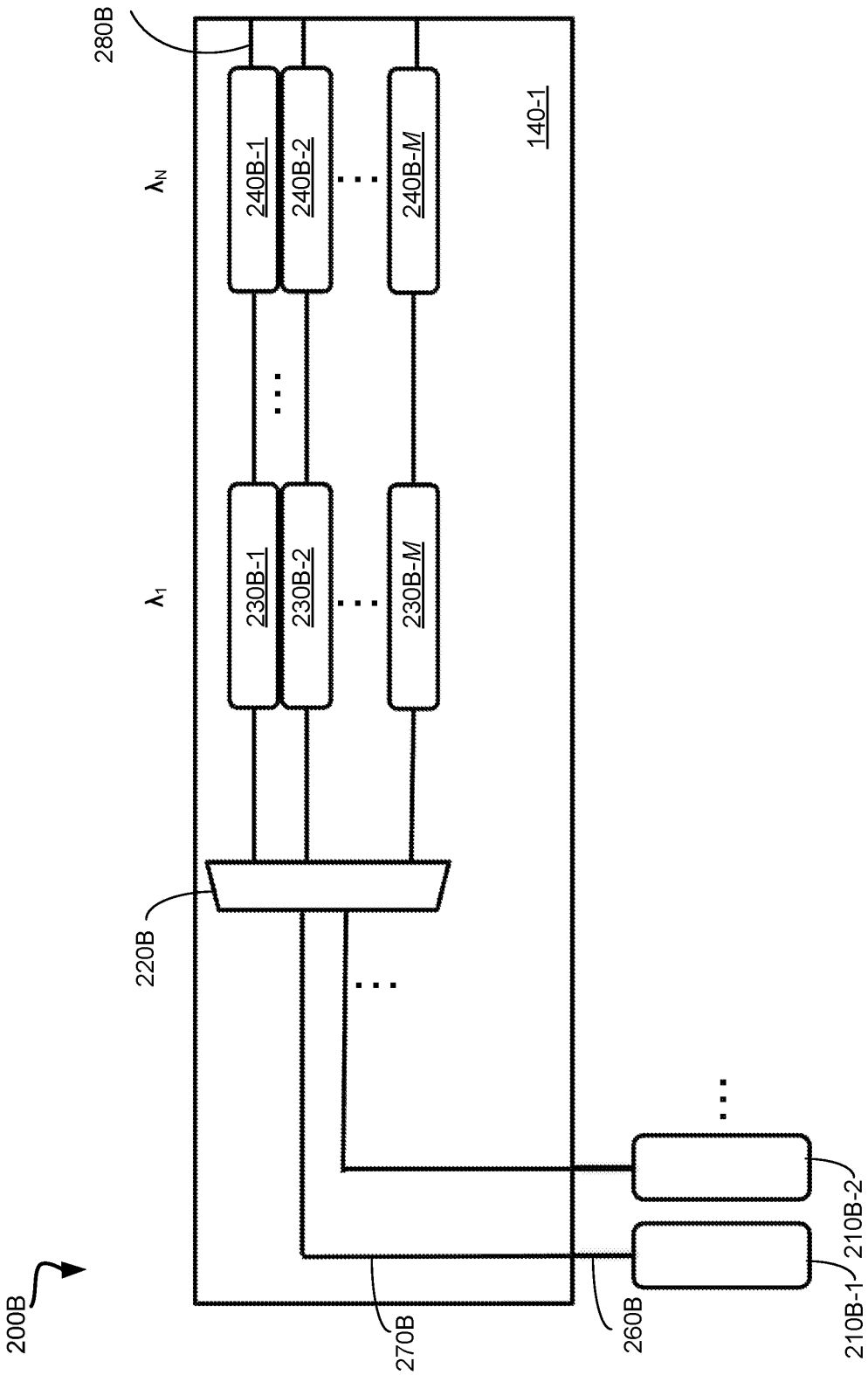
200B
280B
λ_N
λ_1
240B-1
240B-2
240B-M
230B-1
230B-2
230B-M
140-1
220B
270B
260B
210B-1
210B-2

FIG. 2B

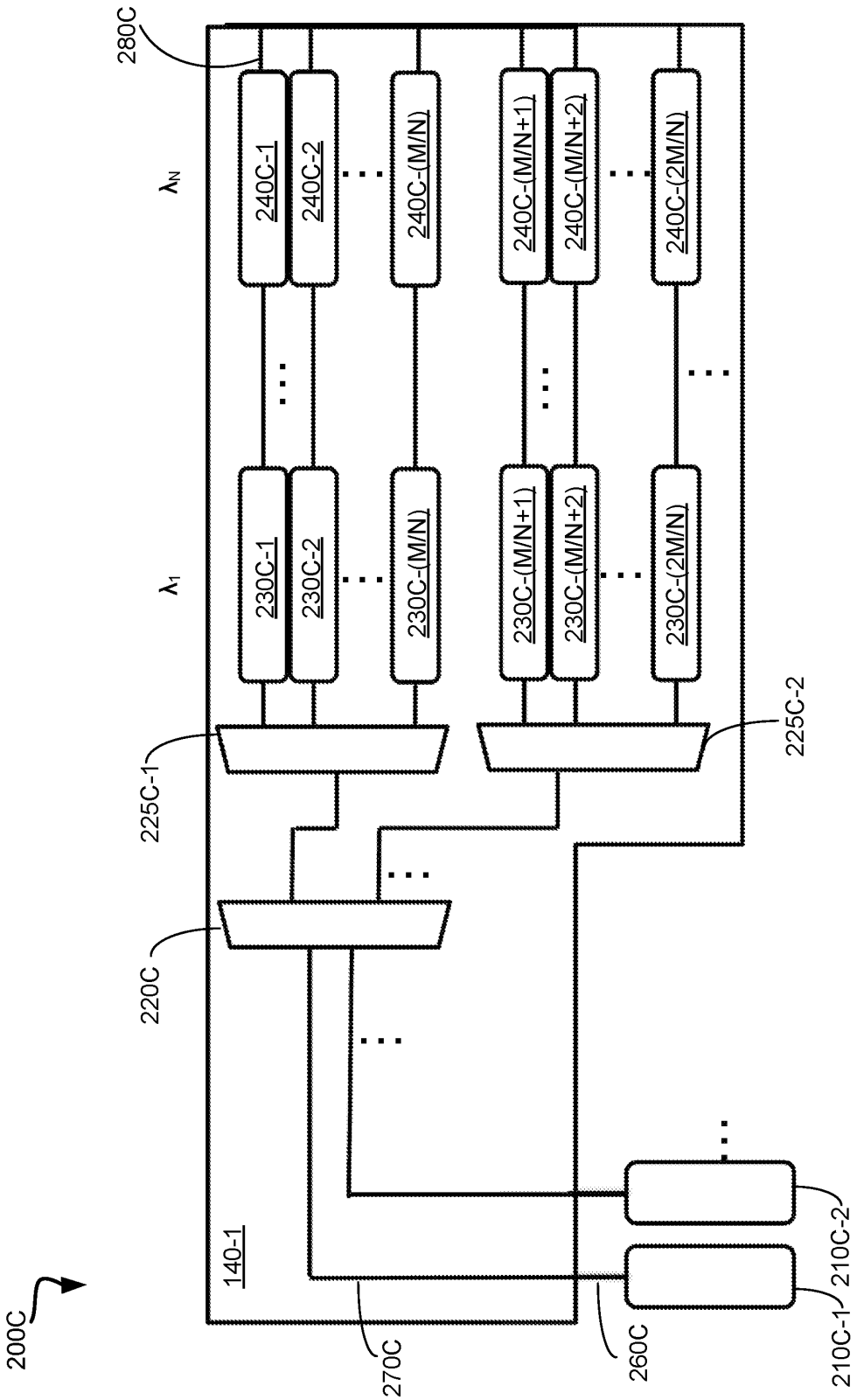
200C
140-1
280C
λ_N
λ_1
240C-1
240C-2
240C-(M/N)
240C-(M/N+1)
240C-(M/N+2)
240C-(2M/N)
230C-1
230C-2
230C-(M/N)
230C-(M/N+1)
230C-(M/N+2)
230C-(2M/N)
225C-1
225C-2
220C
270C
260C
210C-1
210C-2

FIG. 2C

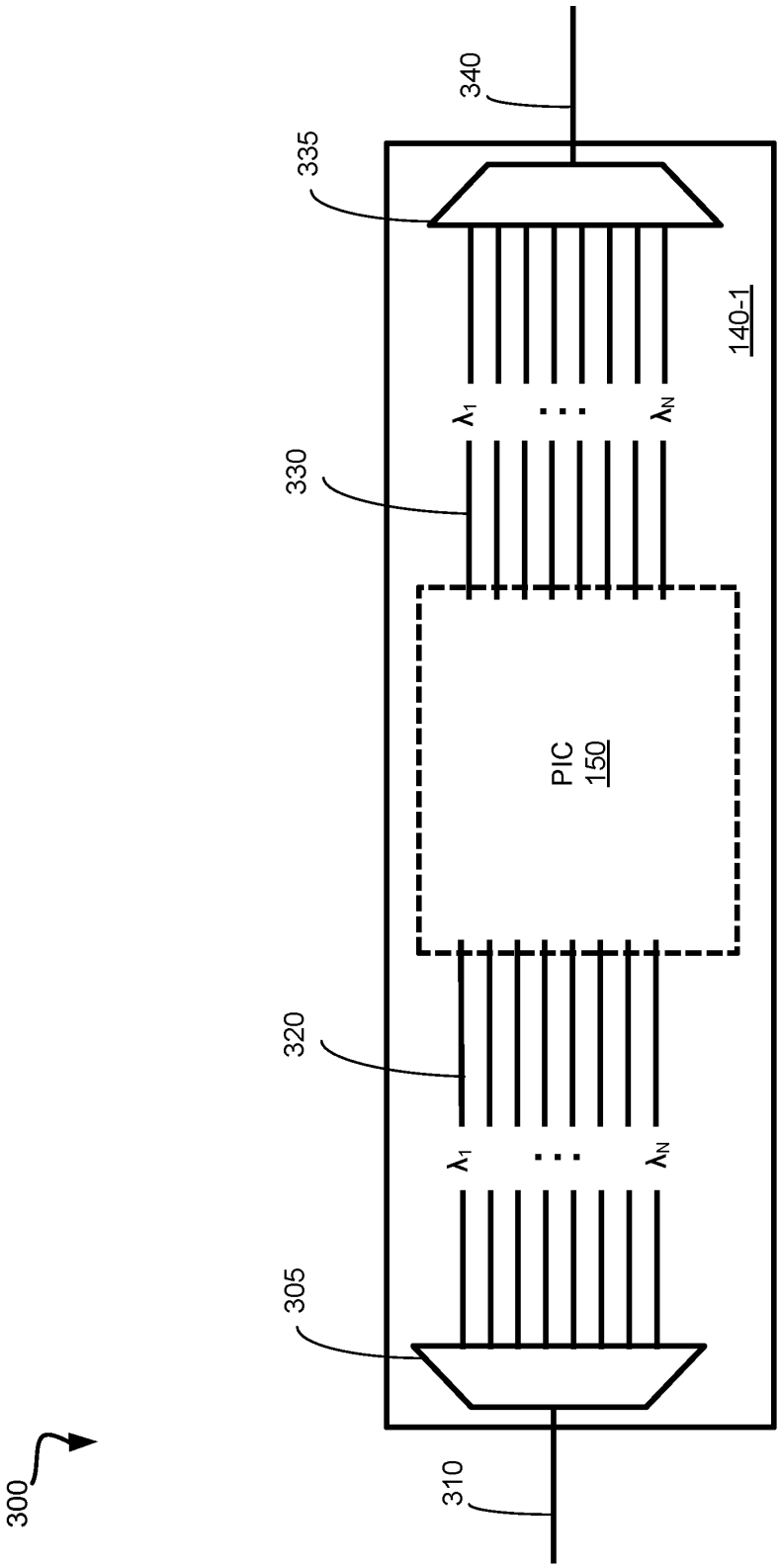
300
310
305
320
330
335
340
140-1
PIC
150
λ_1
λ_N
λ_1
λ_N

FIG. 3

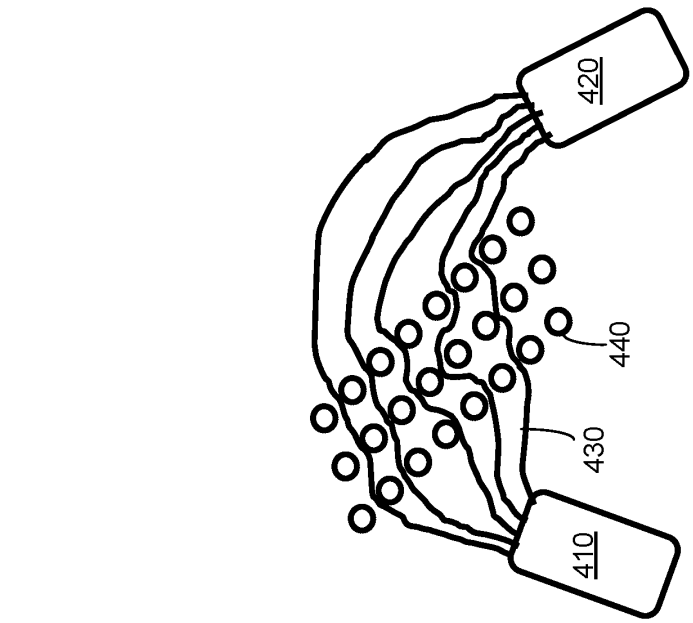
400
420
440
430
410

FIG. 4B

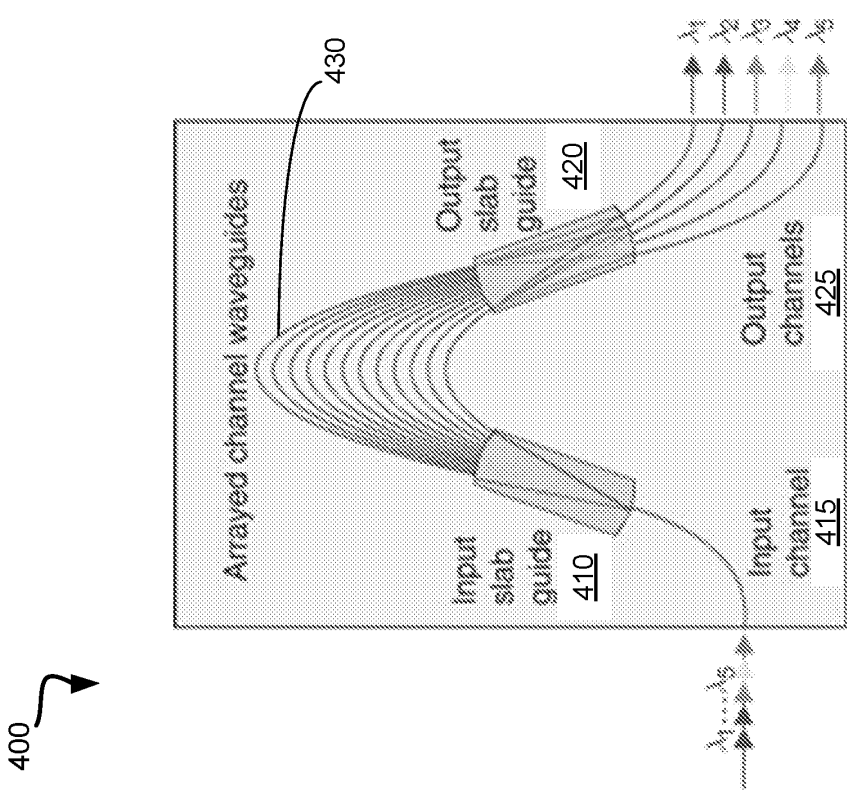
400
λ1...λ5
Input slab guide 410
Arrayed channel waveguides
430
Output slab guide 420
Input channel 415
Output channels 425
λ1
λ2
λ3
λ4
λ5

FIG. 4A

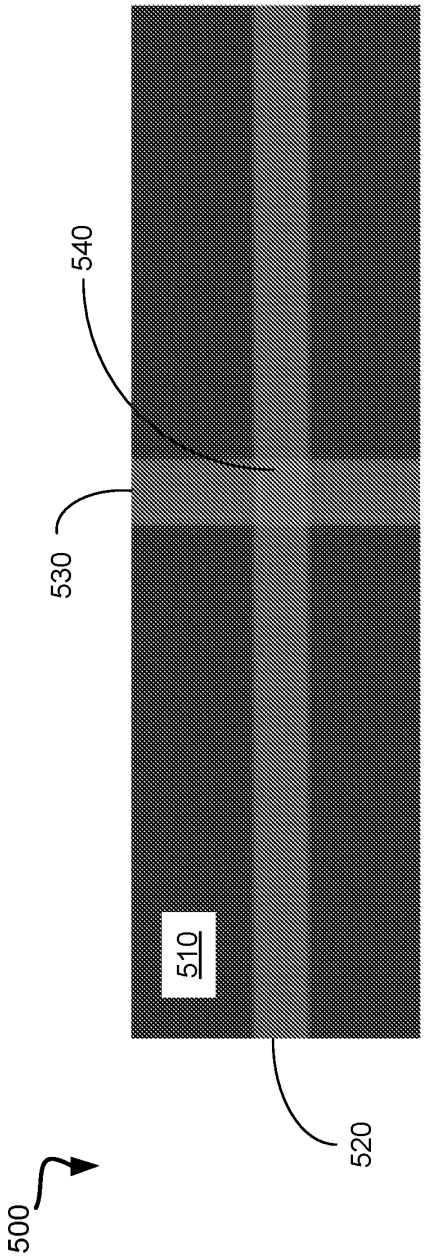

FIG. 5

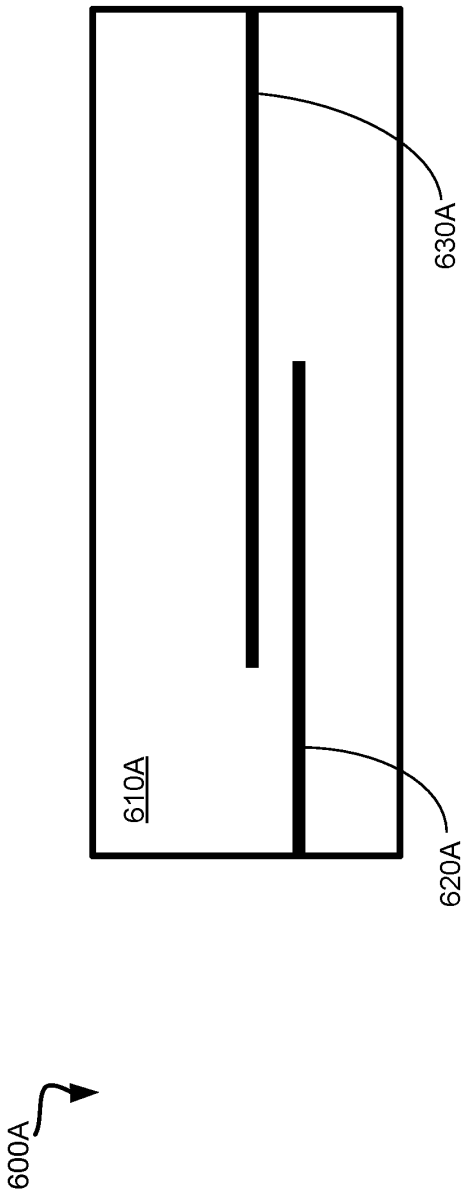

FIG. 6A

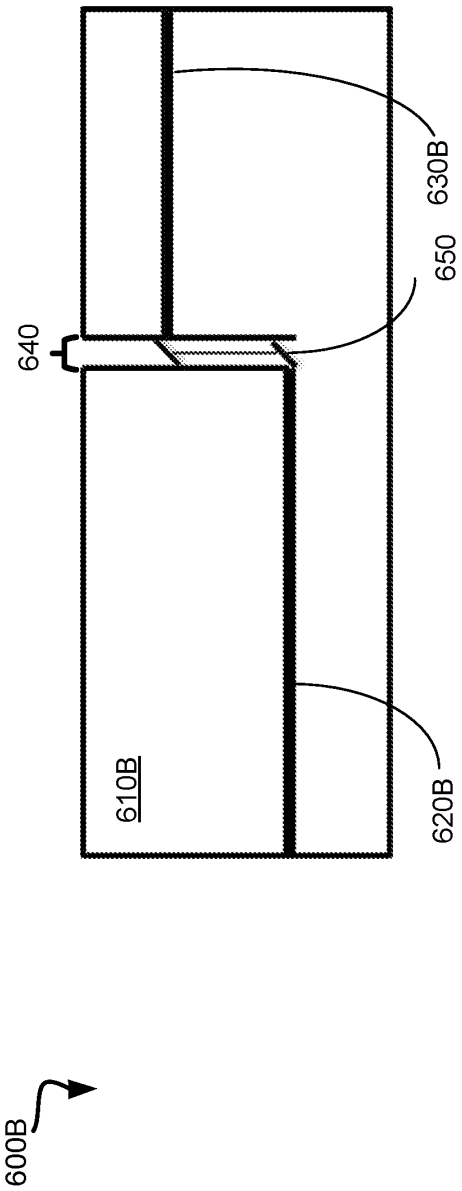

FIG. 6B

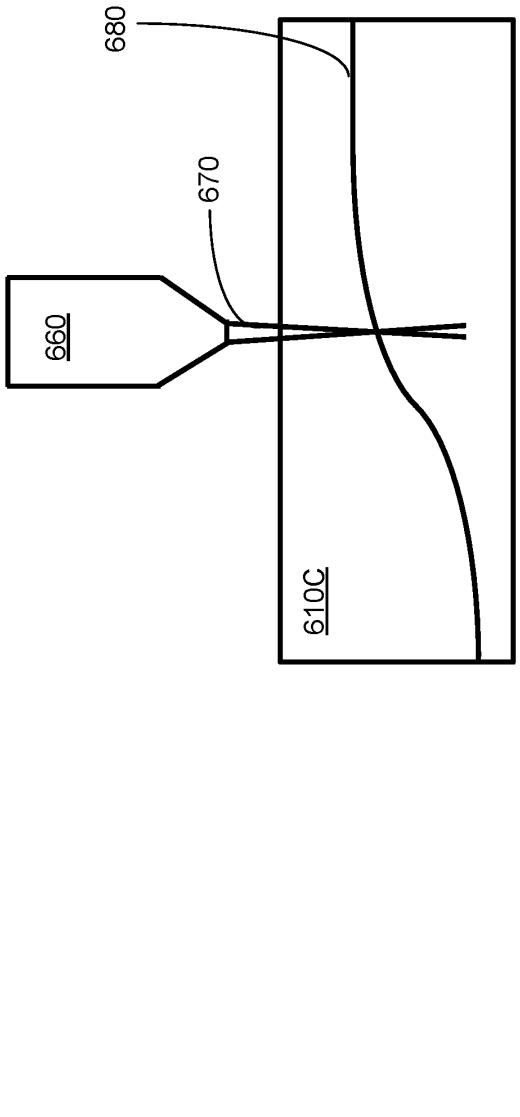

FIG. 6C

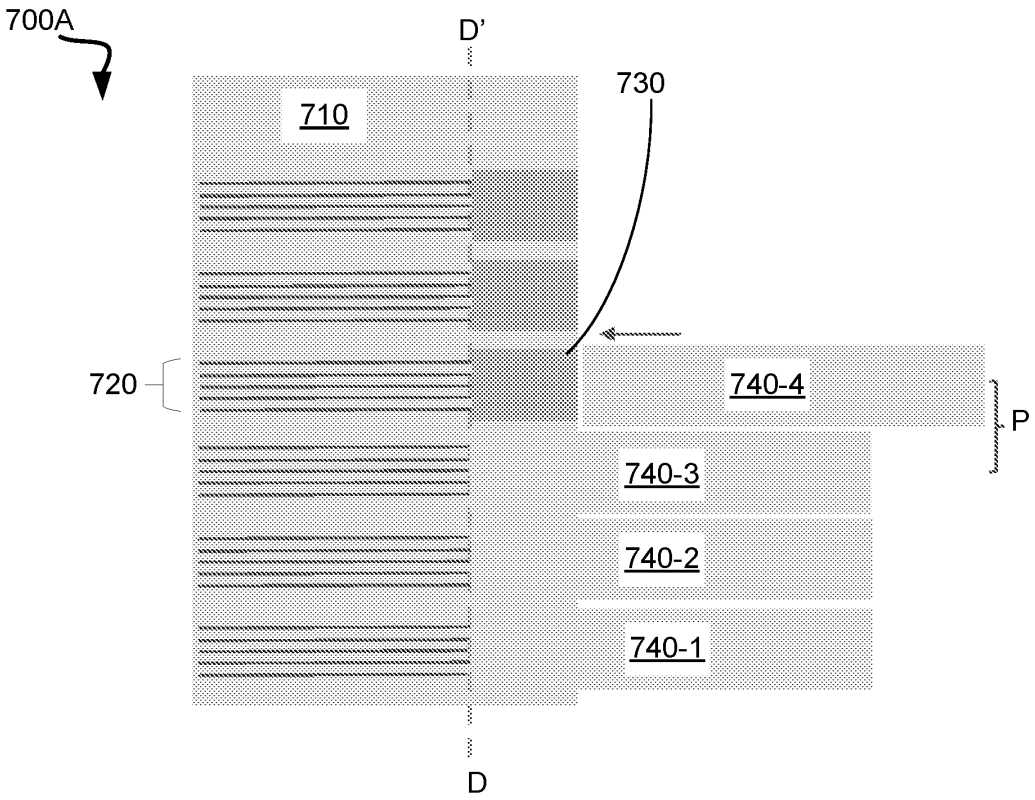
700A
D'
730
710
720
740-4
P
740-3
740-2
740-1
D

FIG. 7A

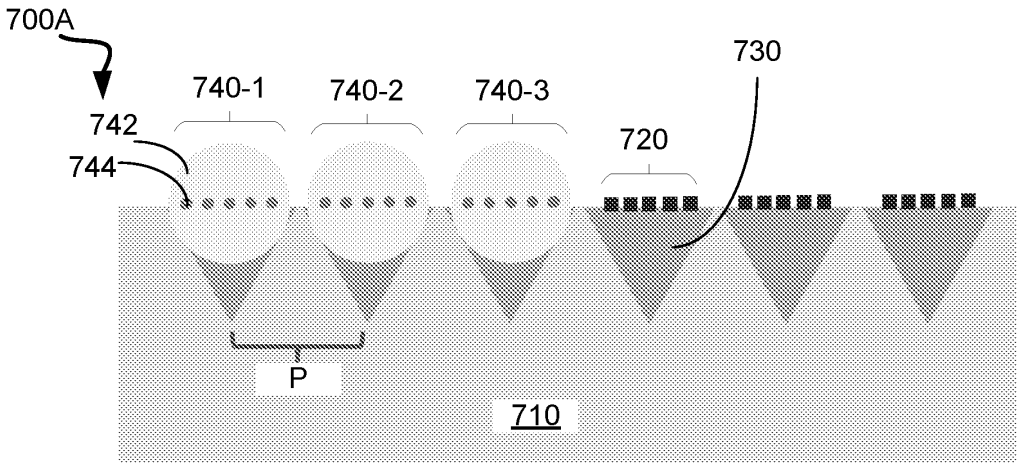
700A
730
740-1
740-2
740-3
742
744
720
P
710

FIG. 7B

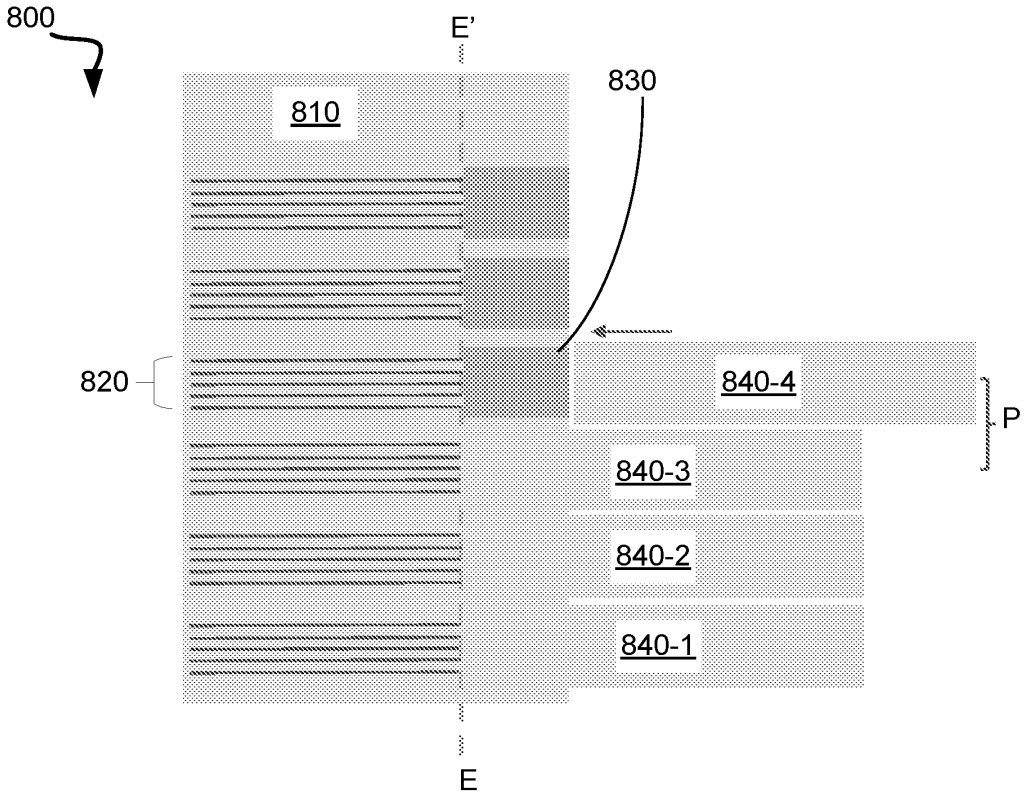
800
E'
830
810
820
840-4
P
840-3
840-2
840-1
E

FIG. 8A

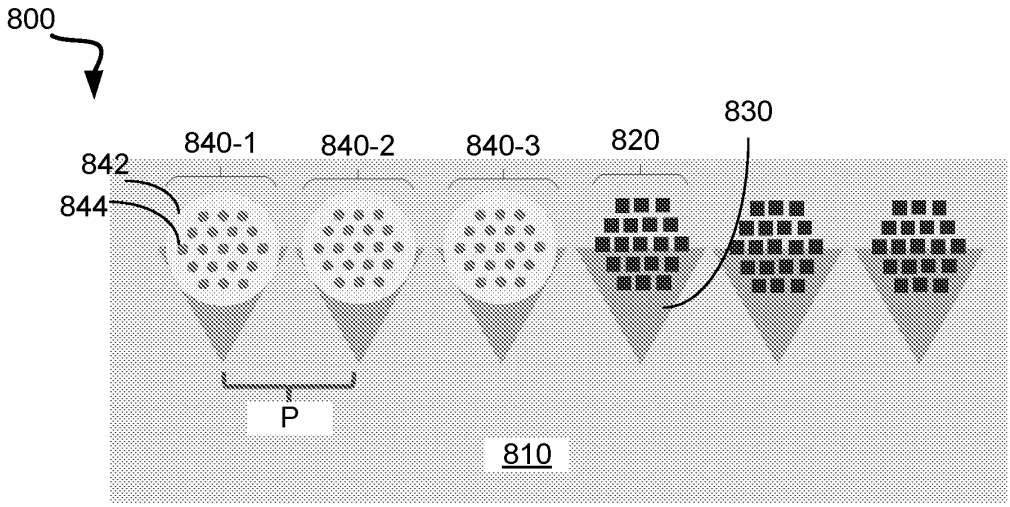
800
840-1
840-2
840-3
820
830
842
844
P
810

FIG. 8B

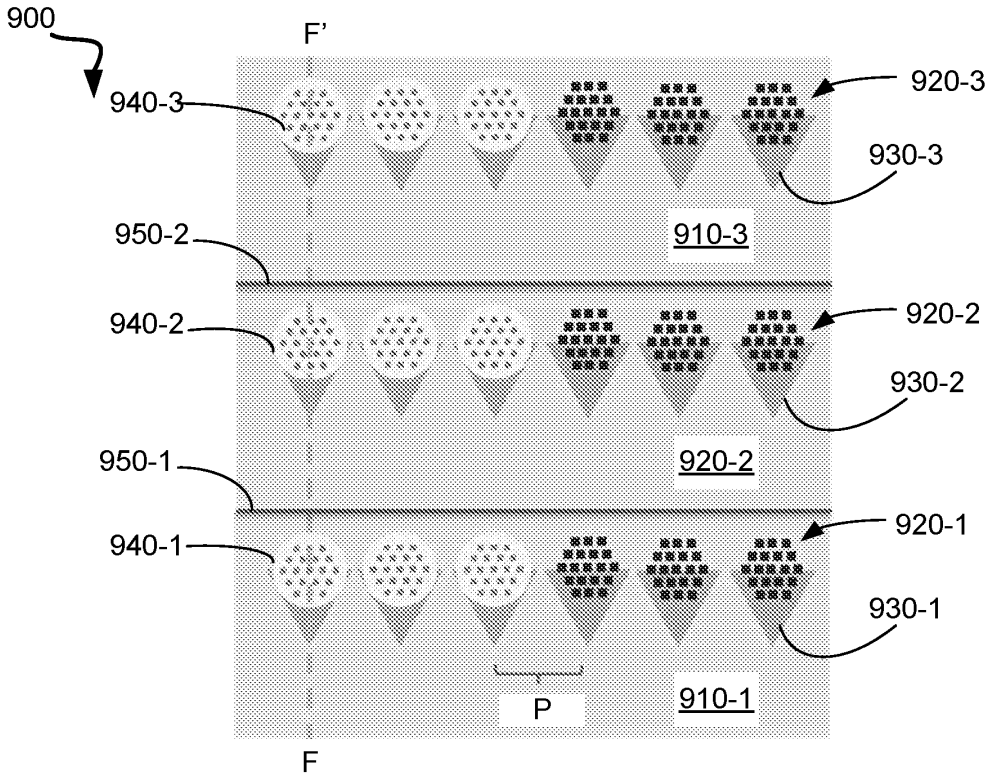
900
F'
940-3
920-3
930-3
910-3
950-2
940-2
920-2
930-2
950-1
920-1
940-1
930-1
P
910-1
F

FIG. 9A

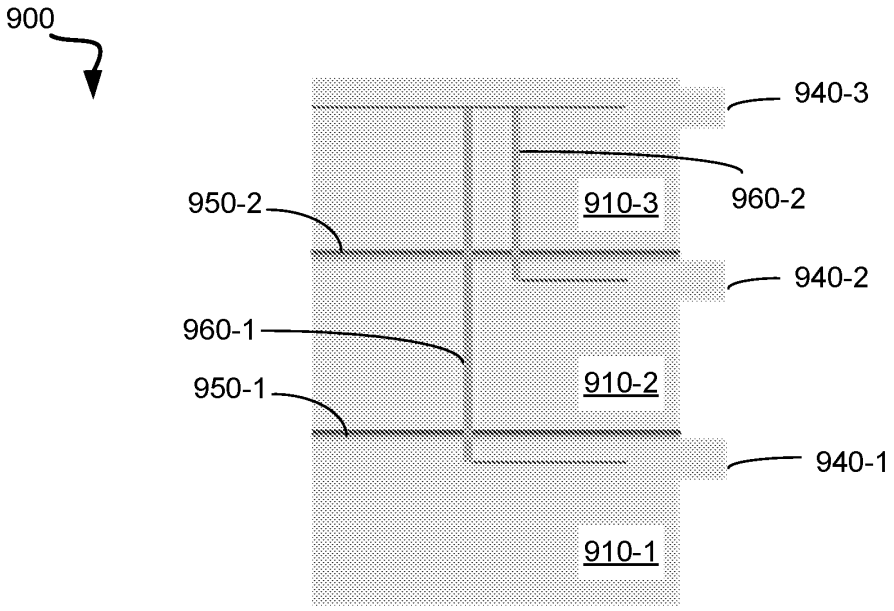
900
940-3
960-2
910-3
950-2
940-2
960-1
910-2
950-1
940-1
910-1

FIG. 9B

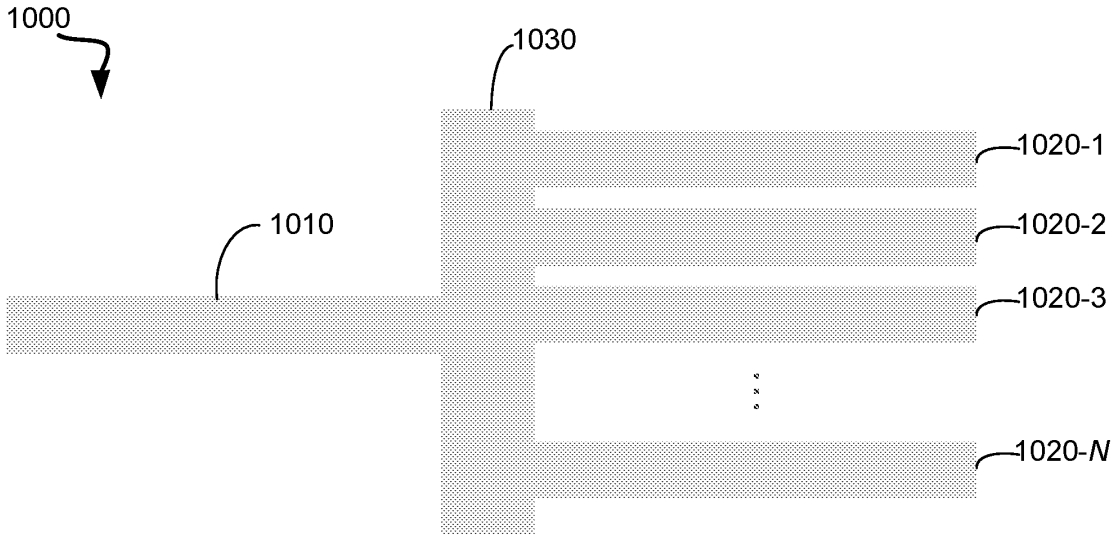

FIG. 10A

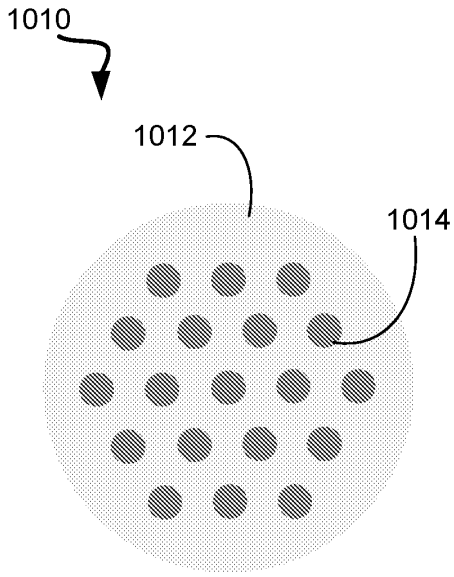

FIG. 10B

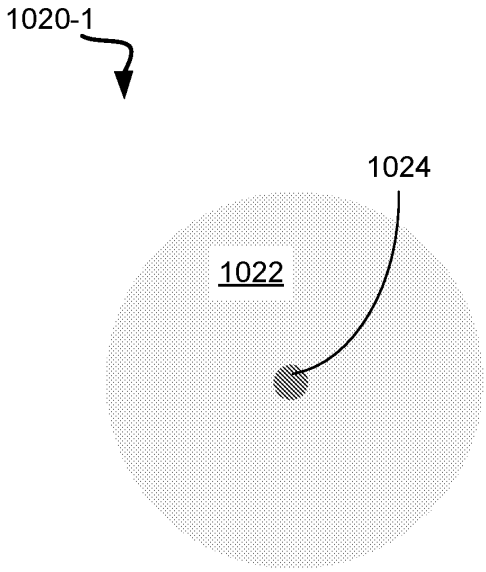

FIG. 10C

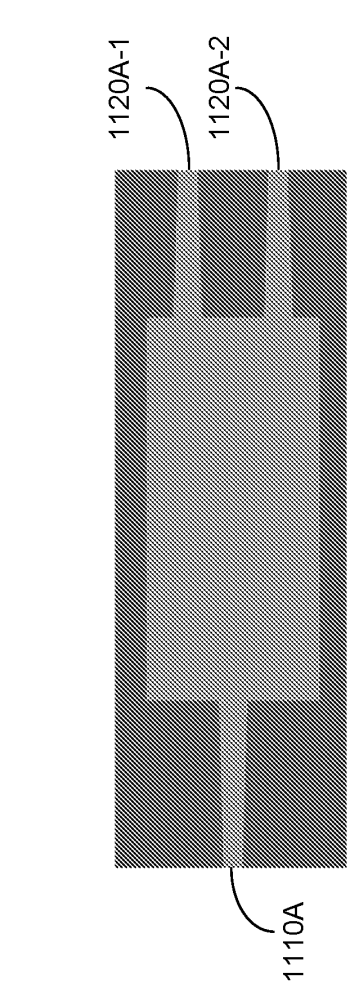

FIG. 11A

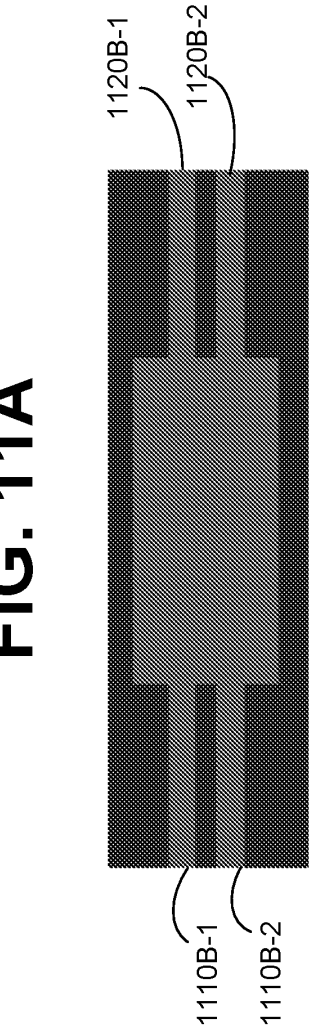

FIG. 11B

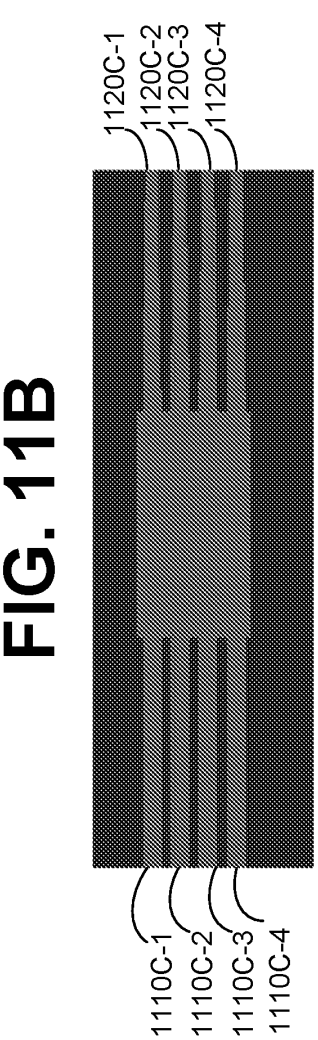

FIG. 11C

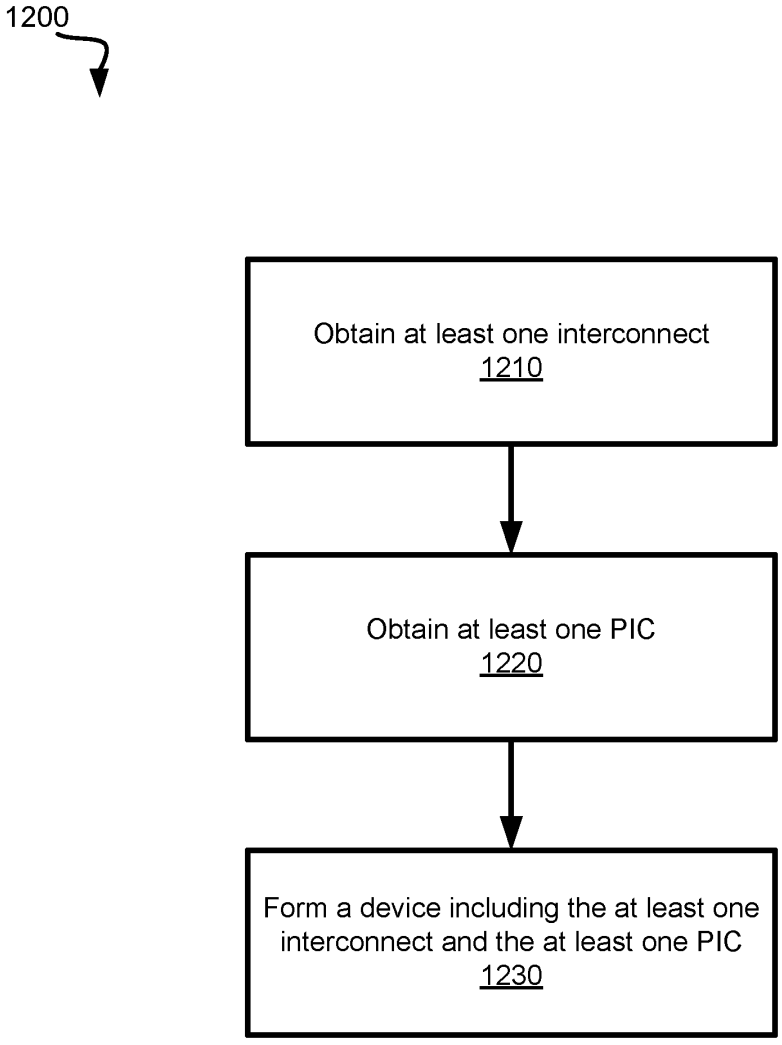
1200
Obtain at least one interconnect
1210
Obtain at least one PIC
1220
Form a device including the at least one interconnect and the at least one PIC
1230

FIG. 12