SEMICONDUCTOR DEVICE AND METHOD OF FORMATION

Field of the Invention

This invention relates in general to processes for forming semiconductor devices, and more particularly to processes for forming semiconductor devices including interconnect barrier layers.

Related Art

Forming conductive bumps over semiconductor device bond pads is becoming increasingly common as the sizes and packages of the semiconductor devices continue to shrink. The bumps are used instead of wires to electrically connect the bond pads to their respective packaging leads. One specific type of bump includes a controlled-collapse chip-connection (C4) bump. Bumps generally require that a pad limiting metal layer be formed between the bond pad and the bump. Pad limiting metal layers typically include chrome and chromium alloys. However, these chromium-containing films can have defects, such as cracks and irregular grain boundaries, which limit the ability of the chromium layer to adequately separate the bond pad and the bump materials.

The bump typically includes elements such as tin (Sn) and lead (Pb). In the event the barrier fails to keep the bond pad and the bump separated, material from the bond pad can react with the lead or tin in the bump and intermetallic alloys of these materials can be formed. If the bond pad includes a copper-containing material, a brittle intermetallic alloy can be the result. The brittle intermetallic alloy can subsequently crack and result in bump failure. In addition, voids can form as a result of the alloying process and degrade adhesion between the bond pad and the bump. In extreme cases this can produce high resistance that can negatively impact the semiconductor device's performance and even result in failure of the semiconductor device.

Brief Description of the Figures

The present invention is illustrated by way of example and not limitation in the accompanying figures, in which like references indicate similar elements, and in which:

FIGs. 1-7 include illustrations of cross-sectional views of forming a semiconductor device having copper interconnects and bumps in accordance with a first set of embodiments.

FIGs. 8-12 include illustrations of cross-sectional views of forming a semiconductor device having copper interconnects and bumps in accordance with a second set of embodiments.

Skilled artisans appreciate that elements in the figures are illustrated for simplicity and clarity and have not necessarily been drawn to scale. For example, the dimensions of some of the elements in the figures may be exaggerated relative to other elements to help to improve understanding of embodiments of the present invention.

Detailed Description

In accordance with embodiments of the present invention a semiconductor device and its method of formation are disclosed. In one embodiment, a conductive barrier layer overlies an interconnect, a passivation layer overlies the conductive barrier layer, and the passivation layer has an opening that exposes portions of the conductive barrier layer. In an alternate embodiment, a passivation layer overlies the interconnect, the passivation layer has an opening that exposes the interconnect, and a conductive barrier layer overlies the interconnect within the opening.

FIG. 1 includes an illustration of a cross-sectional view of a portion of a semiconductor device. The semiconductor device includes a semiconductor device substrate 100, field isolation regions 102, and doped regions 104 formed within the semiconductor device substrate 100. A gate dielectric layer 106 overlies portions of the semiconductor device substrate 100 and a gate electrode 108 overlies the gate dielectric layer 106.

A first interlevel dielectric layer (ILD) 110 is formed over the gate electrode 108 and the semiconductor device substrate 100. The first interlevel

dielectric layer 110 is pattered to form dual inlaid openings that are filled with a adhesion/barrier layer 112 and a copper fill material 114. The adhesion/barrier layer 112 is typically a refractory metal, a refractory metal nitride, or a combination of refractory metals or their nitrides. The copper fill material 114 is typically copper or a copper alloy, wherein the copper content is at least 90 atomic percent. The copper can be alloyed with magnesium, sulfur, carbon, or the like to improve adhesion, electromigration, or other properties of the interconnect. After depositing the adhesion/barrier layer 112 and the copper fill material 114, the substrate is polished to remove portions of the adhesion/barrier layer 112 and copper fill material 114 outside of the opening.

After forming the first interconnect level, an insulating barrier layer 122 is formed over the copper filled interconnect and first ILD layer 110. This insulating barrier layer 122 includes silicon nitride, silicon oxynitride or the like. Using an insulating material to form the insulating barrier layer 122 eliminates the need to form additional patterning and etch processes that would otherwise be required to electrically isolate the interconnects from one another if a conductive barrier would be used. A second ILD layer 124 is formed over the insulating barrier layer 122. A dual inlaid interconnect comprising a conductive adhesion/barrier layer 126 and a copper fill material 128 is formed within the second ILD 124. The dual inlaid interconnect is formed using processes and materials similar to those used to form the dual inlaid interconnect structure in the first ILD layer 110.

A passivation layer 22 is then formed over the second ILD layer 124 and the dual inlaid interconnect, as shown in FIG. 2. The passivation layer can include one or more films of silicon nitride, silicon oxynitride, silicon dioxide, or the like. Portions of the passivation layer 22 closest to the copper fill material 128 typically include silicon nitride or a silicon oxynitride film having a higher concentration of atomic nitrogen relative to atomic oxygen. The passivation layer 22 is patterned to form a bond pad opening 24 that extends through the passivation layer to the copper fill material 128.

A conductive barrier layer 32 is deposited over the passivation layer 22 and the copper fill material 128, as shown in FIG. 3. The conductive barrier layer 32 can be deposited using processes that can include chemical vapor deposition, physical vapor deposition, evaporation deposition, electroplating, electroless plating, or the like. The thickness of this layer is generally in a

range of approximately 50 to 300 nanometers (nm). Typically, the conductive barrier layer 32 includes a refractory metal, a refractory metal nitride, or a combination thereof. In one embodiment the conductive barrier layer 32 includes a combination of titanium (Ti) and titanium nitride (TiN). The titanium/titanium nitride stack improves adhesion to the underlying copper fill material 128 and passivation layer 22. Additionally, the titanium nitride forms a barrier that prevents the copper fill material from reacting with subsequently deposited conductive bumps. Alternatively, the conductive barrier layer 32 can include other materials such as tantalum (Ta), tantalum nitride (TaN), tungsten (W), titanium tungsten nitride (TiWN), titanium tungsten (TiW), tungsten nitride (WN), molybdenum nitride (MoN), cobalt nitride (CoN), or a combination of thereof. In other embodiments, oxygen tolerant materials can be used. These materials can include platinum (Pt), palladium (Pd), nickel (Ni), conductive metal oxides or their corresponding metals, or the like. The conductive metal oxides and their corresponding metals can further include iridium (Ir) and iridium oxide (IrO2); ruthenium (Ru) and ruthenium oxide (RuO2); rhenium (Re) and rhenium oxide (ReO2 and Re03) or osmium (Os) and osmium oxide (OsO2)

A resist layer 34 is then formed over the conductive barrier layer 32. The resist layer 34 exposes portions of the conductive barrier layer 32 overlying the passivation layer 22. The resist is formed such that it covers the bond pad opening 34. In addition, it can also be patterned to extend slightly over surface portions of the conductive barrier layer 32 lying above passivation layer 22, as shown in FIG. 3.

The conductive barrier layer 32 is then etched, using conventional etching processes, to remove the exposed portions of the conductive barrier layer 32 overlying passivation layer 22. After the etch, the patterned resist layer 34 is removed using a plasma ashing process or, alternatively, using a wet chemical process that uses organic chemicals, such as N-methyl-2-pyrrolidone, acetone, methyl isobutyl ketone (MIBK) or the like.

Alternatively, if a plating process such as electroplating or electroless plating is used to form the conductive barrier layer, the previously described patterning process may not be necessary. Instead, the conductive barrier layer can be plated directly over the exposed portions of the copper fill material 128 after forming opening 24. If so desired, plating can proceed to the extent

where the plated material overlies a portion of the passivation layer to form the conductive barrier layer 32, as shown in FIG. 4.

A die coat layer 52 is then formed over the semiconductor device and patterned to form a die coat opening 54 overlying the bond pad opening 24, as shown in FIG. 5. In this specific embodiment, the peripheral portion of the conductive barrier layer 32 have edges that are exposed within the die coat opening 54. The die coat layer 52 can be formed as a photo-imagable polyimide film or, alternatively, as a polyimide film that is patterned using conventional resist and etch processing.

Prior to forming a pad limiting metal layer 62, as shown in FIG. 6, exposed portions of the conductive barrier layer 32 are processed through a radio frequency (RF) sputter clean. The RF sputter clean improves contact resistance between the barrier layer and the pad limiting metal layer 62 by removing uppermost portions of the conductive barrier layer 32 that can contain impurities, such as oxygen, carbon, fluorine, and chlorine. In one embodiment, the RF sputter clean process is performed as part of an in-situ process prior to depositing the pad limiting metal (underbump) layer. In one embodiment, the processing parameters for performing the RF sputter clean are as follows: RF power is in a range of approximately 1200 to 1500 Watts (W), direct current (DC) bias voltage is in a range of approximately -300 to -600 volts (V), pressure is in a range of approximately 0.1 to 0.5 Pascals, and time is in a range of approximately 150 to 250 seconds. The RF sputter clean process removes approximately 20-40 nm of barrier material from the surface of the barrier layer 32.

The pad limiting metal layer 62 is then formed within the die coat opening 54 as illustrated in FIG. 6. A Pad limiting metal layer typically includes a functional combination of films that can include an adhesion film, an intermediate coupling/solderable film and an antioxidation barrier film. In one embodiment, the pad limiting metal layer 62 includes a composite of four different films: a chromium film 622, a chromium-copper alloy film 624, a copper film 626, and a gold film 628. The chromium film 622 and the chromium-copper alloy film 624 each have a thickness in a range of approximately 50 to 500 nm, the copper film 626 has a thickness in a range of approximately 700 to 1300 nm, and the gold film 628 has a thickness in a range of 80 to 140 nm. Alternatively, the pad limiting metal can include other

combinations of films such as a composite of titanium, copper and gold or a composite of titanium, nickel, copper and gold. The pad limiting metal layer 62 is typically formed by evaporation using a shadow mask. However, other methods, such as sputtering can alternatively be used to form the pad limiting metal.

In accordance with one embodiment, following the formation of pad limiting metal layer, a bump material, such as a lead tin solder material 72 is deposited over the pad limiting metal layer 62 as shown in FIG. 7. The lead tin solder material 72 can be evaporated using a shadow mask or, alternatively, it can be formed using other conventional methods, such as plating or solderjetting. A reflow processing step is then performed to round the corners of the lead tin solder material 72 and form the bump as shown in FIG. 7.

At this point in the process, a substantially completed semiconductor device has been made. This device can subsequently be attached to a packaging substrate such as a flip chip or ball grid array package. Although not shown, other levels of interconnects can be formed as needed. Similarly, other interconnects can also be made to the gate electrode 108 and the doped region 104. If additional interconnects would be formed, they would be formed using processes similar to those used to form and deposit insulator barrier layer 122, second ILD layer 124, adhesion/barrier layer 126, and copper fill material 128.

FIGs. 8-12 illustrate an alternative embodiment of the present invention. Referring to FIG. 8, a conductive barrier layer 82 is formed over the second ILD layer 124 and copper fill material 128. The conductive barrier layer 82 is formed by any of the methods or materials described in forming the conductive barrier layer 32 as first shown in FIG. 3. The thickness of the conductive barrier layer 82 is typically in a range of approximately 50 to 300 nm. In this particular embodiment, an optional oxidation-resistant layer 84 is then formed over the conductive barrier layer 82. The oxidation-resistant layer can include any material that either prevents oxidation of the underlying layer or is more readily oxidized in preference to the underlying layer. Examples of materials that can be used include silicon nitride, polysilicon, amorphous silicon, or a conductive metal oxide or its corresponding conductive metal. The oxidation-resistant layer 84 has a thickness in a range of approximately 10-50 nm. A resist layer 86 is then formed over the conductive barrier layer 82 and the

oxidation-resistant layer 84. The resist layer 86 is patterned to cover portions of the conductive barrier layer 82 and the oxidation-resistant layer 84 overlying the copper fill material 128 and the adhesion/barrier layer 126.

The unpatterned portions of conductive barrier layer 82 and oxidation-resistant layer 84 are then removed using conventional etching processes. The resist is then removed, and a passivation layer 92 is formed over the stack comprising conductive barrier layer 82 and oxidation-resistant layer 84, and portions of the dielectric layer 124 as shown in FIG. 9. The passivation layer 92 is similar to the passivation layer 22, first introduced in FIG. 2. In this particular embodiment, the passivation layer 92 is patterned to form a bond pad opening 94. As illustrated in FIG. 9, not all of the passivation layer within the bond pad opening is removed. Therefore, the bond pad opening is only partially formed during the patterning process. A residual portion 96 is left to remain over the oxidation-resistant layer 84 after patterning in complete.

A die coat layer 1001 is then formed and patterned to form a die coat opening 1003, as shown in FIG. 10. The die coat layer 1001 is similar to the die coat 52, as first introduced in FIG. 5. The die coat opening 1003 exposes portions of the passivation layer 92, including the residual portion 96. After forming the die coat opening 1003, an etch is performed to remove the residual portion 96 and the underlying oxidation-resistant layer 84. This forms the die coat opening 1103, as shown in FIG. 11. During this etch, portions of the passivation layer 92 exposed by the die coat layer 1001 are also etched, as indicated by the removed passivation layer portions 1102. In one particular embodiment, the passivation layer 92 includes silicon and nitrogen, such as silicon nitride or silicon oxynitride, and the oxidation-resistant layer 84 includes silicon nitride. Therefore, the same or similar etch chemistries can be used to remove the residual portions 96 of the passivation layer 92 and the oxidation-resistant layer 84.

Processing is continued to form a substantially completed device as shown in FIG. 12. A pad limiting metal layer 1220 is formed similar to the one previously described and includes the chromium film 1222, the chromium-copper alloy film 1224, copper film 1226, and gold film 1228, and the lead tin solder 1230. If necessary, an RF sputter cleaning process, similar to that described previously, can be used to prepare the surface of the barrier layer prior to forming the pad limiting metal layer 1220. In this particular

embodiment, a reflow step is performed to round the shape of the lead tin solder, giving it a dome-like appearance, as shown in FIG. 12.

In the embodiments described in FIGs. 9-12, the insulating barrier layer 122 is used for all interconnect levels except for the uppermost interconnect level. The uppermost interconnect level is the interconnect level over which the bond pads are formed. Therefore, it is the only interconnect level that uses the conductive barrier layer 82.

There are many other embodiments that are possible with the present invention. Turning to FIG. 3, the conductive barrier layer 32 can also include an overlying oxidation-resistant layer similar to the oxidation-resistant layer 84 described in the second set of embodiments in FIGs. 8-12. Similarly, the second set of embodiments do not necessarily require the use of the oxidation-resistant layer 84 because the residual portion 96 of the passivation layer 92 allows an oxygen-containing plasma to be used without damaging the conductive barrier layer 82. This can be important when the conductive barrier layers 82 or 32 include tantalum nitride, titanium nitride, or the like, which can adversely react with oxygen-containing plasmas or other chemicals used to remove or develop resist or polyimide. Examples of these chemicals can include tetramethyl ammonium hydroxide, N-methyl-2-pyrrolidone, acetone, MIBK, and the like.

In addition to forming the conductive barrier layer over the bond pad as described in FIGs. 9-12, the conductive barrier material can also be used to form focused energy-alterable, or laser-alterable, connections between conductive regions of the semiconductor device. The conductivity of these connections can be modified, using the laser, to program or adjust the circuitry of the device.

Forming the laser-alterable connections using the conductive barrier layer has advantages over the prior art. The conductive barrier layer is typically much thinner, less thermally conductive, and less reflective than the interconnect layer, which is normally used to form the laser-alterable connection. The conductive barrier layer is also self-passivating as compared to the interconnect layer. Therefore, reliability of the laser alteration is generally improved because the potential for shorting after laser alteration is reduced. In addition the laser-alterable connection is formed closer to uppermost surface of the semiconductor device. This allows the laser to use

less power to affect the conductivity of the laser-alterable connection, which correspondingly reduces the potential of causing shorts, damaging adjacent connections, and damaging the surrounding passivation layer. Furthermore, the conductive barrier layer and the laser-alterable connections can be formed simultaneously using the same layer. Therefore, the process integration requires no additional processing steps.

Although specific materials were listed with respect to the pad limiting metal layer 62, other materials and other variations of this integration scheme can alternatively be used. For example, the conductive barrier layer can be incorporated as part of the pad limiting metal layer. In this case, it can be evaporated or sputtered onto the wafer before forming the other respective pad limiting metal layer films. In yet another embodiment, the pad limiting metal layer and the solder material can collectively be formed by physical vapor deposition or by jet printing, whereby individual molten solder drops are deposited into place by an orifice.

The embodiments described herein can be integrated into an existing process flow without a need to use exotic materials, develop new processes, or purchase new processing equipment. The conductive barrier layers 32 and 82 are sufficient to prevent the copper from the interconnect and the lead tin solder from the bump from reacting with each other. Therefore, integrity is maintained at the interface between the bump and the interconnect. This improves the mechanical integrity of the bump as well as helps to reduce the electrical resistance between the bump and the interconnect.

In the foregoing specification, the invention has been described with reference to specific embodiments. However, one of ordinary skill in the art appreciates that various modifications and changes can be made without departing from the scope of the present invention as set forth in the claims below. Accordingly, the specification and figures are to be regarded in an illustrative rather than a restrictive sense, and all such modifications are intended to be included within the scope of present invention. Benefits, other advantages, and solutions to problems have been described with regard to specific embodiments. However, the benefits, advantages, solutions to problems, and any element(s) that may cause any benefit, advantage, or solution to occur or become more pronounced are not to be construed as a critical, required, or essential feature or element of any or all the claims.

SEMICONDUCTOR DEVICE AND METHOD OF FORMATION

CLAIMS

What is claimed is:

1. A semiconductor device, comprising:
   a first interconnect that overlies a semiconductor device substrate;
   a insulating barrier layer that overlies the first interconnect;
   a bond pad interconnect that overlies portions of the first interconnect and the insulating barrier layer;
   a conductive barrier layer that overlies a portion the bond pad interconnect, the conductive barrier layer extending beyond an edge region of the portion of the bond pad interconnect; and
   a passivation layer that overlies the conductive barrier layer, the passivation layer having an opening that exposes portions of the conductive barrier layer.

2. The semiconductor device of claim 1, further comprising an oxidation-resistant layer that overlies the conductive barrier layer.

3. The semiconductor device of claim 1, wherein a portion of the conductive barrier layer is a laser-alterable connection between at least two conductive regions.

4. A semiconductor device, comprising:
   a bond pad interconnect over a semiconductor device substrate;
   a passivation layer that overlies the bond pad interconnect (128), the passivation layer having an opening that exposes a portion of the bond pad interconnect; and
   a conductive barrier layer within the opening that overlies the portion of the bond pad interconnect.

5. The semiconductor device of claim 1 or 4, wherein the bond pad interconnect includes mostly copper and the conductive barrier layer includes a refractory metal containing material.

6. A method of forming a semiconductor device comprising:
forming a first interconnect overlying a semiconductor device substrate;
forming an insulating barrier layer overlying the first interconnect;
forming a bond pad interconnect overlying portions of the first interconnect and the insulating barrier layer;
forming a conductive barrier layer overlying a portion of the bond pad interconnect, the conductive barrier layer extending beyond an edge region of the portion of the bond pad interconnect;
forming a passivation layer overlying the conductive barrier layer; and
forming an opening in the passivation layer, wherein the opening exposes portions of the conductive barrier layer.

7. The method of claim 6, wherein forming an opening in the passivation layer further comprises:
forming a partial opening in the passivation layer, wherein a depth of the partial opening is less than a thickness of the passivation layer in a region of the passivation layer where the partial opening is formed;
forming a die coat layer over the passivation layer;
forming an opening in the die coat layer, wherein forming the opening in the die coat layer exposes the partial opening in the passivation layer; and
etching the partial opening in the passivation layer to expose an underlying layer after forming an opening in the die coat layer.

8. The method of claim 6, further comprising:
removing a portion of the conductive barrier layer after forming an opening in the passivation layer, wherein the portion of the conductive barrier layer has a depth; and
forming a conductive bump over the conductive barrier layer after removing a portion of the conductive barrier layer.

9. A method of forming a semiconductor device, comprising:
forming an interconnect over a semiconductor device substrate;
forming a passivation layer over the interconnect;
forming an opening in the passivation layer, the opening exposing portions of the interconnect; and
forming a conductive barrier layer within the opening, the conductive barrier layer overlying exposed portions of the interconnect.

10. The method of claims 6 or 9, wherein the bond pad interconnect includes mostly copper and the conductive barrier layer includes a refractory metal containing material.