

WHAT IS CLAIMED IS:

1. A three-dimensional semiconductor device comprising:
 - a substrate having a cell array region and a contact region;
 - a stacked structure comprising a plurality of electrodes and a plurality of electrode isolation insulating layers, which are alternately stacked on the substrate in a vertical direction, and having a stepwise structure on the contact region;
 - vertical structures penetrating the stacked structure in the cell array region, each of the vertical structures constituting a cell string; and
 - contact plugs in the contact region,wherein for each pair of immediately neighboring electrodes of the plurality of electrodes including an upper electrode and a lower electrode below the upper electrode, a corresponding one of the contact plugs contacts the lower electrode and penetrates and is electrically insulated from the upper electrode,
 - wherein for the each pair of immediately neighboring electrodes, the upper electrode comprises a tread portion corresponding to a portion of the upper electrode that is not overlapped by overlying ones of the plurality of electrodes, and
 - wherein each of the contact plugs penetrates the tread portion of a corresponding upper electrode.
2. The three-dimensional semiconductor device according to claim 1, further comprising:
 - insulating barrier layers between each of the contact plugs and the upper electrode penetrated thereby, the insulating barrier layers at least partially surrounding side surfaces of respective ones of the contact plugs.
3. The three-dimensional semiconductor device according to claim 2, wherein each contact plug has a plug protrusion extending in a horizontal direction into a corresponding insulating barrier layer of the insulating barrier layers.
4. The three-dimensional semiconductor device according to claim 2 or claim 3, wherein upper and lower surfaces of each insulating barrier layer contact respective electrode isolation insulating layers.

5. The three-dimensional semiconductor device according to any one of claims 1 to 4, further comprising:

contact spacers respectively surrounding side surfaces of the contact plugs.

6. The three-dimensional semiconductor device according to claim 5, further comprising:

insulating barrier layers, each insulating barrier layer being provided between a corresponding contact plug and the corresponding upper electrode penetrated thereby.

7. The three-dimensional semiconductor device according to claim 6, wherein the contact spacers and the insulating barrier layers are formed of the same material.

8. The three-dimensional semiconductor device according to any one of claims 1 to 7, further comprising:

a bit line landing plug on each vertical structure;

a dummy landing plug on an uppermost electrode of the plurality of electrodes comprised in the stacked structure; and

a contact landing plug on each contact plug.

9. The three-dimensional semiconductor device according to claim 8,

wherein the bit line landing plug, the dummy landing plug, and the contact landing plug are formed of the same material, and

wherein top surfaces of the bit line landing plug, the dummy landing plug, and the contact landing plug are on the same plane.

10. The three-dimensional semiconductor device according to claim 8 or claim 9, wherein ends of two lowermost electrodes among the plurality of electrodes of the stacked structure are vertically aligned with each other in the contact region.

11. A three-dimensional semiconductor device comprising:

a substrate having a cell array region, a contact region, and a dummy contact region between the cell array region and the contact region;

a stacked structure comprising a plurality of electrodes and a plurality of electrode isolation insulating layers, which are alternately stacked on the substrate in a vertical direction, and having a stepwise structure on the contact region;

contact plugs in the contact region;

a dummy landing plug connected to an uppermost electrode of the plurality of electrodes in the dummy contact region; and

a contact landing plug connected to each of the contact plugs,

wherein for each pair of immediately neighboring electrodes of the plurality of electrodes including an upper electrode and a lower electrode below the upper electrode, a corresponding one of the contact plugs contacts the lower electrode and penetrates and is electrically insulated from the upper electrode,

wherein for the each pair of immediately neighboring electrodes, the upper electrode comprises a tread portion corresponding to a portion of the upper electrode that is not overlapped by overlying ones of the plurality of electrodes, and

wherein each of the contact plugs penetrates the tread portion of a corresponding upper electrode.

12. The three-dimensional semiconductor device according to claim 11,

wherein the dummy landing plug and the contact landing plug are formed of the same material, and

wherein the height of the dummy landing plug is greater than the height of the contact landing plug.

13. The three-dimensional semiconductor device according to claim 11 or claim 12, further comprising:

insulating barrier layers providing electrical insulation between each of the contact plugs and the corresponding upper electrode penetrated thereby, the insulating barrier layers at least partially surrounding side surfaces of respective ones of the contact plugs,

wherein each contact plug has a plug protrusion horizontally extending into a corresponding one of the insulating barrier layers.

14. The three-dimensional semiconductor device according to claim 13, wherein the plug protrusion extends from each contact plug toward the upper electrode penetrated by the contact plug.

15. The three-dimensional semiconductor device according to any one of claims 11 to 14, further comprising:

insulative contact spacers between each of the contact plugs and the upper electrode penetrated thereby, the insulative contact spacers respectively surrounding side surfaces of the contact plugs.

16. The three-dimensional semiconductor device according to claim 15, wherein top surfaces of the contact plugs and uppermost ends of the insulative contact spacers are on the same level.

17. A three-dimensional semiconductor device comprising:

a substrate having a cell array region and a contact region;

a stacked structure comprising a plurality of electrodes and a plurality of electrode isolation insulating layers, which are alternately stacked on the substrate in a vertical direction, and having a stepwise structure on the contact region, wherein ends of two lowermost electrodes among the plurality of electrodes in the contact region are vertically aligned with each other at the same position;

vertical structures penetrating the stacked structure in the cell array region, each of the vertical structures constituting a cell string comprising a plurality of select transistors; and contact plugs in the contact region,

wherein for each pair of immediately neighboring electrodes of the plurality of electrodes including an upper electrode and a lower electrode below the upper electrode, a corresponding one of the contact plugs contacts the lower electrode and penetrates and is electrically insulated from the upper electrode,

wherein for the each pair of immediately neighboring electrodes, the upper electrode comprises a tread portion corresponding to a portion of the upper electrode that is not overlapped by overlying ones of the plurality of electrodes, and

wherein each of the contact plugs penetrates the tread portion of a corresponding upper electrode.

18. The three-dimensional semiconductor device according to claim 17, further comprising a row decoder configured to simultaneously provide the same voltage to two uppermost electrodes among the plurality of electrodes of the stacked structure.

19. The three-dimensional semiconductor device according to claim 17 or claim 18, wherein each contact plug is electrically insulated from the corresponding upper electrode penetrated thereby.