Description

The invention relates to a system for recording an information signal.

The invention further relates to a record carrier and a recording device for use in the system.

In a system disclosed in US 4,473,829 the recording marks are formed by means of an optical write head, which generates a laser beam with which a recording layer of a radiation-sensitive material on the record carrier is scanned. To form recording marks the laser beam is modulated in conformity with write signals whose signal waveforms depend on the dimensions of the recording marks to be formed and the properties of the record-carrier material. The known system has the drawback that the write signals are optimized for recording on recording layers of "ablative" recording materials only, said material being removed from the recording layer under the influence of the radiation energy applied by means of the laser beam. However, when recordings are made on other types of radiation-sensitive recording layers, other write signal waveforms are desirable. As is described in the non-prepublished Netherlands Patent Application 8602718, the write signal waveforms required for making recordings on "phase-change" and "thermo-optical" materials are completely different than in the case of recording on "ablative" materials, as a result of specific thermal effects produced in the recording layer during recording. Moreover, the thermal effects for different materials of the same type also differ from each other, so that the desired write signal waveforms for different materials of the same type may also be different.

Further European Patent Application EP 0,144,436 describes a recording system for recording a binary information signal both on record carriers with a positive write polarity, on which recording marks having a higher reflectivity than the surrounding area can be made by exposure to a laser beam, and on record carriers with a negative write polarity, on which recording marks with a lower reflectivity than the surrounding area can be formed by exposure to the laser beam. The recording apparatus comprises a detector for detecting a mark on the record carrier to determine the write polarity of the relevant record carriers.

Depending on the result of the detection the information signal is applied to the write head in inverted or non-inverted form. On record carriers with positive write polarity portions of the information signal having high signal values are recorded as recording marks with a high reflectivity and on record carriers with negative write polarity portions of the information signal having low signal values are recorded as recording marks with a low reflectivity, so that for both types of record carriers substantially the same recording pattern is formed on the record carrier. In this known recording system the waveforms of the write signals for forming high-reflectivity recording marks on the record carriers with positive write polarity are identical to the write signal waveforms for forming low-reflectivity recording marks of corresponding dimensions on record carriers with negative write polarity. This means that the write signal waveform for forming a high-reflectivity recording of a specific dimension is identical to the write signal waveform for forming a low reflectivity recording mark of the same dimensions. JP-A-61/243974 discloses an inscribable and optically readable record carrier on which adjustment information is stored. This adjustment information relates to a condition for recording and reproducing, for instance, the recording laser power. The adjustment information is read and used for setting an optimum condition for recording and reproducing.

It is an object of the invention to provide a system which enables record carriers with recording layers of different types to be inscribed by means of write signal forms which are adapted to the type of recording layer and which are very suitable to record an EFM-signal.

This object is achieved by a system for recording an information signal, comprising an inscribable and optically readable record carrier, and a recording apparatus for providing the record carrier with a pattern of recording marks having modified optical properties, which pattern represents the information signal, for which purpose the recording apparatus comprises a control circuit for converting the information signal in conformity with a specific relationship into a series of consecutive write signals to form the consecutive recording marks with modified optical properties, the record carrier being provided with readable adjustment information which is indicative of the write signal waveforms required for the relevant record carrier and the recording apparatus comprising a read device for reading the adjustment information on the record carrier in a time interval prior to recording and an adjustment circuit for adjusting the write signal waveforms, in conformity with the adjustment information read, by adapting the relationship between the write signals and the information signal, characterized in that the write signals comprise trains of pulses to form recording marks comprising sequences of overlapping recording sub-marks, and in that the adjustment circuit is adapted to adjust said train of pulses.

By an appropriate choice of the pulse trains used as write signals it is possible to compensate effectively for the influence of thermal effects for all record carriers, as is described in, for example, the

aforementioned Netherlands Patent Application 86002718. The advantage of such a write signal waveform is that it can be generated simply. Moreover, the characteristics of such signal waveforms can be expressed simply in a binary code, enabling them to be stored in a memory or to be defined by means of a digital electronic circuit.

If the system is intended for recording an EFM signal in conformity with the CD-Audio or the CD-ROM standard it is advantageous to include the adjustment information in the subcode Q-channel signal of an EFM signal which is recorded in a predetermined track portion, for example a lead-in track or lead-out track by means of a preformed information structure. In the lead-in track the Q-channel signal indicates the positions where specific track portions begin, an 8-bit code "point" indicating a track number, and an address code MIN, PSEC, PFRAME) indicating the beginning or the end of the track portion specified by the track number. The number of 8-bit codes available for track numbers is smaller than the number of codes needed. Thus it becomes possible to indicate that instead of address information adjustment information has been recorded by means of a unique bit combination in said 8-bit code "point".

If the adjustment information is recorded in this way the adjustment information can also be read in a simple manner by recovering the sub code Q-channel signal from the EFM signal by means of an EFM subcode demodulator and sub-sequently extracting the adjustment information from the remainder of the Q channel signal by detection of the unique bit combination.

It is to be noted that for controlling the read-out of a recorded standard CD signal the address information in the subcode Q-channel is utilized, so that in a combined recording/read apparatus for CD signals the same EFM sub-code demodulator can be used for reading the adjustment information during recording and also for reading the address information for controlling the read process, which means that the electronic circuitry is used very efficiently.

In the system the write signals comprise trains of pulses to form recording marks comprising sequences of overlapping recording sub-marks and the adjustment circuit is adapted to adjust the trains of pulses.

An attractive embodiment of the system for recording an information signal comprising binary bit cells is characterized further in that the control circuit comprises a detection circuit for detecting series of bit cells of the same first logic value and for supplying a detection signal which is representative of the number of bit cells of the detected series and a write signal generator for generating, in response to the detection signals, the write signals in conformity with a specific relationship between the write signals and the detection signals, the adjustment information on the record carrier being representative of the relationship between the write signals and the detection signals required for the relevant record carrier, and the adjustment circuit being adapted to establish the relationship in conformity with the adjustment information read.

In this embodiment of the system the write signal is derived from the information signal in two steps, namely a first step which is independent of the type of recording material such in which the detection signal is derived and a second step which is dependent upon the type or recording material add in which the write signal waveform is established in dependence upon the detection signal. This has the advantage that the relationship between the information signal and the write signals can be adapted very simply to the recording material of the record carrier.

Another attractive embodiment of the system is characterized in that the write signal generator comprises a memory for the storage of different write signals and meals for supplying one of the stored write signals depending on the detection signal, and in that the adjustment circuit comprises a circuit for loading the memory with the write signals in conformity with the adjustment information read.

The use of the memory enables the control circuit to be adapted to deliver an optimum write signal waveform for recording marks any size.

Another suitable embodiment of the system is characterized in that the adjustment information on the record carrier comprises the write signals required for the relevant record carrier, and in that the adjustment circuit is adapted to load the memory with the write signals comprised by the adjustment information.

This embodiment has the advantage that record carriers with novel recording materials to be inscribed by means of write signal waveforms which are still unknown can readily be used in the system. This merely necessitates the storage of the desired new write signal waveforms on the record carrier with the novel recording material.

Embodiments of the invention will now be described, by way of example, with reference to Figs. 1 to 18, of which:

Fig. 1 shows a prior-art recording system,

Figs. 2 and 3 illustrate suitable relationships between the information signal and the write signals for recordings on recording materials of the "ablative" and of the "phase change" type.

Fig. 4 shows a first embodiment of the recording system in accordance with the invention,

Fig. 5 shows a record carrier for use in the recording system in accordance with the inven-

tion,

Fig. 6 shows a suitable format for the storage of the adjustment information on the record carrier,

Fig. 7 shows another embodiment of the recording system in accordance with the invention

Fig. 8 shows an example of a control circuit for use in the recording system shown in Fig. 7,

Fig. 9 illustrates the relationship between the input and output signals of the encoding circuit for use in the control circuit,

Fig. 10 shows the addresses of the write signals stored in the memory of the control circuit,

Fig. 11 shows a number of different write signals,

Fig. 12 shows how the desired write signals are arranged in a data block stored on the record carrier,

Fig. 13 shows some signals occurring in the control circuit as a function of time.

Fig. 14 shows the format of the subcode Q-channel signal of an EFM signal in accordance with a CD standard,

Fig. 15 shows an embodiment of the system in accordance with the invention, which is very suitable for recording EFM signals in conformity with a CD standard,

Fig.16 is a flow chart of a program for a microcomputer system employed in the inventive system,

Fig. 17 shows an example of the control circuit for use in the system shown in Fig. 15, and

Fig 18 shows an example of a number of write signal waveforms generated by the control circuit of Fig. 17 for different settings of the control circuit.

Fig. 1 shows a conventional system of recording an information signal Vi, as is described in for example said United States Patent Specification US 4,473,829. The system comprises a record carrier 1 provided with a radiation-sensitive recording layer 2. A drive means 5 rotates the record carrier 1 relative to a head 4 about an axis 6. The write head 4 is adapted to direct to the recording layer 2 a radiation beam 3 of sufficient energy to bring about a change in optical properties of the recording layer 2 at the location where the beam is incident on this recording layer 2. The radiation beam 3 can be modulated with write signals Vs, which are derived from the information signal Vi to be recorded by means of a control circuit 6 in accordance with a specific relationship.

Fig. 2 shows the information aignal Vi, the write signals Vs and the recording marks 10 for recording on a recording layer of an "ablative" recording material. The information signal Vi is an EFM-modulated signal, for example in conformity with the CD-Audio or CD-ROM standard. Such a signal comprises binary bit cells 11 of constant duration T. The number of successive bit cells of the same logic value is minimum three and maximum eleven in an EFM modulated signal. For the contiguous groups 12a, 12b and 12c of bit cells of the logic value "1" the control signal 6 generates write signals Vsa, Vsb and Vsc respectively. Each of the write signals comprises one or more write pulses 13. In response to every write pulse 13 the write head 4 generates a radiation pulse. As a result of each radiation pulse 13 the ablative recording material is removed at the location where the radiation beam 3 is incident on the recording layer 2, thus producing a unitary recording mark s having modified optical properties in the recording layer 2. In the example illustrated in Fig. 2 the dimension of a unitary recording mark s corresponds to said minimum length of three bit cells. The write signal Vsa for forming a recording mark 10 corresponding to the minimum number of three bit cells of a logic value "1" comprises only one write pulse 13. The recording marks 10 corresponding to a larger number of bit cells comprise a plurality of overlapping unitary recording marks s, which are formed by means of write signals comprising a sequence of write pulses 13 which are shifted relative to one another by a time interval corresponding to the bit cell length T.

Fig. 3 illustrates a suitable relationship between the information signal Vi and the write signals Vsa, Vsb and Vsc for recording on "phase-change" recording materials, as is described in, for example, the said Netherlands Patent Application 8602718 (PHN 11.915). When making a recording on such materials it is desirable, on account of thermal effects occurring within the recording layer during recording, to utilize different write signal waveforms for forming the recording marks 10, additional leader pulses 20a and 20b being generated prior to the formation of the first unitary recording mark s. It is to be noted that the position and the number of leader pulses depend on the "phase-change" recording material being used.

Fig. 4 shows a first embodiment of the recording system in accordance with the invention. The recording system comprises an optical write/read head 30 for scanning an inscribable record carrier 32 by means of a radiation beam 31, which record carrier is rotated with a substantially constant tangential velocity relative to the write/read head 30 by means of a motor 32a. The write/read head 30 is of a customary type, which can be operated in a read mode, in which the intensity of the radiation beam 31 is not high enough to bring about an optical change in the recording layer of the record carrier 32, and a write mode, in which the radiation beam is modulated in conformity with the write signals Vs and the intensity of the modulated radiation beam 31 is adequate to bring about an optical

change in the recording layer of the record carrier 32. By means of a motor 33 and a spindle 34 and the write/read head 30 can be moved in a radial direction relative to the record carrier 32. The motor 33 is energized by a motor-control circuit 41. A first control circuit 35 converts the information signal Vi into a sequence of write signals Vs′ suitable for recording on ablative recording material. Such a control circuit 35, which is adapted to ablative recording and which converts the information signal into write signals Vs in conformity with the relationship illustrated in Fig. 3, is described in detail in the aforementioned Patent Specification US 4,473,829 (PHN 10.317) which publication is incorporated herein by reference. A second control circuit 36 converts the information signal Vi into write signals Vs″ suitable for recording on "phase-change" recording materials. Such a control circuit 36, which is adapted to record on "phase-change" recording materials and which converts the information signal into write signals in conformity with the relationship illustrated in Fig. 3, is described comprehensively in said Netherlands Patent Application 8602718 (PHN 11.915), which document is incorporated herein by reference. By means of an electronically actuated switch 32b either the write signals Vs′ or the write signals Vs″ are selected for modulating the write beam 31 in the write mode. For controlling the selection of write signals the record carrier is provided with adjustment information which indicates whether the relevant record carrier 32 must be inscribed by means of write signals Vs′ or write signals Vs″. This adjustment information is prerecorded as an information structure at a predetermined location on the record carrier.

Fig. 5 shows an embodiment of the record carrier 32 on which the adjustment information has been recorded at a predetermined location. Fig. 5a is a plan view and Fig. 5b shows a small part of the sectional view taken on the line b-b. The record carrier 32 has a preformed track 37, for example a preformed groove or ridge. The track 37 comprises a portion 37b which is intended for recording the information signal. For the purpose of recording the record carrier 32 has a recording layer 96 deposited on a transparent substrate 95 and covered with a protective layer 97. The recording layer 96 is of a material which when exposed to suitable radiation is subjected to an optically detectable change. A survey of such materials is given in the book "Principles of optical disc systems", Adam Hilgar Ltd., Bristol and Boston, pages 210-227.

The reference numeral 37a indicates a lead-in track which precedes the beginning of the portion 37b intended for recording. In the present embodiment of the record carrier 32 the adjustment information is recorded as a pattern of preformed pits 98, a part 92 of the lead-in track 37a formed with such pits being shown to a strongly enlarged scale in Fig. 5c.

Fig. 5d shows the part 92 in a sectional view taken on the line d-d.

It is to be noted that for the sake of clarity the distance between the turns of the spiral track 37 has been exaggerated strongly. In a practical example of the record carrier 32 the distance between the tracks is 1 to 2 μm for a track width of 0.4 - 1.3 μm.

After a new record carrier 32 has been placed the read/write head 30 is brought to a position opposite the lead-in track 37a and the adjustment information is read. This adjustment information may be recorded in the lead-in track 37a, for example, in conformity with the CD-ROM format. In accordance with this CD-ROM format digital data is recorded in blocks 50 (see Fig.6). Each block comprises 588 rows 51 of four eight-bit bytes 52 each. The first three rows of each block 50 store a specific 12-byte synchronization code. The fourth row is reserved for a four-byte block-address code. The other rows are reversed for data storage. The adjustment information can be arranged in a block with a unique block address. For the purpose of reading the adjustment information stored in this leader track 37 the recording system is provided with read circuit 38 coupled to the write/read head 30 for converting the read signal V1 supplied by the optical read/write head 30 in the read mode into a digital information signal V1d comprising the consecutive bytes of the blocks 50 being read. The read circuit 38 is of a customary type as employed, for example, in the Philips Compact Disc Rom system CM100/25,CM100/30, CM110/25 or CM110/30. Such a read circuit supplies the read-out data bytes in the form of a serial bit stream which is in synchronism with a clock signal c1d, which is also supplied by the read circuit. The data bytes supplied by the read circuit are applied to a microcomputer system 40 by means of a customary interface circuit 39.

Adjustment of the write signal waveforms proceeds as follows. After a new record carrier 32 has been placed in the recording system the microcomputer system 40 performs a starting program. During the execution of the starting program the read/write head 30 is set to the read mode via the interface circuit 39. Moreover, under control of the microcomputer system 40 the read/write head 30 is positioned relative to the lead-in track 37a. During reading of the lead-in track 37 the block with the adjustment information is detected by means of the unique block-address code and is subsequently read. After this, the microcomputer system 40 sets the electronically actuated switch 32b in conformity with the adjustment information read. After termina-

tion of the starting program the read/write head 30 is set to the write mode and the information signal Vi is recorded in the track portion 37b with the write signal waveforms thus selected.

Fig. 7 shows another embodiment of a recording system in accordance with the invention. Parts of the recording system corresponding to those of the system shown in Fig. 4 bear the same reference numerals. The recording system further comprises an oscillator system 60 for generating a first clock cl1 and a second clock signal cl2 whose frequency is eight times that of the clock signal cl1. A signal generator 61 supplies the EFM-modulated information signal Vi to be recorded to a control circuit 62 in synchronism with the first clock signal cl1 to convert the information signal Vi into the write signals Vs for the optical read/write head 30. The control circuit 62 comprises a detection circuit 63 for detecting series of consecutive bit cells of the logic value "1". The detection circuit 63 generates a detection signal in the form of codes representing the number of bit cells in the detected series. As already stated, this number is minimum three and maximum eleven for EFM-modulated signals. The detection signal is applied to a write signal generator 65 via signal lines 64, said generator generating a write signal Vs for each of the different detection signals, to write a recording mark having a length corresponding to the number of bit cells represented by the relevant detection signal. Hereinafter, the write signals for forming recording marks representing series of 3, ..., 11 contiguous bit cells will be referred to as Vs3, ..., Vs11 respectively. The recording marks themselves will be referred to briefly as I3 marks, ..., I11 marks, the numerals 3, ..., 11 each indicating the number of bit cells represented by these marks. By means of an adjustment circuit 66 connected to the microcomputer system 40 the relationship between the detection signals and the write signals Vs can be selected, inconformity with the adjustment information read from the lead-in track 37a of the record carrier 32 during the staring phase.

Fig. 8 shows an example of the control circuit 62 in detail. The detection circuit 63 used in the control circuit 62 comprises 12-bit shift register 70 to which the information signal Vi to be recorded is applied via a serial data input 71. The clock signal Cl1 is applied to the clock input of the shift register 70. In response to the clock pulse of the clock signal C11 the information signal Vi is read into the shift register 70, the information signal delayed by 1, ... 12 clock pulses appearing respectively on the Q1 ... Q12 outputs of the shift register 70. The Q11 output of the shift register 70 is applied to a two-input NAND-gate 72. The Q12 output of the shift register 70 is applied to the other input of the NAND gate 72 via an inverter circuit 73. The Q1, ..., Q8 outputs of the shift register 70 are applied to an encoding circuit 74, which converts the signal values on the outputs of the shift register 70 into detection signals D0, D1, D2 and D3 in conformity with the relationship given in Fig.9. Such an encoding circuit may comprise, for example, an integrated circuit of the type of 74LS148. The detection signals are applied to a parallel-in parallel-out register 75 which forms part of the write-signal generator 65. Inconjunction with a counter 76 for counting the number of clock pulses of the clock signal Cl1 the register 75 constitutes an address generator 77 for a memory 78, for example a 2k x 8 bis memory of the RAM type, The counter 76 is of a kind which has a reset input for resetting the count to zero and which stops counting if a predetermined final count "15" is reached. The reset input of the counter 76 is connected to the output of the NAND-gate 72. The address on the output of the address generator 77 is applied to the address inputs ofthe memory 78 via a tristate buffer 79 and an address bus 80. The eight data outputs of the memory 78 are applied to a parallel-serial converter 82 via a data bus 81. The converter 82 is controlled by the clock signal C12 applied to the clock input to control the serial data output and by the clock signal Cl1 applied to the load-enable input to control the parallel input of the data applied via the bus 81. The serial output of the converter 82 constitutes the output for the write signal Vs.

Conversion of the information signal Vi into write signals Vs proceeds as follows. By means of the inverter circuit 73 and the NAND gate 72 the beginning of the series of consecutive bit cells of a logic value "1" is detected (see Fig. 13). As soon as the beginning of such a series reaches the output Q11 of the shift register 70 the output Vn of the NAND gate 72 becomes "0". The detection signals D0, ..., D3, which at this instant represent the length of the detected series, are loaded into the buffer 75 in response to the 1-0 transition on the output of the NAND gate 72. (It is to be noted once again that the series are at least three bit cells long, so that for determining the detection signals D0, ..., D3 the signal values on the outputs Q9 and Q10 of the register 70 are irrelevant, because they are always "1" at the instant at which the leading end of the series reaches the Q11 output). The counter 76 is also set to zero in response to the 1-0 transition on the output of the NAND gate. Thus, in response to the detection of a series of bit cells of the value "1" the address generator 77 is set to an initial address determined by the length of the detected series. This initial address indicates the first address of a series of consecutive 8-bit storage locations in the memory 78, which stores the write signal for forming a

recording mark having a length corresponding to the length of the detected series. Fig. 10 gives the addresses of the storage locations reserved for the storage of the write signals Vs. Fig. 11, by way of example, shows the consecutive bytes Si.j representing the write signals Vs3, Vs7 and Vs11, i indicating to which write signal the relevant byte belongs and j being the sequence number of the byte in the sequence of bytes. The storage locations in which no write signals are stored are loaded with bits of the value "0". In the way described above the storage location in which the first byte of the associated write signal is stored is addressed after detection of a series, Subsequently, in response to a pulse of the clock signal, the part of the address supplied by the counter 76 is each time incremented by one until a subsequent series is detected or until the counter has reached its final count "15". Thus, the consecutive bytes representing the desired write signal Vs are each loaded from the memory 78 into the parallel-serial converter 82 and are subsequently converted into a series of binary bit cells constituting the write signal Vs. With the detection circuit 63 and the write-signal generator 65 described above the write signals Vs can be optimized with respect to the recording material in a very simple way by adapting the write signals Vs stored in the memory 78. For each type of record carrier the optimum write signals can be recorded in the lead-in track 37a, in the data block 50 reserved for this purpose in accordance with the CD-ROM format. Fig. 12, by way of example, shows how the bytes Si.j are arranged within the data block 50. For the arrangement of the bytes S.i.j. shown in Fig. 12 the sequence of the bytes is identical to the sequence in which they must be stored in the memory 78. After a record carrier 32 has been inserted the microcomputer system 40 performs the starting program, during which the read/write head 30 is brought in a position opposite the lead-in track 37a and the information stored in the lead-in track 37a is read. By means of the block addresses the microcomputer system 40 then detects the block address of the block 50 in which the write signals Vs are stored and subsequently loads the memory 78 with the write signals Vs stored in the detected data block 50 via the adjustment circuit 66. For this purpose the adjustment circuit 66 comprises a tri-state buffer 83, which connects the address bus of the microcomputer system 40 to the address inputs of the memory 78 via the address bus 80, and a tri-state buffer 84, which connects the data bus of the microcomputer system 40 to the data inputs of the memory 78 via the bus 81. During loading of the memory 78 the buffers 83 and 84 are enabled by a selection signal Ss from the computer system. The selection signal Ss is also applied to the buffer 79 via an inverter circuit 85, causing the outputs of the tri-state buffer 78 to assume a high-impedance state. Further, a write signal Sw from the microcomputer system 40 is applied to the memory 78 for controlling the loading operation of the memory 78. A gate circuit 86 is arranged in the line supplying the load signal Sw to interrupt the load signal Sw as soon as the buffers 83 and 84 are no longer enabled by the selection signal Ss after termination of the loading process of the memory 78.

In the embodiments described in the foregoing the adjustment information is included in EFM data blocks 50, recorded in the lead-in track 37a. However, the subcode Q-channel signal of an EFM signal in conformity with the CD standard is also very suitable for recording the adjustment information. This Q-channel signal comprises 98 bits in each EFM subcode frame interleaved with the remainder of the information.

Fig. 14 shows the format of the 98 Q-channel bits of a subcode frame. The 98 bits are divided into one 2-bit group100, two 4-bit groups 101 and 102, two 8-bit groups 103 and 64, 56-bit groups 105, and one 16-bit group 106. The bits of group 100 are used for synchronising purposes. The bits of group 101 are employed as control bits. In the lead-in track 37a the groups 102 and 103 form a unique bit combination "100" (hexadecimal), which indicates that the relevant track portion forms part of the lead-in track 37a.

By means of 8 bits of group 104 the type of information stored in the group 105 is characterized. This is generally a track number indicating a specific track portion, the address of this portion being specified in group 105.

However, a unique bit combination, for example FF (hexadecimal), indicates that the bits in group 105 represent information on record-carrier parameters. Some of these bits, for example the three most significant bits of subgroup 105f, are used for storing the adjustment information specifying the desired write signal waveform. The other bits of the group 105f may be used for specifying other parameters, for example the desired write intensity.

During scanning of the lead-in track 37a the control information relating to the record-carrier parameters can be extracted simply from the Q-channel bits recovered from the EFM subcode by means of a conventional EFM subcode demodulator.

Fig. 15 shows an embodiment of the system in accordance with the invention, in which the adjustment information is recovered from the subcode Q-channel signal. Instead of the data signal V1d the subcode Q-channel signal, which is derived from the read signal V1 by means of a subcode de-

modulator 38a of a customary type in the read circuit 38, is applied to the interface circuit 39.

Fig. 16 shows a flowchart for extracting the control information from the Q-channel signal. This program is carried out each time that the recording system 10 is put into operation after changing of the record carrier. In step S71 the read/write head 30 is positioned opposite the lead-in track 37a under control of the microcomputer system 40 by means of the motor 33 and the spindle 34. Subsequently, reading of the information recorded in the lead-in track 37a is started.

In step S72 a block of 98 associated Q-channel bits is read and in step S73 it is ascertained by means of the bits of groups 102, 103 and 104 whether adjustment information is stored in the group 105f. If this is so, the information represented by the bits ofthegroup 105f is stored in a memory of the microcomputer system in step S75. The program then proceeds with step S72, in which a subsequent block of 98 Q-channel bits is read in. If during step S73 it is found that block 105f does not contain any parameter information, step S73 is followed by step S74, in which it is ascertained with the aid of the block of Q-channel bits read in whether the end of the lead-in track 4a is reached. If this is not the case, the program proceeds with step S72, If the end is reached the program is terminated.

For the adjustment of the write signal waveforms the system shown in Fig. 15 comprises a control circuit 110 which converts the EFM modulated signal Vi into write signals Vs having a waveform defined by the adjustment information. For the purpose of adjustment the control circuit 110 is coupled to the microcomputer 40 via a bus 111 and the interface circuit 39. The control circuit 110, which will be described in more detail hereinafter, generates pulse-shaped write signals Vs which are applied to a multiplier circuit 112, in which the write signal is multiplied by a signal appearing on the output of the digital-to-analog converter 113, in order to adjust the desired write intensity of the beam 31. The digital inputs of the digital-to-analog converter 113 are connected to the microcomputer system 40 via a bus 114 and the interface circuit 39.

The output signal Vs′ of the multiplier circuit 112 is applied to the read/write head 30, which in response to the pulses on the output of the multiplier produces radiation pulses of an intensity proportional to the magnitude of the applied pulses.

Fig. 17 shows an example of the control circuit 110 for converting the signal Vi into write signals Vs. The control circuit 110 comprises two three-bit parallel-serial converters 120 and 121. The parallel inputs of the converter 120 are connected to the outputs of a 3-channel multiplex circuit 122. A bit combination "000" is applied to input a of the multiplex circuit 122 and bit combinations "001" and "010" are applied to the inputs b and c respectively. The control inputs of the multiplex circuit 122 are connected to the bus 111, in such a way that depending on the adjustment information applied via the bus 11 one of the bit combinations "000", "001" or "010" is applied to the parallel inputs of the parallel-serial converter 120.

The bit combination "010" is applied to the parallel inputs of the parallel-serial converter 121. The parallel-load inputs of the converters 120 and 121 are controlled by means of the clock signal Cl1 whose frequency is equal to the bit frequency of the EFM-modulated signal Vi. The clock inputs for the serial output of the bit combinations in the converters are controlled by a clock signal c13 of a frequency equal to three times the bit frequency of the signal Vi. The aerial outputs of the converters 120 and 121 are respectively fed to a first input and a second input of a 3-channel multiplex circuit 123. A logic "0" signal is applied to the third input of the multiplex circuit 123. The multiplex circuit 123 connects the output 124 of the multiplex circuit 123 to one of its inputs depending on the control signals applied by a decoder circuit 128.

The input signals of the decoder circuit 128 are derived from the signal Vi. For this purpose the control circuit 110 comprises a delay circuit 125, for example a flip-flop controlled by the clock signal Cl1, which flip-flop delays the signal Vi by a time interval corresponding to one bit length. The delayed signal is designated Vi′. The delayed signal Vi′ is applied to an input of a two-input AND gate 127 via an inverter circuit 126. The signal Vi is applied to the other input of the AND gate 127, so that the output signal ofthe AND gate 127 indicates whether the bit of the signal Vi is the first logic "1" bit of a sequence of logic "1" bits.

The output signal of the AND gate 127 and the signal Vi are applied to the inputs of the decoder circuit 128, which depending on the bit combination represented by the applied signals controls the multiplex circuit 123 in such a way that the output of the converter 120 is connected to the output 124 if the output signal of the AND gate 127 has the logic value "1", the output of the converter 121 is connected to the output 129 if the output signal of the AND gate 117 has the logic value "0" and the logic value of the signal Vi is "1", and the output 129 is connected to the input carrying the logic "0" signal if the logic value of the signal Vi is "0".

The system shown in Fig. 17 operates as follows. If a signal Vi is to be recorded, the read/write head 30 is positioned opposite the track portion in which the recording is to be made.

Moreover, the write intensity is adjusted to the desired value by the microcomputer system 40, by

loading the digital-to-analog converter 113 with a value corresponding to the desired write intensity d stored in the memory of the microcomputer 40, after the adjustment information has been read from the lead-in track 37a. Moreover, the adjustment circuit 110 is set in conformity with the adjustment information thus read and stored in the memory. Finally, the read/write head 30 is set to the write move, after which recording begins.

During recording the signal Vi is converted into the signal Vs. In response to a clock pulse of the clock signal Cl1 with the bit combinations on the parallel inputs are loaded into the parallel-serial converters 120 and 121 with the bit frequency of the signal Vi and subsequently the contents of the converters 120 and 121 is read out serially with the clock frequency c13, which is three times as high. If the first logic "1" bit of a sequence of logic "1" s of the signal Vi is applied to the control circuit 110, the bit pattern loaded into the parallel-serial converter 120 is transferred as the write signals Vs, via the multiplex circuit 123. This depends on the setting of the control circuit, "000" (see Fig. 18a), "001" (see Fig. 19b), or "010" (see Fig. 18c). For the second and subsequent logic "1" bits and a sequence of logic "1" bits of the signal Vi the bit pattern "010" from the serial-parallel converter 121 is transferred as the write signal via the multiplex circuit 123. For every logic "0" bit of the signal Vi the logic "0" signal is transferred to the input of the multiplex circuit 133.

Fig. 18 shows the write signal waveform for three different setting of the control circuit 110, the signal Vsa being the write signal in the case that the "a" input of the multiplex circuit 122 is selected. The signal Vsb is the write signal if the "b" input of the multiplex circuit 122 is selected, and signal Vsc is the write signal if the "c" input is selected. The pulses 20a and 20b again are the leader pulses to compensate for the occurrence of thermal effects in the control system.

Owing to the possibility of adjusting the write intensity and the possibility to choose from the three different pulse patterns shown in Fig. 18 it is possible to provide compensation for the thermal effects occuring during recording for a very large number of different record-carrier types.

Claims

1. A system for recording an information signal, comprising an inscribable and optically readable record carrier, and a recording apparatus for providing the record carrier with a pattern of recording marks having modified optical properties, which pattern represents the information signal, for which purpose the recording apparatus comprises a control circuit for converting the information signal in conformity with a specific relationship into a series of consecutive write signals to form the consecutive recording marks with modified optical properties, the record carrier being provided with readable adjustment information which is indicative of the write signal waveforms required for the relevant record carrier, and the recording apparatus comprising a read device for reading the adjustment information on the record carrier in a time interval prior to recording and an adjustment circuit for adjusting the write signal waveforms, in conformity with the adjustment information read, by adapting the relationship between the write signals and the information signal, characterized in that the write signals comprise trains of pulses to form recording marks comprising sequences of overlapping recording sub-marks, and in that the adjustment circuit is adapted to adjust said trains of pulses.

2. A system as claimed in Claim 1, characterized in that the recording apparatus comprises an optical write head responsive to the pulses of the pulse trains of the write signals to generate radiation pulses for the formation of recording sub-marks, which pulse trains may comprise at least one leader pulse for generating a preheating radiation pulse to compensate for thermal effects in the record carrier, the adjustment circuit being adapted to adjust the number of leader pulses and the position of the leader pulses relative to the other pulses, depending on the adjustment information being read.

3. A system as claimed in Claim 1, or 2 characterized in that the recording apparatus comprises scanning means for scanning a radiation-sensitive layer of the record carrier, for the purpose of forming recording marks, by means of a radiation beam modulated in conformity with the write signals, the adjustment information being at least indicative of the write intensity of the radiation beam required during the formation of the recording marks and the adjusment circuit including means for adjusting the write intensity in conformity with the adjustment information being read.

4. A system as claimed in any one of the Claims 1 to 3, for recording an information signal comprising binary bit cells characterized in that the control circuit comprises a detection circuit for detecting series of bit cells of the same first logic value and for supplying a detection signal which is representative of the number of bit

loading the digital-to-analog converter 113 with a value corresponding to the desired write intensity d stored in the memory of the microcomputer 40, after the adjustment information has been read from the lead-in track 37a. Moreover, the adjustment circuit 110 is set in conformity with the adjustment information thus read and stored in the memory. Finally, the read/write head 30 is set to the write move, after which recording begins.

During recording the signal Vi is converted into the signal Vs. In response to a clock pulse of the clock signal Cl1 with the bit combinations on the parallel inputs are loaded into the parallel-serial converters 120 and 121 with the bit frequency of the signal Vi and subsequently the contents of the converters 120 and 121 is read out serially with the clock frequency c13, which is three times as high. If the first logic "1" bit of a sequence of logic "1" s of the signal Vi is applied to the control circuit 110, the bit pattern loaded into the parallel-serial converter 120 is transferred as the write signals Vs, via the multiplex circuit 123. This depends on the setting of the control circuit, "000" (see Fig. 18a), "001" (see Fig. 19b), or "010" (see Fig. 18c). For the second and subsequent logic "1" bits and a sequence of logic "1" bits of the signal Vi the bit pattern "010" from the serial-parallel converter 121 is transferred as the write signal via the multiplex circuit 123. For every logic "0" bit of the signal Vi the logic "0" signal is transferred to the input of the multiplex circuit 133.

Fig. 18 shows the write signal waveform for three different setting of the control circuit 110, the signal Vsa being the write signal in the case that the "a" input of the multiplex circuit 122 is selected. The signal Vsb is the write signal if the "b" input of the multiplex circuit 122 is selected, and signal Vsc is the write signal if the "c" input is selected. The pulses 20a and 20b again are the leader pulses to compensate for the occurrence of thermal effects in the control system.

Owing to the possibility of adjusting the write intensity and the possibility to choose from the three different pulse patterns shown in Fig. 18 it is possible to provide compensation for the thermal effects occuring during recording for a very large number of different record-carrier types.

Claims

1. A system for recording an information signal, comprising an inscribable and optically readable record carrier, and a recording apparatus for providing the record carrier with a pattern of recording marks having modified optical properties, which pattern represents the information signal, for which purpose the recording apparatus comprises a control circuit for converting the information signal in conformity with a specific relationship into a series of consecutive write signals to form the consecutive recording marks with modified optical properties, the record carrier being provided with readable adjustment information which is indicative of the write signal waveforms required for the relevant record carrier, and the recording apparatus comprising a read device for reading the adjustment information on the record carrier in a time interval prior to recording and an adjustment circuit for adjusting the write signal waveforms, in conformity with the adjustment information read, by adapting the relationship between the write signals and the information signal, characterized in that the write signals comprise trains of pulses to form recording marks comprising sequences of overlapping recording sub-marks, and in that the adjustment circuit is adapted to adjust said trains of pulses.

2. A system as claimed in Claim 1, characterized in that the recording apparatus comprises an optical write head responsive to the pulses of the pulse trains of the write signals to generate radiation pulses for the formation of recording sub-marks, which pulse trains may comprise at least one leader pulse for generating a preheating radiation pulse to compensate for thermal effects in the record carrier, the adjustment circuit being adapted to adjust the number of leader pulses and the position of the leader pulses relative to the other pulses, depending on the adjustment information being read.

3. A system as claimed in Claim 1, or 2 characterized in that the recording apparatus comprises scanning means for scanning a radiation-sensitive layer of the record carrier, for the purpose of forming recording marks, by means of a radiation beam modulated in conformity with the write signals, the adjustment information being at least indicative of the write intensity of the radiation beam required during the formation of the recording marks and the adjusment circuit including means for adjusting the write intensity in conformity with the adjustment information being read.

4. A system as claimed in any one of the Claims 1 to 3, for recording an information signal comprising binary bit cells characterized in that the control circuit comprises a detection circuit for detecting series of bit cells of the same first logic value and for supplying a detection signal which is representative of the number of bit

cells of the detected series, and a write signal generator for generating, in response to the detection signals, the write signals, in conformity with a specific relationship between the write signals and the detection signals, the adjustment information on the record carrier being representative of the relationship between the write signals and the detection signals required for the relevant record carrier, and the adjustment circuit being adapted to establish the relationship in conformity with the adjustment information read.

5. A system as claimed in any one of the Claims 1 to 4, characterized in that the write signal generator comprises a memory for the storage of different write signals and means for supplying one of the stored write signals depending on the detection signal, and in that the adjustment circuit comprises a circuit for loading the memory with the write signals in conformity with the adjustment information read.

6. A system as claimed in Claim 5, characterized in that the adjustment information on the record carrier comprises the write signals required for the relevant recordcarrier, and in that the adjustment circuit is adapted to load the memory with the write signals comprised by the adjustment information.

7. A system as claimed in any one of the preceding Claims, characterized in that the adjustment information is recorded as a preformed information structure in a predetermined portion of a servo track of the record carrier, the recording apparatus comprising control means for reading the adjustment information from the predetermined portion of the servo track prior to recording.

8. A system as claimed in Claim 7, characterized in that the predetermined portion is a lead-in track situated at the beginning of the servo track.

9. A system as claimed in Claim 8, characterized in that a standard EFM signal, including a subcode signal, is recorded in the predetermined portion, the adjustment information being included in the Q-channel signal of the subcode signal, the read means comprising an EFM subcode demodulator for recovering the Q-channel signal from the EFM signal being read and means for extracting the adjustment information from the Q-channel signal.

10. A system as claimed in Claim 9, characterized in that the position of the adjustment information in the Q-channel signal is indicated by a unique bit combination at predetermined bit positions, the read means comprising detection means for detecting the unique bit combination and in response to the detection of said bit combination extracting the adjustment information from the Q-channel signal.

11. A recording apparatus comprising all the technical recording apparatus features as defined in any of the claims 1 to 10.

12. A record carrier comprising all the technical record carrier features as defined in any of the claims 4 to 10.

13. A recording apparatus for providing a record carrier with a pattern of recording marks with modified optical properties, which pattern represents an information signal made up of binary bit cells, for which purpose the recording apparatus comprises a control circuit for converting the information signal in conformity with a specific relationship into a sequence of consecutive write signals for the purpose of forming the consecutive recording marks with modified optical properties, characterized in that the control circuit comprises a detection circuit for detecting the sequences of bit cells of the same first logic value and for supplying a detection signal which represents the number of bit cells of the detected sequence, and a write signal generator for generating, in response to the detection signals, the write signals in conformity with a specified relationship between the write signals and the detection signals.

14. A recording apparatus as claimed in claim 13 characterized in that the write signals comprise trains of pulses to form recording marks comprising sequences of overlapping recording sub-marks, the write signal generator being adapted to generate the trains of pulses in patterns in which the arrangement of pulses depends on the number of bit cells of the detected sequences.

15. A recording apparatus as claimed in Claim 13 or 14 characterized in that the write signal generator comprises a memory for the storage of different write signals and means for supplying one of the write signals stored, depending upon the detection signal.

16. A recording apparatus as claimed in Claim 15, characterized in that the recording apparatus

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comprises an adjsutment circuit for loading the memory with the write signals.

Patentansprüche

1. System zum Aufzeichnen eines Informationssignals, mit einem beschreibbaren und optisch lesbaren Aufzeichnungsträger und einer Aufzeichnungseinrichtung zum Versehen des Aufzeichnungsträgers mit einem Muster von Aufzeichnungsmarken mit veränderten optischen Eigenschaften, welches Muster das Informationssignal darstellt, zu welchem Zweck die Aufzeichnungseinrichtung eine Steuerschaltung zum Umsetzen des Informationssignals in eine Reihe aufeinanderfolgender Schreibsignale entsprechend einer bestimmten Beziehung hat, um die aufeinanderfolgenden Aufzeichnungsmarken mit veränderten optischen Eigenschaften zu bilden, wobei der Aufzeichnungsträger mit lesbarer Einstellinformation versehen ist, die die für den betreffenden Aufzeichnungsträger geforderten Schreibsignalformen anzeigt, und die Aufzeichnungseinrichtung eine Leseeinrichtung zum Auslesen der Einstellinformation aufdem Aufzeichnungsträger in einem vor der Aufzeichnung gelegenen Zeitintervall und eine Einstellschaltung zum Einstellen der Schreibsignalformen entsprechend der gelesenen Einstellinformation durch Anpassen der Beziehung zwischen den Lesesignalen und dem Informationssignal hat, dadurch gekennzeichnet, daß die Schreibsignale Impulsserien zum Bilden von Aufzeichnungsmarken aus Folgen überlappender Teil-Aufzeichnungsmarken enthalten und daß die Einstellschaltung zum Einstellen der genannten Impulsserien eingerichtet ist.

2. System nach Anspruch 1, dadurch gekennzeichnet, daß die Aufzeichnungseinrichtung einen auf die Impulse der Impulsserien der Schreibsignale ansprechenden optischen Schreibkopf hat, um Strahlungsimpulse zur Bildung von Teil-Aufzeichnungsmarken zu erzeugen, welche Impulsserien mindestens einen Vorlaufimpuls zur Erzeugung eines Vorheizstrahlungsimpulses zum Ausgleichen thermischer Effekte in dem Aufzeichnungsträger enthalten können, wobei die Einstellschaltung zum Einstellen der Anzahl Vorlaufimpulse und der Lage der Vorlaufimpulse in bezug auf die anderen Impulse abhängig von der gelesenen Einstellinformation eingerichtet ist.

3. System nach Anspruch 1 oder 2, dadurch gekennzeichnet, daß die Aufzeichnungseinrichtung Abtastmittel zur Ablastung einer strahlungsempfindlichen Schicht des Aufzeichnungsträgers enthält, um mit Hilfe eines den Schreibsignalen entsprechend modulierten Strahlungsbündels Aufzeichnungsmarken zu bilden, wobei die Einstellinformation mindestens die während der Bildung der Aufzeichnungsmarken erforderliche Schreibintensität des Strahlungsbündels anzeigt und wobei die Einstellschaltung Mittel zur Einstellung der Schreibintensität entsprechend der gelesenen Einstellinformation enthält.

4. System nach einem der Ansprüche 1 bis 3 zum Aufzeichnen eines binäre Bitzellen enthaltenden Informationssignals, dadurch gekennzeichnet, daß die Steuerschaltung eine Detektorschaltung zum Detektieren von Bitzellenfolgen mit dem gleichen ersten Logikwert und zum Ausgeben eines Detektorsignals, das die Anzahl von Bitzellen der detektierten Folge darstellt, und einen Schreibsignalgenerator zum Erzeugen der Schreibsignale entsprechend einer bestimmten Beziehung zwischen den Schreibsignalen und den Detektorsignalen als Reaktion auf die Detektorsignale umfaßt, wobei die Einstellinformation auf dem Aufzeichnungsträger die für den betreffenden Aufzeichnungsträger geforderte Beziehung zwischen den Schreibsignalen und den Detekiorsignalen darstellt und wobei die Einstellschaltung zum Erstellen der Beziehung entsprechend der gelesenen Einstellinformation eingerichtet ist.

5. System nach einem der Ansprüche 1 bis 4, dadurch gekennzeichnet, daß der Schreibsignalgenerator einen Speicher zum Speichern verschiedener Schreibsignale sowie Mittel zum Abgeben eines der gespeicherten Schreibsignale in Abhängigkeit vom Detektorsignal umfaßt, und daß die Einstellschaltung eine Schaltung zum Laden des Speichers mit den Schreibsignalen entsprechend der gelesenen Einstellinformation enthält.

6. System nach Anspruch 5, dadurch gekennzeichnet, daß die Einstellinformation auf dem Aufzeichnungsträger die für den betreffenden Aufzeichnungsträger geforderten Schreibsignale enthält und daß die Einstellschaltung zum Laden des Speichers mit den in der Einstellinformation enthaltenen Schreibsignalen eingerichtet ist.

7. System nach einem der vorhergehenden Ansprüche, dadurch gekennzeichnet, daß die Einstellinformation als zuvor gebildete Informationsstruktur in einem vorgegebenen Abschnitt

einer Servospur des Aufzeichnungsträger aufgezeichnet ist, wobei die Aufzeichnungseinrichtung Steuerungsmittel zum Auslesen der Einstellinformation aus dem vorgegebenen Abschnitt der Servospur vor der Aufzeichnung enthält.

8. System nach Anspruch 7, dadurch gekennzeichnet, daß der vorgegebene Abschnitt eine am Anfang der Servospur liegende Anlaufspur ist.

9. System nach Anspruch 8, dadurch gekennzeichnet, daß in dem vorgegebenen Abschnitt ein ein Subcodesignal enthaltendes Standard-EFM-Signal aufgezeichnet ist, wobei die Einstellinformation in das Q-Kanalsignal des Subcodesignals aufgenommen ist und wobei die Lesemittel einen EFM-Subcode-Demodulator zum Rückgewinnen des Q-Kanalsignals aus dem gelesenen EFM-Signal und Mittel zum Extrahieren der Einstellinformation aus dem Q-Kanalsignal enthalten.

10. System nach Anspruch 9, dadurch gekennzeichnet, daß die Lage der Einstellinformation in dem Q-Kanalsignal durch eine eindeutige Bitkombination an vorgegebenen Bitpositionen angegeben wird, wobei die Lesemittel Detektormittel zum Detektieren der eindeutigen Bitkombination und zum Extrahieren der Einstellinformation aus dem Q-Kanalsignal als Reaktion auf die Detektion dieser Bitkombination enthalten.

11. Aufzeichnungseinrichtung mit all den technischen Aufzeichnungseinrichtung-Eigenschaften wie in einem der Ansprüche 1 bis 10 definiert.

12. Aufzeichnungsträger mit all den technischen Aufzeichnungsträger-Egenschaffen wie in einem der Ansprüche 4 bis 10 definiert.

13. Aufzeichnungseinrichtung zum Versehen eines Aufzeichnungsträgers mit einem Muster von Aufzeichnungsmarken mit veränderten optischen Eigenschaften, welches Muster ein aus binären Bitzellen gebildetes Informationssignal darstellt, zu welchem Zweck die Aufzeichnungseinrichtung eine Steuerschaltung zum Umsetzen des Informationssignals in eine Reihe aufeinanderfolgender Schreibsignalen entsprechend einer bestimmten Beziehung hat, um die aufeinanderfolgenden Aufzeichnungsmarken mit veränderten optischen Eigenschaften zu bilden, dadurch gekennzeichnet, daß die Steuerschaltung eine Detektorschaltung zum Detektieren der Bitzellenfolgen mit gleichem ersten Logikwert und zum Ausgeben eines die Anzahl von Bitzellen der detektierten Folge darstellenden Detektorsignals sowie einen Schreibsignalgenerator zum Erzeugen der Schreibsignale entsprechend einer bestimmten Beziehung zwischen den Schreibsignalen und den Detektorsignalen als Reaktion auf die Detektorsignale umfaßt.

14. Aufzeichnungseinrichtung nach Anspruch 13, dadurch gekennzeichnet, daß die Schreibsignale Impulsserien zur Bildung von Aufzeichnungsmarken aus Folgen überlappender Teil-Aufzeichnungsmarken enthalten, wobei der Schreibsignalgenerator für die Erzeugung von Impulsserien in Mustern eingerichtet ist, in denen die Anordnung der Impulse von der Anzahl Bitzellen der detektierten Folgen abhängt.

15. Aufzeichnungseinrichtung nach Anspruch 13 oder 14, dadurch gekennzeichnet, daß der Schreibsignalgenerator einen Speicher zum Speichern verschiedener Schreibsignale sowie Mittel zum Abgeben eines der gespeicherten Schreibsignale in Abhängigkeit von dem Detektorsignal umfaßt.

16. Aufzeichnungseinrichtung nach Anspruch 15, dadurch gekennzeichnet, daß die Aufzeichnungseinrichtung eine Einstellschaltung zum laden des Speichers mit den Schreibsignalen enthält.

Revendications

1. Système d'enregistrement d'un signal d'information, comportant un support d'enregistrement enregistrable et optiquement lisible et un dispositif d'enregistrement pour pourvoir le support d'enregistrement d'une configuration de marques d'enregistrement ayant des propriétés optiques modifiées et représentant le signal d'information, raison pour laquelle le dispositif d'enregistrement comporte un circuit de commande pour convertir, selon un rapport déterminé, le signal d'information en une série de signaux d'écriture successifs pour former les marques d'enregistrement successives à propriétés optiques modifiées, le support d'enregistrement étant pourvu d'information de réglage lisible, indicative des formes d'onde de signal d'écriture requises pour le support d'enregistrement concerné et, le dispositif d'enregistrement comportant un dispositif de lecture pour lire l'information de réglage sur le support d'enregistrement dans un intervalle de temps précédant l'enregistrement et un circuit de réglage pour régler les formes d'onde du signal

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d'écriture selon l'information de réglage lue en adaptant le rapport entre les signaux d'écriture et le signal d'information, caractérisé en ce que les signaux d'écriture comportent des trains d'impulsions pour former des marques d'enregistrement comportant des séries de sous-marques d'enregistrement chevauchantes, et en ce que le circuit de réglage est conçu pour régler lesdits trains d'impulsions.

2. Système selon la revendication 1, caractérisé en ce que le dispositif d'enregistrement comporte une tête d'écriture optique pour engendrer, en réaction aux impulsions des trains d'impulsions des signaux d'écriture, des impulsions de rayonnement pour former des sous-marques d'enregistrement, trains d'impulsions qui peuvent comporter au moins une impulsion de début pour engendrer une impulsion de rayonnement de préchauffage servant à compenser des effets thermiques dans le support d'enregistrement, le circuit de réglage étant conçu pour régler en fonction de l'information de réglage lue le nombre d'impulsions de début et la position des impulsions de début par rapport aux autres impulsions.

3. Système selon la revendication 1 ou 2, caractérisé en ce que le dispositif d'enregistrement comporte des moyens d'exploration d'une couche du support d'information, sensible au rayonnement, afin de former des marques d'enregistrement à l'aide d'un faisceau de rayonnement modulé selon les signaux d'écriture, l'information de réglage étant au moins indicative de l'intensité d'écriture du faisceau de rayonnement, nécessaire au cours de la formation des marques d'enregistrement et le circuit de réglage comportant des moyens pour régler l'intensité d'écriture selon l'information de réglage lue.

4. Système selon l'une quelconque des revendications 1 à 3, pour enregistrer un signal d'information comportant des cellules de bit binaires, caractérisé en ce que le circuit de commande comporte un circuit de détection pour détecter des séries de cellules de bit ayant la même première valeur logique et pour fournir un signal de détection représentatif du nombre de cellules de bit de la série détectée, et un générateur de signaux d'écriture pour engendrer, en réaction aux signaux de détection, les signaux d'écriture selon un rapport déterminé entre les signaux d'écriture et les signaux de détection, l'information de réglage que porte le support d'enregistrement étant représentatif du rapport entre les signaux d'écriture et les signaux de détection nécessaires pour le support d'enregistrement concerné, et le circuit de réglage étant conçu pour établir le rapport selon l'information de réglage lue.

5. Système selon l'une quelconque des revendications 1 à 4, caractérisé en ce que le générateur de signaux d'écriture comporte une mémoire pour stocker différents signaux d'écriture et des moyens pour délivrer, en fonction du signal de détection, l'un des signaux d'écriture stockés et en ce que le circuit de réglage comporte un circuit pour introduire dans la mémoire les signaux d'écriture selon l'information de réglage lue.

6. Système selon la revendication 5, caractérisé en ce que l'information de réglage existant sur le support d'enregistrement comporte les signaux d'écriture requis pour le support d'enregistrement concerné, et en ce que le circuit de réglage est agencé pour introduire dans la mémoire les signaux d'écriture compris par l'information de réglage.

7. Système selon l'une quelconque des revendications précédentes, caractérisé en ce que l'information de réglage est enregistrée sous la forme d'une structure d'information préformée, dans une partie prédéterminée d'une servopiste du support d'enregistrement, le dispositif d'enregistrement comportant des moyens de commande pour la lecture, avant l'enregistrement, de l'information de réglage dans la partie prédéterminée de la servopiste.

8. Système selon la revendication 7, caractérisé en ce que la partie prédéterminée est une piste de départ située au début de la servopiste.

9. Système selon la revendication 8, caractérisé en ce qu'un signal EFM standard, comportant un signal de sous-code, est enregistré dans la partie prédéterminée, l'information de réglage étant comprise dans le signal de canal Q du signal de sous-code, les moyens de lecture comportant a démodulateur de sous-code EFM pour récupérer le signal de canal Q à partir du signal EFM lu et des moyens pour extraire l'information de réglage du signal de canal Q.

10. Système selon la revendication 9, caractérisé en ce que la position qu'occupe l'information de réglage dans le signal de canal Q est indiquée par une combinaison unique de bits dans des positions de bit prédéterminées, les moyens de lecture comportant des moyens de

détection pour détecter la combinaison de bits unique et pour extraire, en réaction à la détection de ladite combinaison de bits, l'information de réglage du signal de canal Q.

11. Dispositif d'enregistrement comportant toutes les propriétés techniques de dispositif d'enregistrement telles que définies dans l'une quelconque des revendications 1 à 10.

12. Support d'enregistrement comportant toutes les propriétés techniques de support d'enregistrement telles que définies dans l'une quelconque des revendications 4 à 10.

13. Dispositif d'enregistrement pour pourvoir le support d'enregistrement d'une configuration de marques d'enregistrement ayant des propriétés optiques modifiées et représentant un signal d'information constitué par des cellules de bit binaires, raison pour laquelle le dispositif d'enregistrement comporte un circuit de commande pour convertir, selon un rapport déterminé, le signal d'information en une série de signaux d'écriture successifs pour former les marques d'enregistrement successives à propriétés optiques modifées, caractérisé en ce que le circuit de commande comporte un circuit de détection pour détecter les séries de cellules de bit ayant la même première valeur logique et pour fournir un signal de détection représentant le nombre de cellules de bit de la série détectée, et un générateur de signaux d'écriture pour engendrer, en réaction aux signaux de détection, les signaux d'écriture selon un rapport déterminé entre les signaux d'écriture d'une part et les signaux de détection d'autre part.

14. Dispositif d'enregistrement selon la revendication 13, caractérisé en ce que les signaux d'écriture comportent des trains d'impulsions pour former des marques d'enregistrement comportant des séries de sous-marques d'enregistrement chevauchantes, le générateur de signaux d'écriture étant agencé pour engendrer les trains d'impulsions sous la forme de configurations dans lesquelles l'arrangement d'impulsions dépend du nombre de cellules de bit des séries détectées.

15. Dispositif d'enregistrement selon la revendication 13 ou 14, caractérisé en ce que le générateur de signaux d'écriture comporte une mémoire pour stocker différents signaux d'écriture, et des moyens pour délivrer, en fonction du signal de détection, l'un des signaux d'écriture stockés.

16. Dispositif d'enregistrement selon la revendication 15, caractérisé en ce qu'il comporte un circuit de réglage pour introduire les signaux d'écriture dans la mémoire.