CLAIMS

What is claimed is:

1. A method, comprising:

applying a first voltage to a first access line and a second access line of a first plurality of access lines of a memory array that comprises a plurality of memory cells to store a logic state, wherein the first plurality of access lines is in electronic communication with a plurality of capacitive cells to generate a filter capacitance and is perpendicular to a second plurality of access lines that is in electronic communication with the plurality of capacitive cells;

applying a second voltage to a third access line of the first plurality of access lines, wherein the third access line of the first plurality of access lines is adjacent to the first access line and the second access line of the first plurality of access lines; and

regulating the first voltage or the second voltage, or both, for at least a portion of the memory array with a capacitance between access lines of the first plurality of access lines resulting from the application of the first voltage and the second voltage.

2. The method of claim 1, wherein:

applying the first voltage comprises electronically coupling a first voltage rail to the first access line and the second access line of the first plurality of access lines; and

applying the second voltage comprises electronically coupling a second voltage rail to the third access line of the first plurality of access lines.

3. The method of claim 2, wherein electronically coupling the first voltage rail and the second voltage rail with the first, second, and third access lines of the first plurality of access lines comprises:

activating a first decoder that is in electronic communication with the first voltage rail, the second voltage rail, and the first plurality of access lines.

4. The method of claim 3, further comprising:

electronically coupling the first voltage rail to a fourth access line and a fifth access line of the first plurality of access lines;

electronically coupling the second voltage rail to a sixth access line of the first plurality of access lines, wherein the first voltage rail and the second voltage rail are

electronically coupled with the first, second, and the third access lines of the first plurality of access lines independently of electronically coupling the first voltage rail and the second voltage rail with the fourth, fifth, and sixth access lines of the first plurality of access lines.

5. The method of claim 4, wherein electronically coupling the first voltage rail and the second voltage rail with the fourth, fifth, and sixth access lines of the first plurality of access lines comprises:

activating a second decoder that is in electronic communication with the first voltage rail, the second voltage rail, and the first plurality of access lines.

6. The method of claim 2, wherein the first voltage rail is connected to a positive voltage source and the second voltage rail is connected to ground or virtual ground.

7. The method of claim 1, further comprising:

isolating the second plurality of access lines from the first voltage and the second voltage.

8. The method of claim 7, wherein isolating the second plurality of access lines from the first voltage and the second voltage comprises:

deactivating a decoder that is in electronic communication with the second plurality of access lines, the first voltage, and the second voltage.

9. The method of claim 1, further comprising:

applying a third voltage to the second plurality of access lines, wherein a magnitude of the third voltage is greater than a magnitude of the first voltage and less than a magnitude of the second voltage.

10. The method of claim 1, further comprising:

applying the first voltage to a first access line and a second access line of the second plurality of access lines, wherein applying the first voltage comprises electronically coupling a first voltage rail to the first access line and the second access line of the second plurality of access lines;

applying the second voltage to a third access line of the second plurality of access lines, wherein applying the second voltage comprises electronically coupling a second voltage rail to the third access line of the second plurality of access lines, and wherein the first voltage or the second voltage, or both, is regulated based on the capacitance between the

access lines of the first plurality of access lines and another capacitance between access lines of the second plurality of access lines resulting from the application of the first voltage and the second voltage.

11. The method of claim 10, wherein electronically coupling the first voltage rail and the second voltage rail with the first, second, and third access lines of the second plurality of access lines comprises:

activating a first decoder that is in electronic communication with the first voltage rail, the second voltage rail, and the second plurality of access lines.

12. An apparatus, comprising:

an array of memory cells to store a logic state;

a plurality of capacitive cells to generate a filter capacitance;

a first plurality of access lines in electronic communication with the plurality of capacitive cells;

a second plurality of access lines in electronic communication with the plurality of capacitive cells, wherein the second plurality of access lines is perpendicular to the first plurality of access lines;

a first voltage rail in electronic communication with a first subset of the first plurality of access lines; and

a second voltage rail in electronic communication with a second subset of the first plurality of access lines, wherein the plurality of capacitive cells, the first plurality of access lines, and the second plurality of access lines form a capacitive element between the first voltage rail and the second voltage rail.

13. The apparatus of claim 12, wherein the first voltage rail is in electronic communication with a first subset of the second plurality of access lines and the second voltage rail is in electronic communication with a second subset of the second plurality of access lines.

14. The apparatus of claim 12, further comprising:

a third voltage rail in electronic communication with the second plurality of access lines.

15. The apparatus of claim 12, wherein a capacitive cell of the plurality of capacitive cells comprises a capacitor and a selection component.

16. The apparatus of claim 12, wherein the capacitive element is variable based on a configuration of the first plurality of access lines and the second plurality of access lines.

17. The apparatus of claim 15, wherein the capacitor is any of a ferroelectric capacitor, a dielectric capacitor, or a ceramic capacitor.

18. An apparatus, comprising:

an array of memory cells to store a logic state;

a plurality of capacitive cells to generate a filter capacitance;

a first plurality of access lines in electronic communication with the plurality of capacitive cells, wherein access lines of the first plurality of access lines are oriented in a first direction; and

a second plurality of access lines in electronic communication with the plurality of capacitive cells, wherein access lines of the second plurality of access lines are oriented in a second direction that is perpendicular to the first direction;

wherein a first subset of the plurality of capacitive cells segments the array of memory cells in the first direction and a second subset of the plurality of capacitive cells segments the array of memory cells in the second direction.

19. The apparatus of claim 18, further comprising:

a plurality of decoders in electronic communication with the first plurality of access lines, the second plurality of access lines, and the capacitive cells, wherein a first subset of the plurality of decoders segments the array of memory cells in the first direction and a second subset of the plurality of decoders segments the array of memory cells in the second direction.

20. The apparatus of claim 19, wherein the array of memory cells, the plurality of capacitive cells, the first plurality of access lines, and the second plurality of access lines are located on a first layer of a plurality of layers, and the plurality of decoders are located on a second layer of the plurality of layers.

21. The apparatus of claim 18, wherein a first decoder of the plurality of decoders is in electronic communication with a first subset of the first plurality of access lines, a second decoder of the plurality of decoders is in electronic communication with a second subset of the first plurality of access lines.

22. The apparatus of claim 21, wherein a third decoder of the plurality of decoders is in electronic communication with a first subset of the second plurality of access lines, and a fourth decoder of the plurality of decoders is in electronic communication with a second subset of the second plurality of access lines.

23. An apparatus, comprising:

an array of memory cells to store a logic state;

a capacitive element comprising:

a plurality of capacitive cells to generate a filter capacitance;

a first plurality of access lines in electronic communication with the plurality of capacitive cells;

a second plurality of access lines in electronic communication with the plurality of capacitive cells, wherein the first plurality of access lines is in electronic communication with the plurality of capacitive cells and is perpendicular to a second plurality of access lines that is in electronic communication with the plurality of capacitive cells, and wherein the plurality of capacitive cells, the first plurality of access lines, and the second plurality of access lines are used to generate a variable capacitance; and

a controller in electronic communication with the array of memory cells and the capacitive element, wherein the controller is operable to:

apply a first voltage to a first access line and a second access line of the first plurality of access lines; and

apply a second voltage to a third access line of the first plurality of access lines, wherein the third access line is adjacent to the first access line and the second access line of the first plurality of access lines.

24. The apparatus of claim 23, further comprising:

a first voltage rail associated with the first voltage;

a second voltage rail associated with the second voltage;

a first decoder in electronic communication with the first plurality of access lines; and

a second decoder in electronic communication with the second plurality of access lines, wherein the controller is operable to:

activate the first decoder connecting the first voltage rail to the first access line and the second access line of the first plurality of access lines and the second voltage rail to the third access line of the first plurality of access lines, and

activate the second decoder connecting the first voltage rail to a first access line and a second access line of the second plurality of access lines and the second voltage rail to a third access line of the second plurality of access lines.

25. The apparatus of claim 23, further comprising:

a first voltage rail;

a second voltage rail;

a first decoder in electronic communication with the first plurality of access lines; and

a second decoder in electronic communication with the second plurality of access lines, wherein the controller is operable to:

deactivate the second decoder isolating the first voltage rail and the second voltage rail from the second plurality of access lines.