

PID FILTER CIRCUIT AND FIFO CIRCUIT

BACKGROUND OF THE INVENTION

The present invention relates to a filter circuit for selecting packets from among a plurality of packets of a time division multiplexed data stream. More particularly this invention relates to a filter circuit for selecting packets based on the PID (packet identifier) incorporated in the packet, and to a FIFO (first-in first-out) memory used in the filter circuit.

DESCRIPTION OF THE PRIOR ART

A plurality of types of data may be transmitted in a single data stream as individual time division multiplexed packets. Each packet includes a packet identifier (PID) that denotes the type of data that the packet contains. When the packet is received, the PID may be used to determine whether the packet contains a desired type of data.

The well-known MPEG 2 (Moving Picture Experts Group 2) audio/video/data compression standard uses time division multiplexed data packets. Each TS (Transport Stream) packet has a fixed length of 188 bytes as shown in Figure 1. The PID is thirteen bits long and is located twelve bits from the beginning of the packet.

In some cases, the position of the PID within a packet is not fixed. In the packet shown in Figure 2, the position of the PID is not fixed within the packet. In such instances, the packet includes a pointer that indicates the location of the PID. In the example shown in Figure 2, the pointer is located at the beginning of the packet.

In a system using time division multiplexed packets, the receiving side determines whether a received packet contains a desired type of data based on the packet ID. This process is implemented by a filter circuit that samples packets having predetermined PIDs from the packet stream.

Figure 3 is a block diagram showing one example of a configuration of a conventional PID filter circuit. In the example of Figure 3, the PID has a length of three words.

The filter circuit includes flip-flops (FF) 61 to 63 that delay the input packet data by a length of three words. An output of the flip-flop 63 of the last stage is provided to a FIFO (First-in First-out) memory 60 for implementing first-in first-out storage of the received packet data. Further, the outputs of the flip-flops 61 to 63 are provided to respective comparators 64 to 66 that compare the inputs from the flip-flops with predetermined data. The outputs of the respective comparators 64 to 66 are inputted to a three input AND gate 67 and the output of the AND gate controls the writing of data in the FIFO.

The PID filter circuit of Figure 3 operates as follows. The respective flip-flops 61 to 63 delay the input

data by one word. The comparator 64, the comparator 65 and the comparator 66 perform a comparison on respective sequential words of the received data. Therefore three continuous words are simultaneously delayed by the flip-flops 61 to 63 and three continuous words are compared by the comparators 64 to 66 at the same time. When the three words that constitute the PID of the received data are received by the comparators and are found to be the same as the predetermined PID words, the comparator provides an appropriate signal to the AND gate 67 and the output of the AND gate 67 is used as a control signal to enable writing of the input packet into the FIFO memory 60.

However, the conventional circuit of Figure 1 suffers from the problems described below. First, the example of Figure 3 is designed to operate only on a PID having a fixed length of three words. To operate on data having PIDs that are five words in length, five flip-flops and five comparators would be required. Furthermore, the circuit cannot use a simple two input AND gate since the number of inputs to the AND gate depends on the number of words in the PID. Therefore a complicated circuit is required.

Second, the example of Figure 3 requires that the position of the PID within the packet data is fixed. In the example shown in Figure 3, it is necessary for the PID to be located at the beginning of the packet data, in order to provide the correct data to the comparators and hence to store desired packets in the FIFO memory 60. For instance, if the PID begins at the third word of the packet, it is necessary to provide two additional flip-flops in between the flip-flop 63 and the FIFO memory 60. Furthermore, the PID must be provided at the same position in each packet, and therefore the circuit of Figure 3 cannot be used where the position of the PID is variable.

Thus the operation of the conventional circuit depends upon the PID having a fixed length and a fixed position within the packet.

SUMMARY OF THE INVENTION

In view of the foregoing, embodiments of the present invention seek to provide a PID filter circuit which may be configured to operate on PIDs having varying lengths and having varying positions within the packet data, and which includes a FIFO memory.

According to a first aspect of the present invention, there is provided a First-in First-out (FIFO) circuit including a FIFO memory for storing input data, said FIFO memory comprising:

- a dual port memory for storing said input data;
- a write pointer for indicating a write address within said dual port memory;
- a read pointer for indicating a read address within said dual port memory;
- a write control section for controlling write operations of said dual port memory such that the value of said write pointer is incremented when a write operation is performed, and such that when there is received a control signal indicating that input data stored in the dual port memory is not desired data, the value of said write pointer is decremented in accordance with a quantity of the desired input data already stored in the dual port memory; and

a read control section for controlling read operations of said dual port memory such that a read operation causes a value of said read pointer to be incremented, and such that read operations are not performed when a quantity of unread input data stored in the dual port memory is less than predetermined amount.

The above and further objects and novel features of the invention will be more fully understood from the following detailed description when the same is read in connection with the accompanying drawings. It should be expressly understood, however, that the drawings are for purpose of illustration only and are not intended as a definition of the limits of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

Figure 1 is a view showing a configuration of TS (Transport Stream) packets in accordance with the MPEG 2 (Moving Picture Experts Group 2) standard;

Figure 2 is a view showing one example of a packet having a variable PID (Packet identifier) position;

Figure 3 is a block diagram showing the configuration of a conventional PID filter circuit;

Figure 4 is a block diagram showing the configuration of a PID filter circuit of a preferred embodiment of the invention;

Figure 5 is a block diagram showing the configuration of a FIFO memory in accordance with the preferred embodiment; and

Figure 6 is a block diagram showing the configuration of a PID filter circuit of an alternative embodiment of the invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENTS

A preferred embodiment of the present invention will be described in detail in accordance with the accompanying drawings. Figure 4 is a block diagram showing a configuration of a PID filter circuit of a preferred embodiment of the invention, and Figure 5 is a block diagram showing an internal configuration of a FIFO memory.

The PID filter circuit shown in Figure 4 is provided with a FIFO memory 11 that stores input

packet data and provides output packet data, a comparator 12 for comparing data of respective words of respective packets of the input packet data, and a comparison value table 13 for storing therein comparison value data that is used for comparison to input packet data in the comparator 12. The FIFO memory 11 stores input packet data in response to an external a write demand signal, and the FIFO memory 11 outputs packet data in response to the combination of an external read demand from the external side and, a signal from the comparator 12. The FIFO memory 11 also clears input data within the FIFO memory 11 in response to the signal from the comparator 12. The input packet data is initially written to the FIFO memory without alteration. The comparison value table 13 is constituted by memory, and the comparator 12 specifies a word order of the PID to be detected such that the comparison value table 13 outputs words of comparison values in accordance with the specified word order.

Next, there is described an internal configuration of the FIFO memory 11 using Figure Figure 5. The FIFO memory 11 includes a dual port memory 21 that stores the packet data. The memory 21 is capable of executing a write operation and a read operation independently. The FIFO memory 11 is further provided with a write control section 22 for executing a write operation to the memory 21 in accordance with an external write demand signal, and a read control section 23 for executing a read operation from the memory 21 in accordance with an external read demand signal. A write pointer 24 maintains a next write address of the memory 21, and a read pointer 25 maintains a next read address of

the memory 21. A subtracter 26 calculates a difference between the write address maintained by the write pointer 24 and the read address maintained by the read pointer 25. An output signal from the comparator 12 (Figure 4) is provided to the write control section 22 and the read control section 23 as a control signal.

As described above, the memory 21 executes a write operation under the control of the write control section 22 and executes a read operation under the control of the read control section 23. When an external write demand signal is received, the write control section 22 commands the memory 21 to perform a write operation and increments the value of the write pointer 24. Thereafter, if the signal from the comparator indicates that the PID does not agree with the comparison value, the written packet data is to be superseded, and therefore the write control section 22 effectively clears the packet data by subtracting the quantity of data already written to the memory 21 from the value of the write pointer 24. When an external read demand signal is received, the read control section 23 commands the memory 21 to read out data so long as the signal from the comparator and the output of the subtracter 26 allow read out to occur. If the signal from the comparator does not indicate agreement between the input data and the comparison value, or if the output value of the subtracter 26 is less than the corresponding length of the packet and thus indicates that there is less than a complete packet of unread data available in the memory 21, the read control section 23 does not execute the read operation regardless of existence of the read demand.

Next, there will be described operation of the PID filter circuit. A fundamental operation of the PID filter circuit is that when an input packet is received, it is written to the FIFO memory 11

and at the same time, the comparator 12 compares the received data with the (comparison value) read out from the comparison value table 13. The single comparator 12 is used for the comparison regardless of word length of the PID or its position within the packet. When the length of the PID is more than the corresponding length of the comparator, the comparison value is read from the comparison value table 13 in successive portions, thus executing comparison successively. Furthermore, the FIFO memory 11 does not output packets while the comparator 12 is performing the comparison despite a read demand. When the result of comparison indicated by the output signal of the comparator indicates disagreement, the packet data of the compared packet written into the memory during the comparison is superseded in the FIFO memory 11 through adjustment of the write pointer as described above. Through this manner of operation, the circuit of the present embodiment operates as a packet ID (PID) filter.

Hereinafter, there will be described operation of the PID filter circuit further in detail.

Each packet of the input packet data contains a unique PID. Therefore the comparison value table 13 stores predetermined PIDs of desired packets prior to performing the packet filtering process. When the PID section of an input data packet is received, the comparator 12 reads out a PID from the comparison value table 13 and compares that PID to the PID of the input data packet.

In general, the FIFO memory implements a read operation in response to a read demand if data remains within the FIFO memory but does not implement a read operation if data does not remain within the

FIFO memory. In the case of the present PID circuit, it is not known whether a current input packet data is a desired packet data while the comparator 12 is in the process of comparing the PID. Therefore, in this PID filter circuit, a read demand is implemented if there is unread data with a length of more than one packet within the FIFO memory 11, and a read demand is not implemented if there is unread data with a length of less than one packet within the FIFO memory 11. The amount of the unread data stored in the FIFO memory 11 is indicated by the output of the subtracter 26, which represents the difference between the next write address and the next read address.

The PID filter circuit enables input packet data to be written to the FIFO unconditionally, but if the input packet data is determined not to be desired packet data, the input packet data already written in the FIFO memory 11 is superceded. Since any remaining data of undesired input packet data that has not yet arrived at the FIFO is not necessary, the writing of such remaining data may be prohibited on the basis of the signal from the comparator.

Next, there will be described operation of the comparator 12. The comparator 12 counts the amount of data (for instance, byte number, octet number) from the beginning of an input packet. When the position of the PID is variable and position information (a pointer) of the PID is included in the packet data, the comparator reads the pointer and uses the pointer to

locate the PID. When the position of the PID is fixed, the position of the PID is established beforehand, such as by a host CPU (not illustrated). In all cases, the comparator 12 counts the data from the beginning of the input packet data to detect the position of the PID.

When the data at the position of the PID arrives, the comparator 12 compares the value of the PID with a value of the comparison value table 13. The comparator 12 obtains the first word of the comparison value from the comparison value table 13 for comparison to the first word of the PID. The comparator 12 then compares the first word of the comparison value to the first word of the PID, while obtaining the second word of the comparison value from the comparison value table 13. The comparator 12 then compares the second word of the comparison value with the second word of the PID. The comparator 12 thus compares the whole PID data from the comparison value table 13 with the whole PID within the input packet data on a word by word basis. If the PID agrees completely with the comparison value, this is indicated to the FIFO memory 11 by an output signal of the comparator. In effect, the signal outputted from the comparator 12 represents either that it is in the process of performing the comparison operation (including a waiting period during which the PID of the input packet data has not arrived at the comparator), or that the PID agrees with the comparison value, or that the PID does not agree with the comparison value.

Next, the operation of the FIFO memory 11 is described with respect to Figure 5.

When a write demand for writing to the memory 21 is received, the write control section 22 causes the write operation to be performed. The write operation is performed with reference to the write pointer 24 as the write address, and after completion of the write operation the value of the write pointer 24 is incremented in accordance with an instruction from the write control section 22. A read operation is similarly performed in response to an external read demand. When there is a read demand, the read control section 23 causes the read operation to be performed in the memory 21. The read operation is performed with respect to the read pointer 25, and after completion of the read operation, the value of the read pointer 25 is incremented in accordance with an instruction from the read control section 23. As a result, the quantity of unread data stored in the memory 21 is the difference between the value of write pointer 24 and the value of read pointer 25. When the value of the write pointer 24 equals the value of the read pointer 25, all data in the memory 21 has been read, and consequently the read control section 23 does not reply to the read demand.

When the comparator 12 (Figure 4) is performing the comparison operation, it is not known whether the input packet data is a desired packet data. For that reason, write operations may be performed during the comparison operation. However, if at this time the difference between the write pointer 24 and the read pointer 25 is less than the length of one packet, the read control section 23 does not implement a read operation in response to the read demand. After the comparison is completed, if the data is determined to be desired data, the read control section 23 implements a read operation.

In contrast, if the data is determined not to be desired data the undesired data already written in the memory 21 is superseded by subtracting the amount of undesired data already written in the memory 21 from the value of the write pointer 24. Moreover, the write control section may be implemented such that no additional undesired data may be written into the FIFO memory 11 when the signal from the comparator after performing comparison indicates that the data is not desired data.

Thus, in the PID filter circuit of the first preferred embodiment, the comparator 12 counts the amount of data from the top of the packet data to locate the PID data in the packet to be used in the comparison operation. The comparator 12 allows the input packet data to remain within the FIFO memory 11 until it is determined whether the input packet data is desired. The input packet data stored in the FIFO is used if it is determined to be desired data, and is superseded if it is determined not to be desired data. Therefore, even if the position of the PID within the packet data is variable, packet filtering may be implemented without changing the circuit. Furthermore, since comparison is performed successively on words of the PID in the comparator 12 while reading out comparison value words from the comparison value table 13, the comparison is performed word by word using only one comparator. Therefore, if the PID has a multiple word length this is addressed by enlarging the comparison value table 13. Thus, differences in the word

length of the PID do not require a change in the circuit scale.

Figure 6 is a block diagram showing a configuration of a PID filter circuit according to another embodiment of the present invention. The PID filter circuit shown in Figure Figure 6 is compared with the PID filter circuit shown in Figure Figure 4. The PID filter circuit shown in Figure 6 is provided with two FIFO memories 11A and 11B that are controlled by the signal from the comparator 12 and that receive input packet data. A switch 14 directs the input packet data to either one of the FIFO memories 11A and 11B, and a switch 15 selects an opposite one of the FIFO memories 11A and 11B for providing output data. In this connection the PID filter circuit shown in Figure 6 differs from the PID filter circuit shown in Figure 4. The switches 14 and 15 are interlocked so as to select different FIFO memories mutually, and are controlled by the output signal of the comparator.

In this PID filter circuit, when the switch 14 selects the FIFO memory 11 A, the input packet data is written in the FIFO memory 11A, and at the same time the PID included therein is compared with a value from the comparison value table 13 by the comparator 12. Also at the same time, an output packet data is read out from the FIFO memory 11B, because the switch 15 selects the FIFO memory 11B. When the input packet data written in the FIFO memory 11B is necessary packet data, it causes the switches 14,15 to be reversed by the output signal of the comparator, thus permitting the data read out from the FIFO memory 11A to be outputted. When the input packet data written in the FIFO memory 11A is not desired packet data, it is superseded. Therefore, even if the packet data has a variable PID position, it is capable of being filtered by this circuit.

As described above, according to the present invention, a comparison value from the comparison value table is read out and used for comparison with the input packet data, therefore, even if the word length of the PID is long,

the comparison may be implemented by enlarging the comparison value table, and thus only one comparator is required. Therefore, even if the word length of the PID is long, little change to the circuit is required.

Furthermore, according to the present invention, input packet data remains within the FIFO memory until it is determined whether the input packet data is desired. The packet data is used if it is determined to be desired packet data, and is superseded if it is not determined to be desired packet data. Therefore, even if the position of the PID is variable within the packet data, filtering may be implemented without the need to change the circuit.

While preferred embodiments of the invention have been described using specific terms, such description is for illustrative purpose only, and it is to be understood that changes and variations may be made without departing from the spirit or scope of the following claims.

WHAT IS CLAIMED IS:

1. A FIFO circuit including a FIFO memory for storing input data, said FIFO memory comprising:

- a dual port memory for storing said input data;

- a write pointer for indicating a write address within said dual port memory;

- a read pointer for indicating a read address within said dual port memory;

- a write control section for controlling write operations of said dual port memory such that the value of said write pointer is incremented when a write operation is performed, and such that when there is received a control signal indicating that input data stored in the dual port memory is not desired data, the value of said write pointer is decremented in accordance with a quantity of the desired input data already stored in the dual port memory; and

- a read control section for controlling read operations of said dual port memory such that a read operation causes a value of said read pointer to be incremented, and such that read operations are not performed when a quantity of unread input data stored in the dual port memory is less than predetermined amount.

2. A FIFO circuit as claimed in claim 1, further comprising a subtracter for calculating a difference between a value of said write pointer and a value of said read pointer and providing said difference to said read control section as representing an unread data quantity within said dual port memory.

PID FILTER CIRCUIT AND FIFO CIRCUIT

Abstract

A PID (Packet Identifier) filter circuit includes a FIFO (First-in, First-out) memory. Filtering may be performed irrespective of the length of the PID and irrespective of whether the position of the PID is fixed in the packet. The circuit includes a comparison value table for storing therein comparison values and a comparator for taking comparison values successively from the comparison value table and for comparing value of the PID in the input packet data with the comparison values on a word by word basis. A FIFO memory stores input packet data. The FIFO memory does not implement a read operation until the input packet data is determined to contain desired data based on its PID. If the input packet data is determined not to contain desired data, any portion of the input packet data already stored in the FIFO is superseded.

Figure 4