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SPECIFICATION

TITLE OF THE INVENTION

Semiconductor device and its manufacturing method

BACKGROUNG OF THE INVENTION

This invention relates to the technique that is applied for a semiconductor device, especially for a semiconductor device with the base substrate that comprises flexible films.

As suitable semiconductor device for high-pin-count package, the semiconductor equipment of the BGA(BALL GRID ARRAY) structure has been developed. This semiconductor device of the BGA structure mounts a semiconductor chip on a chip mount area of a main surface of a base substrate by using adhesive material and has several bump electrodes positioned in an array to the side of the back that is opposed to said main surface of a base substrate.

The above base substrate is made of the rigid resin substrate that is impregnated glass fiber with for example, an epoxy resin, a polyimide resin, maleimide resin, etc.. Electrode pads for wire connection are arranged in a peripheral area that surrounds the periphery of the chip mount area of the main surface of the base substrate. And, several electrode pads for bump connection are arranged in the back of the base substrate. The bump electrodes comprise the solder materials of for example, the Pb-Sn composition, fix and connect to the electrode pads for bump connection electrically and

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mechanically.

The above semiconductor chip comprises the structure mainly of the semiconductor substrate that includes for example, monocrystal silicon. To the semiconductor chip, a logical circuit system, a storage circuit system or those mixture circuit systems are formed. And, several external terminals (bonding pad) are allocated to the main surface (element formation face) of the semiconductor chip. These external terminals are electrically connected to electrode pads for wire connection arranged on the main surface of the base substrate through wires.

The above semiconductor chip, the wires, the electrode pads for wire connection, etc. are sealed in the resin sealing body formed on the main surface of the base substrate. The resin sealing body is formed by the method of a transfer mold which is suitable for the mass production.

The semiconductor device of the BGA structure composed like this is mounted on the surface of a printed circuit board by the melting connection of the bump electrodes to the electrode pads formed on the surface of the printed circuit board.

And, it is stated in for example, the NIKKEI electronics (number on February 28, 1994, from the 111th page to the 117th page) of NIKKEI BP company publication about the semiconductor device of the above BGA structure.

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SUMMARY OF THE INVENTION

The semiconductor device of the BGA structure using a flexible film as a base substrate has been developed in recent years. The semiconductor device of this BGA structure can plan to make it thinner type, to make it high-pin-count package and to miniaturize it comparing with a semiconductor device using a rigid resin substrate as a base substrate. However, these inventors, etc. have found the following problems in developing semiconductor equipment using a flexible film as a base substrate.

The base substrate that comprises flexible films is generally made in the following process. First, a connection hole is formed to the bump connection area of a flexible film. Then, the metal foil that comprises of for example, copper (Cu) is attached to the one-sided surface of a flexible film through an adhesive material. Then, electric conductor layers that comprise electrode pads for bump connection, an electric conductor, an electrode pad for wire connection and an electric conductor for plating etc. is formed by doing patterning to the metal foil. Then, the insulation layer that protects the electric conductor layer is formed. Then, processing of plating to form a plating layer to the electrode pad for bump connection and wire connection is done. Plating processing is done by the method of electrolytic plating. This plating processing is sometimes done in the step before forming an insulation layer. The plating

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layer is formed on for example, gold (Au)/ nickel (Ni) film or the gold(Au)/ palladium (Pd)/nickel(Ni) film.

The above insulation layer is formed by following process for example. First, a photosensitive resin film is formed to the one-sided surface of a flexible film. Then, after doing baking processing, by using a photograph printing technique, processing of photosensitive processing, development processing and cleaning are done. The insulation layer is formed to almost all areas of the one-sided surface of the flexible film containing electric conductor layers except electrode pads for wire connection. That is, insulation layers are formed to almost all areas of the one-sided surface of the flexible film. Therefore, the warp and distortion, etc. arise in the base substrate. This deformation of a base substrate causes a transfer trouble in the manufacturing process (assembly process) of a semiconductor device. And, this deformation of a base substrate becomes a cause that in the process that mounts a semiconductor chip, the wetting performance of an adhesive material is deteriorated.

As for a deformation of the above base substrate, it is the main factor that the thermal expansion coefficient and the hardening shrinkage rate of an insulation layer are large. But in case an insulation layer is not formed, the following problems arise.

(1)Electrode pads for bump connection are arranged to the chip mount area of a main surface of a base substrate.

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Therefore, when mounting a semiconductor chip through the adhesive insulation material to the chip mount area of a main surface of the base substrate, it is difficult to control the thickness of an adhesive material. And, because a semiconductor chip touches electrode pads for bump connection, a short circuit arises between them.

(2)Electrode pads for bump connection are arranged to the chip mount area of the main surface of the base substrate. Bump electrodes arranged to the side of the back of a base substrate are connected to these electrode pads for bump connection through connection holes formed in the chip mount area of a base substrate. That is, bump electrodes are arranged in the area under a semiconductor chip.

The electrode pads for bump connection arranged to the chip mount area of the above base substrate are integrated and are electrically connected through electric conductors to the electrode pads for wire connection arranged to the peripheral area that surrounds the periphery of the chip mount area of the main surface of a base substrate. That is, in the peripheral area of the main surface of the base substrate, electric conductors are arranged to the area between a semiconductor chip and electrode pads for wire connection. Therefore, when connecting the external terminals of a semiconductor chip and pads for wire connection with wires, other electric conductors that adjoin electric conductors electrically connected to the

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wires and these wires sometimes cross themselves. In case it sufficiently has the height of a wire connection, it is no problem. However, there is some possibility of causation of a short circuit with wires and other electric conductors, when wires and other electric conductors do not become parallel at the corner of a semiconductor chip. And, it has possibility that in case wires and other electric conductors cross each other on the side of electrode pads for wire connection, a short circuit with wires and other electric conductors also arise.

It is an object of the present invention to provide a technique that is possible to suppress a deformation (warp and distortion) of a base substrate in the semiconductor device with the base substrate that comprises flexible films.

It is another object of the present invention to provide a technique that is possible to suppress a deformation of a base substrate in the semiconductor device with the base substrate that comprises flexible films and to prevent a short circuit with the electric conductors of the base substrate and the semiconductor chip.

It is another object of the present invention to provide a technique, in the semiconductor device with the base substrate that comprises of flexible films, that is possible to suppress a deformation of a base substrate and to prevent the electric conductor layer of a base substrate and wires from short-circuiting.

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These and other objects, features and advantages of the invention will become more apparent upon a reading of the following description and appended drawings.

Summary of the invention disclosed in this application is explained as follows.

(1)Semiconductor device that arranged electric conductor layers in a main surface of a base substrate that comprises flexible films and mounted a semiconductor chip by using a adhesive material on the above main surface of a base substrate. And insulation layers are portioned into block construction on said electric conductor layers of the main surface of the base substrate. Insulation layers are portioned into block construction for example, every electric conductor layers.

(2)Semiconductor device that arranged electric conductor layers in a chip mount area of a main surface of a base substrate that comprises flexible films and mounted a semiconductor chip by using an adhesive material on the above chip mount area of a main surface of a base substrate. And insulation layers are portioned into block construction on said electric conductor layers of the main surface of the base substrate. Insulation layers are portioned into block construction for example, every electric conductor layers.

(3) Semiconductor device that arranged a semiconductor chip in a chip mount area of a main surface of base substrate

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being made of flexible film by using an adhesive material. Electrode pads for wire connection formed in a peripheral area that surrounds said chip mount area. Electric conductors being arranged between said semiconductor chip and said electrode pads for wire connection in said peripheral area. External terminals of said semiconductor chip and said electrode pads for wire connection are electrically connected through wires. And insulation layers are portioned into block construction on said electric conductors.

By means of (1) mentioned above, as a stress by contraction of expansion and hardening of an insulation film is relieved, a deformation (warp and distortion) of a base substrate can be suppressed.

By means of (2) mentioned above, as a semiconductor chip does not touch electric conductor layers, when a semiconductor chip is mounted on the chip mount area of the main surface of the base substrate by using an adhesive material, a short circuit with electric conductor layers and a semiconductor chip can be prevented.

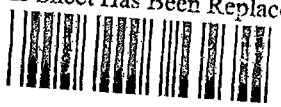
By means of (3) mentioned above, as wires do not touch electric conductors, the electric conductor of a base substrate and the wires can be prevented from short-circuiting.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is the plan view of a semiconductor device that is

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one embodiment of this invention;

Fig. 2 is an enlarged sectional view cut at the position of the A-A line that is shown in Fig. 1;

Fig. 3 is the main part enlarged sectional view of Fig. 2;

Fig. 4 is the plan view of a state that the resin sealing body of the above semiconductor device was removed;

Fig. 5 is the plan view of a base substrate;

Fig. 6 is the main part enlarged sectional view of the above semiconductor device;

Fig. 7 is the main part plan view of the frame structure that is used in the manufacturing process of the above semiconductor device;

Fig. 8 is an enlarged sectional view cut at the position of the B-B line that is shown in Fig. 7;

Fig. 9 is a main part cross-sectional view to explain a method of manufacturing the above frame structure;

Fig.10 is a main part cross-sectional view to explain a method of manufacturing the above frame structure.

Fig. 11 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device;

Fig. 12 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device.

Fig. 13 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device.

Fig. 14 is a main cross-sectional view to explain a method

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of manufacturing the above semiconductor device.

Fig. 15 is a main part plan view to explain a method of manufacturing the above semiconductor device.

Fig. 16 is a main part plan view to explain a method of manufacturing the above semiconductor device;

Fig. 17 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device;

Fig. 18 is the outline structure figure that shows a state that the above frame structure was stacked to the multisteps;

Fig. 19 is a main part cross-sectional view to explain a method of manufacturing the above frame structure;

Fig. 20 is a main part cross-sectional view to explain a method of manufacturing the above frame structure;

Fig. 21 is a main part cross-sectional view that shows the first formation example of a semiconductor device that is one embodiment of this invention.

Fig. 22 is the plan view of the base substrate that shows the first formation example of a semiconductor device that is one embodiment of this invention.

Fig. 23 is the plan view of the base substrate that shows the second formation example of a semiconductor device that is one embodiment of this invention.

Fig. 24 is the main part cross-sectional view of a semiconductor device using the base substrate that is shown in Fig. 23.

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Fig. 25 is the plan view of the base substrate that shows the third formation example of a semiconductor device that is one embodiment of this invention.

Fig. 26 is the plan view of the base substrate that shows the fourth formation example of a semiconductor device that is one embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As follows, it is explained with an embodiment of this invention applying for the semiconductor device of the BGA structure. And, the same code is put on the thing that has the same function in several drawings to explain an embodiment, and an explanation of its repeat is omitted.

Fig. 1 is a plan view of a semiconductor device that is one embodiment of this invention. Fig. 2 shows an enlarged sectional view cut at the position of the A-A line that is shown in Fig. 1. Fig. 3 is an enlarged sectional view of an essential part of Fig. 2. Fig. 4 is a plan view of a state that a resin sealing body was removed. Fig. 5 is a plan view of a base substrate. Fig. 6 is an enlarged sectional view of an essential part of the above semiconductor device.

As it is shown in Fig. 1, Fig. 2 and Fig. 3, the semiconductor device becomes the following structure. Semiconductor chip 10 is mounted by using adhesive material 12 on the chip mount area of a main surface of base substrate

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1. And several bump electrodes 15 are positioned in an array to the side of the back that is opposed to the main surface of base substrate 1. Bump electrodes 15 are formed in the solder material of for example, 63 weight % Pb-37 weight % Sn composition. The semiconductor device of this embodiment is a surface-mounted type BGA(Ball Grid Array) package and it is called as the CSP(CHIP SIZE PACKAGE) which has a chip mounting area almost equal to the size of the semiconductor chip.

The plane shape of above base substrate 1 is formed in the square-form. This base substrate 1 is made of flexible film that comprises the insulation resins of for example, epoxy system or the insulation resin of a polyimide system. Base substrate 1 is set at the thickness of 50 micron [μ M] of for example.

The electric conductor layers that comprise electrode pads 2 (bump land) for bump connections, electric conductors 3 and electrode pads 4 for wire connection, electric conductors 5 for plating, etc. are arranged on the main surface of above base substrate 1. Several electrode pads 2 for bump connection and electrode pads 4 for wire connection are provided, and several electric conductors 3 and electric conductors 5 for plating are provided. That is, several electric conductor layers are arranged on the main surface of base substrate 1. Electrode pads 2 for bump connection are integrated with electrode pads 4 for wire connection through electric conductors 3 and are

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electrically connected each other. Electric conductors 5 for plating are integrated with electrode pads 4 for wire connection and are electrically connected each other. Electrode pad 2 for bump connection, electric conductors 3 , electrode pads 4 for wire connection and electric conductors 5 for plating etc. are formed by doing etching processing on a metal foil after sticking metal foil, for example, the Cupper(Cu) foil to main surface of a flexible film by using adhesive materials. These electrode pads 2 for bump connection and electric conductors 3, electrode pads 4 for wire connection and electric conductors 5 for plating are set at the thickness of 18 micron [μ Ms] for example.

The plane shape of above semiconductor chip 10 is formed in the square-form. This semiconductor chip 10 becomes structure mainly of the semiconductor substrate that comprises for example, monocrystal silicon. To semiconductor chip 10, a logical circuit system, a storage circuit system or those mixture circuit systems are formed. These circuit systems are formed by connecting several semiconductor elements formed to the side of main surface (element formation face) 10A of semiconductor chip 10 through the electric conductors.

Several external terminals (bonding pad) 11 arranged along each side of semiconductor chip 10 are arranged on main surface 10A of above semiconductor chip 10. Each of this several external terminals 11 are formed to the top layer of

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electric conductor layers formed on the main surface of the semiconductor substrate, and are made of for example, aluminum (Al) film or an aluminum alloy film. And, each of several external terminals 11 are electrically connected to circuit systems formed to semiconductor chip 10.

A great part of above several electrode pads 2 for bump connection are arranged in the chip mount area of the main surface of base substrate 1. Other (remainder) electrode pads 2 for bump connection are arranged to the peripheral area that surrounds the periphery of the chip mount area of the main surface of base substrate 1. Several bump electrodes 15 arranged to the side of the back of base substrate 1 fix on the back of each of these several electrode pads 2 for bump connection through connection holes 6 formed in base substrate 1, and they are connected electrically and mechanically. And, in this embodiment, the plane shape of electrode pads 2 for bump connection are formed in the circle-form.

As it is shown in Fig. 2, Fig. 3 and Fig. 4, each of said electrode pads 4 for wire connection are arranged to the peripheral area of main surface of base substrate 1 and are arranged along each side of semiconductor chip 10. Each of electrode pads 4 for wire connection are electrically connected to each of several external terminals 11 arranged on main face 10A of semiconductor chip 10 through wires 13. For example, the Au wires are used as wires 13. Wires 13 are connected by

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the method of bonding that used an ultrasonic in combination with thermo compression bonding for example.

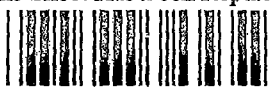
Electric conductors 3 integrated with electrode pads 2 for bump connection arranged to the chip mount area of main surface of base substrate 1 exist and extend in the chip mount area and the peripheral area of main surface of base substrate 1. And, electric conductors 3 integrated with electrode pads 2 for bump connection arranged to the peripheral area of main surface of base substrate 1 exist and extend in the peripheral area of main surface of base substrate 1. That is, in the peripheral area of main surface of base substrate 1, electric conductors 3 are arranged to the area between semiconductor chip 1 and electrode pads 4 for wire connection.

Above semiconductor chip 10, electric conductors 3, electrode pads 4 for wire connection and wires 13, etc. are sealed in resin sealing body 14. Resin sealing body 14 is formed in the resin of an epoxy system to which for example, phenol system hardener, silicone rubber and a filler were added for the purpose of planning a lower stress. Resin sealing body 14 is formed by the method of a transfer mold suitable for the mass production. The transfer molding method uses a molded die assembly with a pot, a runner, a gate, a cavity, etc.. And it is a method of injecting a resin in the cavity through a runner and a gate from the pot and forming a resin sealing body.

Each of electric conductors 5 for plating is arranged

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outside electrode pads 4 for wire connection in the peripheral area of 1 surface of base substrate 1. Each of these electric conductors 5 for plating are arranged along each side of semiconductor chip 10. A part of electric conductors 5 for plating are arranged to the inside of resin sealing body 14, and other parts are arranged to the outside of the resin sealing body.

As it is shown in Fig. 2, Fig. 3 and Fig. 5, insulation layers 9 are arranged to the over surface of each of several electrode pads 2 for bump connection arranged to the chip mount area of main surface of above base substrate 1. These insulation layers 9 are divided and arranged for every electrode pads 2 for bump connection in the chip mount area of main surface of base substrate 1. Insulation layers 9 are divided into several part so that it is scattered in the chip mount area of main surface of base substrate 1. That is, the semiconductor device of this embodiment divides insulation layers 9 into several parts in the chip mount area of main surface of base substrate 1 and arranges this divided insulation layer 9 on electrode pads 2 for bump connection. And, the plane shape of insulation layer 9 arranged on electrode pads 2 for bump connection in the embodiment is formed in the circle-form.

On the over surface of each of electric conductors 5 for plating arranged to the peripheral area of one surface of above base substrate 1, insulation layers 9 are arranged. These

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insulation layers 9 exist and extend along each side of base substrate 1 and are divided into every side of base substrate 1. Insulation layers 9 are divided into several to dot in the peripheral area of base substrate 1. That is, the semiconductor device of this embodiment divides insulation layer 9 into several in the peripheral area of one surface of base substrate 1 and is arranging these insulation layers 9 on electric conductors 5 for plating.

The part of insulation layers 9 arranged on above electric conductors 5 for plating are arranged to the inside of resin sealing body 14, and other parts are arranged outside resin sealing body 14. That is, insulation layers 9 lie between electric conductors 5 for plating and resin sealing body 14.

As it is shown in Fig. 5 and Fig. 6, vent hole 7 is provided in the chip mount area of above base substrate 1. Like this, by providing vent hole 7 in the chip mount area of base substrate 1, the out gas that occurs at the time of hardening of adhesive material 12 when applying adhesive material 12 on the chip mount area of one surface of base substrate 1 and mounting semiconductor chip 10 on it can be emitted to the outside. And, the steam that occurs in adhesive material 12 by the heat at the time of surface-mounting that mounts a semiconductor device on the surface of a mounting substrate or the heat at the time of a temperature cycle test that is an environmental test after product completion of a semiconductor device can be

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emitted to the outside.

On the chip mount area of main surface of above base substrate 1, dam 8 that surrounds the periphery of vent hole 7 is built. Dam 8 of this embodiment is composed of conduction film 8A and insulation layers 9 arranged on the conduction film 8A.

Above vent hole 7 is arranged to the position that deviated from center line P1 of the X direction (horizontal direction in the figure) of base substrate 1 and center line P2 of the Y direction (vertical direction in the figure) of base substrate 1 as it is shown in Fig. 5. That is, vent hole 7 is arranged to the position that deviated from the center of base substrate 1. In case a semiconductor device is looked at from the side of the back of base substrate 1, like this, the arrangement to the position that deviated from the center of base substrate 1 of vent hole 7 can clear a direction as an index. And, because a direction can be cleared as an index, vent hole 7 can be used as an index.

Then, the frame structure that is used in the manufacturing process of the above semiconductor device is explained.

While frame structure 20 is not limited to this, it is composed of the matrix frame structure that arranged unidirectionally several areas specified in for example, frame body 21 like the indication in Fig. 7(main part plan view).Film

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base material 1A is arranged in each area specified in frame body 21. Film base material 1A of this embodiment prepares four(4) resin sealing areas 22. That is, film base material 1A to form four(4) products in each area specified in frame body 21 is arranged. And, the electric conductor layer pattern that is shown in Fig. 5 to resin sealing area 22 is formed.

Above frame body 21 is formed by doing manufacture of etching manufacture or press punching on a board material. The thing that comprises for example, the Cu system alloy materials is used as a board material.

As it is shown in Fig. 7 and Fig. 8 (cross-sectional view cut at the position of the B-B line that is shown in Fig. 7), the above film base material 1A is fixed to two(2) portions of adhesion area where parts of frame body 21 is opposed each other by using adhesive material. Slit 23 is prepared in the adhesion area of each of frame body 21. This slit 23 puts a specified space on the longitudinal direction of frame structure 20, and several are arranged. Like this, by preparing slit 23 in the adhesion area of frame body 21, because a stress by difference between the materials of frame body 21 and film base material 1A can be relieved, transformation of a warp, distortion, etc. of film base material 1A can be suppressed.

Then, a method of manufacturing above frame structure 20 is explained by using Fig. 9 and Fig. 10 (main part cross-sectional view to explain a manufacturing method).

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First, as it is shown in Fig. 9-(A), film base material 1A is prepared. Film base material 1A is made of the insulation resin of for example, epoxy system or the insulation resin of a polyimide system. Then, as it is shown in Fig. 9-(B), adhesive material 30 is attached to the side of one surface of above film base material 1A. It can be attached by a heat pressurization without using adhesive material 30.

Then, while connection hole 6 is being formed to the bump connection area of above film base material 1A, as it is shown in Fig. 9-(C), and vent hole 7 is formed to the chip mount area of film base material 1A, it is not being illustrated. Connection hole 6 and vent hole 7 are formed by for example, die assembly, laser manufacture, etc.. Then, as it is shown in Fig. 9-(D), metal foil (the Cu foil for example) 31 is attached to the side of one surface of above film base material 1A through connection material 30. After attaching metal foil 31 to film base material 1A, connection hole 6 and vent hole 7 can be formed by a die assembly or laser manufacture, etc.

Then while electrode pads 2 for bump connection are formed on one surface of film base material 1A, as patterning is done on above metal foil 31 and is shown in Fig. 9-(E), and electric conductors 3 and electrode pads 4, electric conductors 5, etc. for plating for wire connection are formed, it is not being illustrated. That is, a electric conductor layer pattern is formed in this process. And, conduction film 8A that also surrounds the

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periphery of vent hole 7 in the chip mount area of one surface of film base material 1A is formed, it is not being illustrated also.

Then as it is shown in Fig. 10-(F), photosensitive resin film 32 of a uniform film thickness is formed to the whole surface on film base material 1A including the above electric conductor layer pattern. After applying a photosensitive resin, photosensitive resin film 32 is formed by the method of screen printing. Then, after doing baking processing, a photograph printing technique, that is, processing of photosensitive processing, development processing and cleaning, etc. are done, and as it is shown in Fig. 10-(G), insulation layer 9 of a specified pattern is formed. In this process, as it is shown in Fig. 5, insulation layers 9 divided into several are arranged on the electric conductor layers. And, dam 8 that also comprises insulation layers 9 arranged on conduction film 8A and this conduction film 8A in this process also is formed. In case insulation layers 9 are arranged to the whole surface on film base material 1A, by difference between material characteristics such as film base material 1A, electric conductor layers and insulation layers 9, it warps in base substrate 1, and transformation of a distortion, etc. arises. But by dividing and arranging insulation layers 9 like this embodiment, a deformation of base substrate 1 can be suppressed because that a stress by shrinkage of expansion and hardening of insulation layers 9 are relieved.

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Then, the plating layer (for example, the Au/Ni layer, the Au/Pd/Ni, Pd/Ni layer and the Sn/Ni layer, etc.) that is possible to be bonded is formed by the plating processing by the method of electrolytic plating is formed on the electric conductor layer which is not covered by said insulation layers. The frame structure that is shown in Fig. 7 is formed after this by cutting film base material 1A an individual piece and attaching it to the adhesion area of frame body 21 by using adhesive material 24. A transfer of film base material 1A in the manufacturing process (assembly process) of a semiconductor device improves, and formation of frame structure 20 that has film base material 1A to the area specified in frame body 21 like this that attached film base material 1A to the adhesion area of frame body 21 improves handling.

Then, a method of manufacturing the above semiconductor device is explained.

First, frame structure 20 that is shown in Fig. 7 is prepared. Frame structure 20 has film base material 1A in the area specified in frame body 21. Resin sealing area 22 is arranged to film base material 1A, and the electric conductor layer pattern that is shown in Fig. 5 is formed to this resin sealing area 22.

Then, a semiconductor chip 10 is mounted through adhesive material 12 on the chip mount area of main surface of above film base material 1A, as it is shown in Fig. 11 (main part cross-

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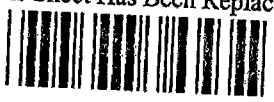
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sectional view). Adhesive material 12 is supplied to the chip mount area of one surface of film substrate 1A by the multi-point potting method. The heat curable insulation resin of for example, epoxy system or a polyimide system is used as adhesive material 12. And as an adhesive material 12, the thermoplastic insulation resin of for example, epoxy system or polyimide system is also fine. Out gas that occurs at the time of hardening of adhesive material 12 because vent hole 7 that is shown in Fig. 6 is provided to the chip mount area of film base material 1A in this process can be set free in the outside. And, the inflow to vent hole 7 of adhesive material 12 because of building dam 8 that surrounds the periphery of vent hole 7 that is shown in Fig. 6 on the chip mount area of one surface of film base material 12 can be stemmed and can be stopped. Therefore, the prevention of a blockage of vent hole 7 by adhesive material 12 and the going round inwardly of adhesive material 12 to the side of the back of film base material 1A can be prevented. And, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, semiconductor chip 10 does not touch electrode pads 2 for bump connection because insulation layers 9 are arranged on electrode pads 2 for bump connection. And, even if it is mounted in the state that semiconductor chip 10 tilted and the film thickness of adhesive material 12 thins, semiconductor chip 10 touches insulation layers 9 and semiconductor chip 10 does not touch electric

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conductors 3 because it is supported by this insulation layers 9.

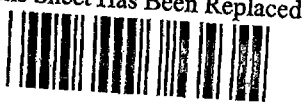
Then, as it is shown in Fig. 12 (main part cross-sectional view), external terminal 11 of above semiconductor chip 10 and electrode pads 4 for wire connection of film component 1A are electrically connected with wires 13. The Au wires are used as wires 13.

Then, above frame structure 20 is set to a molding die assembly. As it is shown in Fig. 13 (main part cross-sectional view), resin sealing area 22, semiconductor chip 10, wires 13, etc. of film base material 1A are arranged in cavity 36 that is formed in upper die 35A and lower die 35B of a molding die assembly. As it is shown in Fig. 14 (main part cross-sectional view), the molding die assembly prepares sub-runner (trunk runner) 37 and protrusion 38, and further, it is not being illustrated , each of an inflow gate, the main runner (main runner) and a pot are arranged. The pot is connected to cavity 36 through each of the main runner, sub-runner 37 and an inflow gate.

The lower die 35B of the above molding die assembly has stepped portion 39 in which frame body 21 of frame structure 20 is installed and stepped portion 40 in which film base material 1A is installed. That is, frame body 21 of frame structure 20 is installed in stepped portion 39 of lower die 35B, and film base material 1A of frame structure 20 is installed in stepped portion 40 of lower die 35B. Vertical matching of upper die 35A and lower

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die 35B is done in the structure of frame body 21- adhesive material 24- film base material 1A.

While it is not being in detail illustrated, above sub-runner 37 crosses stepped portion 39 in which frame body 21 of frame structure 20 is installed and stepped portion 40 in which film base material 1A is installed and exists from the outside of frame structure 20 to inside of it and connects to the cavity 36 through the inflow gate. The above main runner exists and extends along the longitudinal direction of frame structure 20 outside of it and connects to the one end of said sub-runner 37 withdrawn outside frame structure 20. And, protrusion 38 is provided for ease cutting of a resin stiffened in the inside of sub-runner 37. This protrusion 38 is positioned on the area of the stepped portion that is formed in frame body 21 of frame structure 20 and film base material 1A.

Then a resin tablet is put into the above pot. This resin tablet is pressurized in the plunger of transfer mold equipment, and a resin is supplied in cavity 36 through each of the main runner, sub-runner 37 and an inflow gate from the pot. Thus, resin sealing body 14 is formed. After this, frame structure 20 is taken out from the molding die assembly. The state of frame structure 20 unloaded from a molded die assembly is shown in Fig. 15 (main part plan view). In Fig. 15, code 41 is a sub-runner resin stiffened in sub-runner 37 of a molding die assembly, and code 42 is main-runner resin 42 stiffened in the inside of

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main-runner of a molding die assembly. Main-runner resin 42 is existing along the longitudinal direction of frame structure 20. Sub-runner resin 41 is existing from the outside of frame body 21 to the inside of it. And Fig. 14 shows a cross-sectional view at the position of the C-C line that is shown in Fig. 15 .

Then, sub-runner stiffened resin 41 and main runner stiffened resin 42 that is in the outside above frame body 21 are removed. Sub-runner resin 41 that is in the inside of above frame body 21is left. This state is shown in Fig. 16 (main part plan view).

Then, as it is shown in Fig. 17, bump electrodes 15 are connected to the back of electrode pads 2 for bump connection passing through connection holes 6 formed in film base material 1A. Bump electrodes 15 are supplied by carrying ball on the substrate for example, and is connected by melting in the infrared ray reflow, etc.. A transfer state after forming bump electrodes 15 is shown in Fig. 18 (outline structure figure). In case frame structure 20 is stacked to the several steps, a space between frame structure 20 of an upper step and a lower step can be secured in sub-runner stiffened resin 41 provided in frame structure 20 of an upper step. Therefore, bump electrodes 15 of a semiconductor device manufactured in frame structure 20 of a lower step can be protected. Because it can carry in the state that frame structure 20 was stacked to the several steps, a transfer of frame structure 20 improves. And, production rationality in

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the manufacturing process of a semiconductor device improves.

Then, the cutting to the specified shape (base substrate shape) of film base material 1A almost completes a semiconductor device with base substrate 1 that comprises film base materials 1A. The semiconductor device is shipped as a product after this. The semiconductor device shipped as a product is installed on the surface of printed circuit board.

And, bump electrodes 15 can be connected in the state of an individual piece by cutting film base material 1A after forming resin sealing body 14.

And, plating processing can go in the step before forming insulation layers 9. In case plating processing is done in the step after forming insulation layers 9 like this embodiment, as it is shown in Fig. 19 (main part cross-sectional view), plating layers 33 are formed on electrode pads 2 for bump connection, electric conductors 3 and electrode pads 4 for wire connection arranged to the peripheral area of main surface of base substrate (film base material 1A) 1 and to the back of electrode pads 2 for bump connection. That is, plating layers 33 are not formed between a electric conductor layers and insulation layers 9. In case plating processing is done in the step before forming insulation layers 9, as it is shown in Fig. 20 (main part cross-sectional view), plating layers 33 are formed on the electrode pads 2 for bump connection , electric conductors 3, electrode pads 4 for wire connection, electric conductors 5 for plating arranged to the

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periphery of the chip mount area of main surface of base substrate (film base material 1A) 1, and to the back of electrode pads 2 for bump connection. That is, plating layers 33 are formed between electric conductor layers and insulation layers 9.

As it was explained above, according to this embodiment, the following effects are obtained.

(1)By dividing and arranging insulation layers 9 on the electric conductor layers, because a stress by shrinkage of expansion and hardening of insulation layers 9 are relieved, transformation of a warp, distortion, etc. of base substrate (film base material 1A) 1 can be suppressed.

And, because a deformation of base substrate 1 can be suppressed, the yield in the manufacturing process of a semiconductor device improves.

(2)By building dam 8 that surrounds the periphery of vent hole 7, the inflow to vent hole 7 of adhesive material 12 can be stemmed and can be stopped. As a result the prevention of a blockage of vent hole 7 by adhesive material 12 and the going round inwardly of adhesive material 12 to the side of the back of film base material 1A can be prevented.

(3)In case a semiconductor device is looked at from the side of the back of base substrate 1, the arrangement of vent hole 7 to the position that deviated from the center of base substrate 1 can clear a direction as an index.

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(4)By forming insulation layers 9 by the method of printing, low cost of a semiconductor device can be planned as compared with a case that insulation layers 9 formed to the sheet-form is attached and is formed,.

And production rationality of a semiconductor device improves because the pattern shape of insulation layers 9 can be set at freedom.

(5)By using frame structure 20 that film base material 1A was arranged in the area specified in frame body 21, a transfer of film base material 1A in the manufacturing process of a semiconductor device improves, and handling of the manufacturing of a semiconductor device improves.

(6) An alien substance that occurs at the time of sealing and cutting can be reduced by the formation of resin sealing body 14 in the transfer molding method using a molding die assembly with stepped portion 39 that frame body 21 of frame structure 20 is installed and stepped portion 40 that film base material 1A of frame structure 20 is installed in a sub-runner path, because the resin burr that adheres to film base material 1A and frame body 21 can be prevented.

(7)In the state that there is runner resin 41 in frame body 21 of frame structure 20, bump electrodes 15 are connected. In case from this, frame structure 20 is stacked to the multisteps, a protection can be done for bump electrodes 15 of a semiconductor device formed in frame structure 20 of a lower

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position because of the sub-runner resin 41 that is in frame structure 20 of an upper position can keep a space between frame structure 20 of an upper case and frame structure 20 of a lower position. Therefore, a transfer of frame structure 20 improves because it can carry in the state that frame structure 20 was stacked to the multisteps. And, production rationality in the manufacturing process of a semiconductor device improves.

(8)Because insulation layers 9 are arranged on electrode pads 2 for bump connection, when intercalating adhesive material 12 on the chip mount area of main surface of base substrate (film base material 1A) 1 and mounting semiconductor chip 10, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, semiconductor chip 10 does not touch electrode pads 2 for bump connection. Therefore, a short circuit with electrode pads 2 for bump connection and semiconductor chip 10 is prevented, that is, a short circuit with electric conductor layers and semiconductor chip 10 can be also prevented.

And, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, semiconductor chip 10 touches insulation layers 9 and supports it by this insulation layers 9. As a result, a short circuit with electric conductors 3 and semiconductor chip 10 is prevented, that is, a short circuit with electric conductor layers and semiconductor chip 10 can be prevented.

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(9) Transformation of a warp, distortion, etc. of film base material 1A can be suppressed by preparing slit 23 in the adhesion area of frame body 21, because a stress by difference between the materials of frame body 21 and film base material 1A can be reduced.

And, while in the above embodiment, an example of forming insulation layers 9 on electrode pads 2 for bump connection in the chip mount area of base substrate 1 was explained, insulation layers 9 can be formed on electric conductors 3. And, insulation layers 9 can be formed on electrode pads 2 for bump connection and on electric conductors 3. In case of these, when intercalating adhesive material 12 on the chip mount area of main surface of base substrate (film base material 1A) 1 and mounting semiconductor chip 10, likewise with the above embodiment, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, a short circuit with electrode pads 2 for bump connection and an electric conductors 3 can be prevented, that is, a short circuit with electric conductor layers and semiconductor chip 10 can be prevented.

And, as it is shown in Fig. 21 (main part cross-sectional view of a semiconductor device) and Fig. 22 (plan view of a base substrate), insulation layers 9 can be divided into several on base substrate 1 to arrange insulation layers 9 on electric conductors 3 that was the peripheral area of main surface of base

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substrate 1 and was formed to the area between semiconductor chip 10 and electrode pads 4 for wire connection. In this case, because wires 13 do not touch to electric conductors 3, a short circuit with other electric conductors 3 that adjoin electric conductors 3 electrically connected to wires 13 and these wire 13 can be prevented, that is, electric conductor layers and wires 13 can be prevented from short-circuiting.

And, as it is shown in Fig. 23 (plan view of a base substrate) and Fig. 24 (main part cross-sectional view of a semiconductor device), insulation layers 9 are divided into every electric conductor layers on base substrate 1. And then, insulation layers 9 can be formed to all areas of electric conductor layers (electrode pads 2 for bump connection, electric conductors 3 and electric conductors 5 for plating) except electrode pads 4 for wire connection. In this case, even if a conductive foreign material adheres between electric conductor layers in the manufacturing process of a semiconductor device, a short circuit between electric conductor layers can be prevented because a conductive foreign material does not touch a electric conductor layers.

And, as it is shown in Fig. 25 (plan view of a base substrate) insulation layers 9 can be divided into several on base substrate 1, and this divided insulation layers 9 can be arranged on the electric conductor layers. As for each of several insulation layers 9, a plane is formed in the square-form, a specified space is put, and a matrix-form arranges it.

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And, as it is shown in Fig. 26 (plan view of a base substrate), insulation layers 9 can be divided into several on base substrate 1, and this divided insulation layers 9 can be arranged on the electric conductor layers. Each of several insulation layers 9 is formed to the long plate form and is radially arranged in the state that a specified space was put.

And, even though a spherical bump electrode 15 was explained as an example electrode that is arranged to the side of the back of base substrate 1 while in the above embodiment, as an electrode of this invention, a protruding portion electrode like a stud bump or even electrode that is formed by the method of ball bonding can be used.

While this invention was concretely explained on the basis of the above embodiment, this invention is not limited to the above embodiment only, and it is possible to change it variously in the range that does not deviate from the gist of the invention.

If the effect that is obtained by a representative in the invention that is disclosed in this application is easily explained as follows.

In the semiconductor device with the base substrate that comprises of flexible films, a deformation (warp and distortion) of a base substrate can be suppressed.

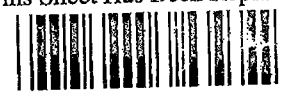
In the semiconductor device with the base substrate that comprises of flexible films, a deformation of a base substrate can be suppressed and a short circuit with the electric conductor of

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a base substrate and a semiconductor chip can be prevented.

In the semiconductor device with the base substrate that comprises of flexible films, a deformation of a base substrate can be suppressed and the electric conductor layers of a base substrate and wires can be prevented from short-circuiting.

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What is claimed is;

1. A semiconductor device comprising : /

a film substrate having a first surface and a second surface that is opposed on the first surface ;

a plurality of electric conductor layers formed on the first surface of said substrate;

a semiconductor chip mounted through an adhesive material on the first surface of said substrate and arranged on said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers;

a resin member formed on said first surface and sealing said semiconductor chip, said electric conductor layers and said bonding wires;

an insulation layer formed between said electric conductor layers and said semiconductor chip;

wherein said insulation layer has plural parts which are separated each other in a plane view in the area on which said

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semiconductor chip is mounted.

2.A semiconductor device according to claim 1, wherein said substrate comprises a flexible film.

3.A semiconductor device according to claim 1, wherein said substrate has a plurality of connection holes that reache said second surface from said first surface at the position that corresponds to the under area of said electric conductor layers, and wherein said bump electrodes are connected to said electric conductor layers through said connection holes.

4.A semiconductor device according to claim 1, wherein each of said electric conductor layers having a first part that is positioned in the area under said semiconductor chip and a second part that is positioned in the area outside of said semiconductor chip, the second part begin continuously formed with said first part, and wherein said bonding wires are connected to the second parts of said electric conductor layers.

5.A semiconductor device according to claim 1, wherein said insulation layer comprises a photosensitive resin film.

6.A semiconductor device comprising :

a film substrate having a first surface and a second

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surface that is opposed on the first surface ;

a semiconductor chip mounted through an adhesive material on the first surface of said substrate, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main face;

a plurality of electric conductor layers formed on said first surface of said substrate, and formed between said semiconductor chip and said substrate;

each of said electric conductor layers having a first part that is positioned in the area under said semiconductor chip and a second part that is positioned in the area outside of said semiconductor chip, the second part being continuously formed with said first part, and the first part having bump land at the one end;

a plurality of bonding wires to which the second parts of said electric conductor layers and said external terminals are electrically connected;

a plurality of bump electrodes arranged on said second surface and electrically connected to said electric conductor layers;

said substrate having a plurality of connection holes that reach said second surface from said first surface at the position that corresponds to said bump lands of electric conductor layers, said bump electrode being connected to said bump lands

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through said connection holes;

a resin member formed on said first surface and sealing said semiconductor chip, said electric conductor layers and said bonding wires;

a plurality of insulation layer patterns formed between said semiconductor chip and each of bump lands of electric conductor layers;

wherein said insulation layer patterns are separated each other in a plane view.

7.A semiconductor device according to claim 6 , wherein said substrate comprises a flexible film.

8.A semiconductor device according to claim 7 , wherein each of said insulation layer patterns comprises a photosensitive resin film.

9.A semiconductor device having a semiconductor chip mounted through an adhesive material on a surface of a flexible film that the plural number of electric conductor layer is arranged to a main surface of a base substrate composed of the flexible film,

wherein said semiconductor chip is mounted on said plural number of electric conductor layer,

an insulation layer is formed between said plural number

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of electric conductor layer and said semiconductor chip,

said insulation layer is divided into the plural number of part in the area under said semiconductor chip.

10.A semiconductor device having a semiconductor chip mounted through an adhesive material on the chip mount area of the main surface of a base substrate in which a vent hole is formed to the chip mount area of the main surface of a base substrate composed of flexible films,

wherein a dam that surrounds the periphery of said vent hole is formed in the chip mount area of said main surface of a base substrate.

11.A semiconductor device according to claim 10,

wherein said vent hole is arranged to the position that deviated from the center of said base substrate.

12.A semiconductor device according to claim 10,

wherein said adhesive material comprises thermo hardening resins.

13.A method for manufacturing a semiconductor device comprising the steps of:

A) preparing a lead frame made of metal that supplies the

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plural number of area partitioned by a frame body.

B) supplying film substrate to said plural number of area, said substrate has first surface, second surface that is opposed on said first surface and the plural number of electric conductor layer formed on the first surface;

C) mounting a semiconductor chip through an adhesive material on the first surface of said plural number of substrate, this semiconductor chip has the plural number of semiconductor element and the plural number of outside terminal formed on its main surface and is mounted on said plural number of electric conductor layer.

D) electrically connecting the plural number of outside terminal of said semiconductor chip and said plural number of electric conductor layer by using the plural number of wire.

E) sealing said semiconductor chip, said plural number of electric conductor layer and said plural number of wire by resin.

F) forming the plural number of bump electrode on the second surface of said substrate.

14.A method for manufacturing a semiconductor device according to claim 13, further comprising the step for cutting said lead frame made of metal to said plural number of area in order to form the plural number of resin molded semiconductor package after said step F).

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15.A method for manufacturing a semiconductor device according to claim 13,

wherein said step E) comprises a transfer mold using a die assembly and further including a step for leaving a stiffened runner resin positioned inside of said frame body and removing stiffened runner resin positioned outside of said frame body.

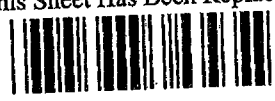
16. A method for manufacturing a semiconductor device according to claim 13,

wherein said step B) includes a step for fixing said substrate to the frame body of a lead frame made of metal by an adhesive material.

17. A method for manufacturing a semiconductor device according to claim 16,

wherein said frame body having slits in the adhesion area of said frame body and said substrate.

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ABSTRACT OF THE DISCLOSURE

Ball Grid Array type semiconductor package is disclosed. A semiconductor chip is mounted through an adhesive material on a surface of a flexible film substrate. The plural of bump electrode are arranged in array to the opposite side of said substrate and the semiconductor chip is sealed by resin.

Concretely, an insulation layer is formed to cover an electric conductor layer pattern formed on the surface of the substrate, and the semiconductor chip is mounted through an adhesive material on the insulation layer.

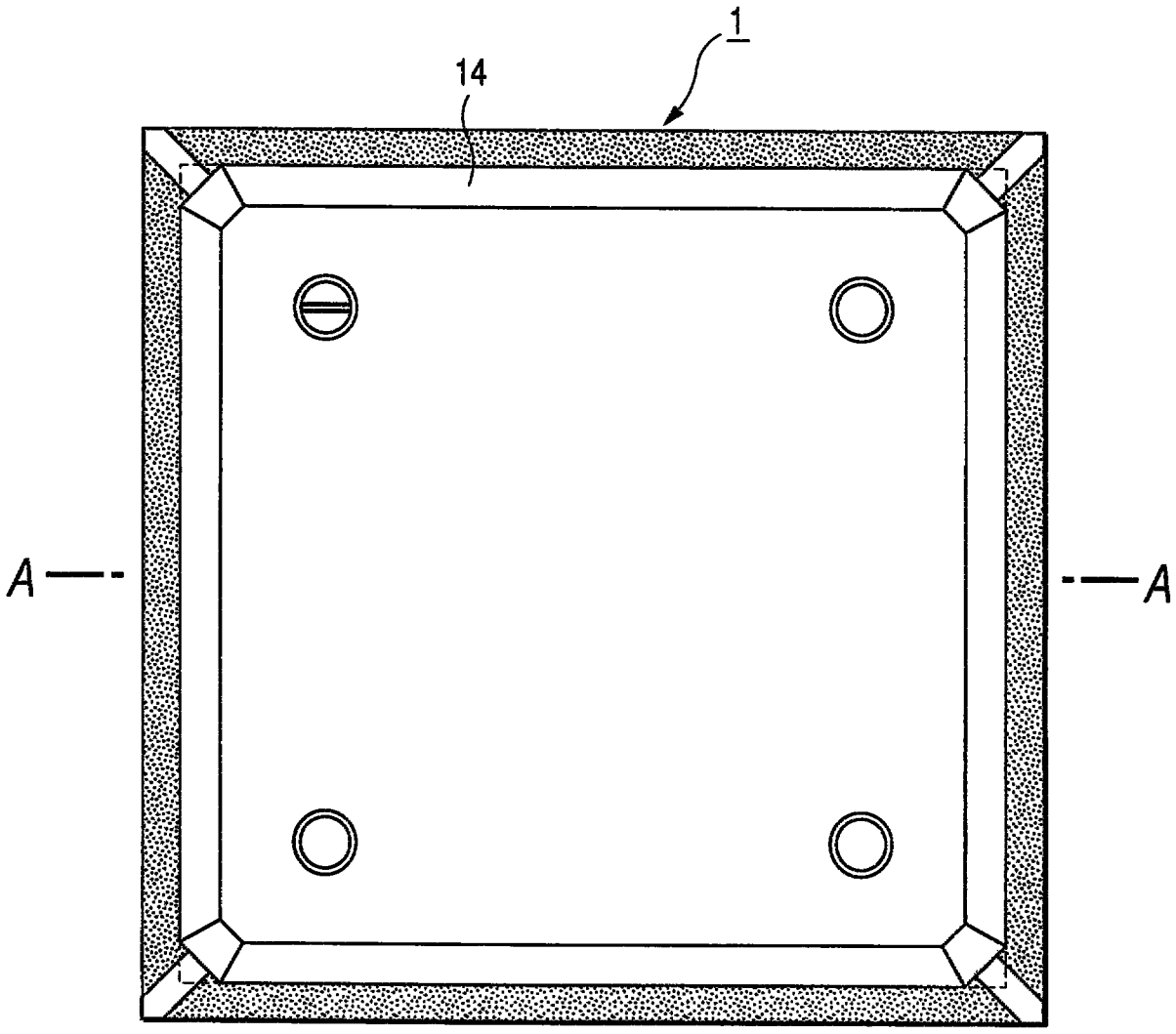
The above insulation layer is divided into the plural number of part that is mutually discontinuous in the area under the above semiconductor chip. By this divided insulation layer, the short circuit between above semiconductor chip and above electric conductor layer pattern is prevented and the deformation of the substrate that comprises the above flexible films is suppressed.

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FIG. 1

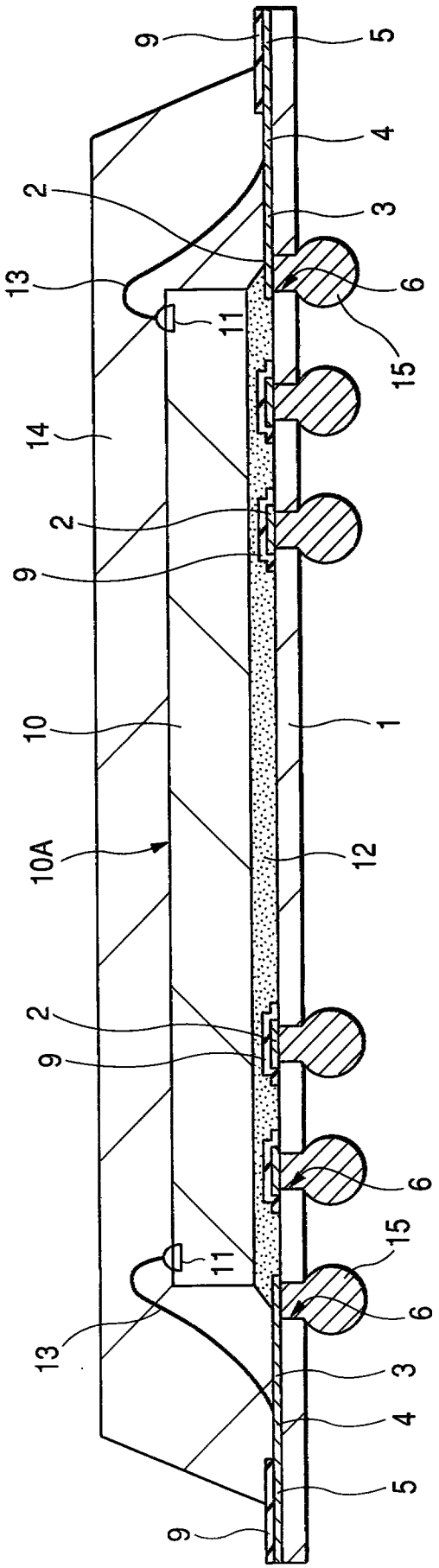


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FIG. 2

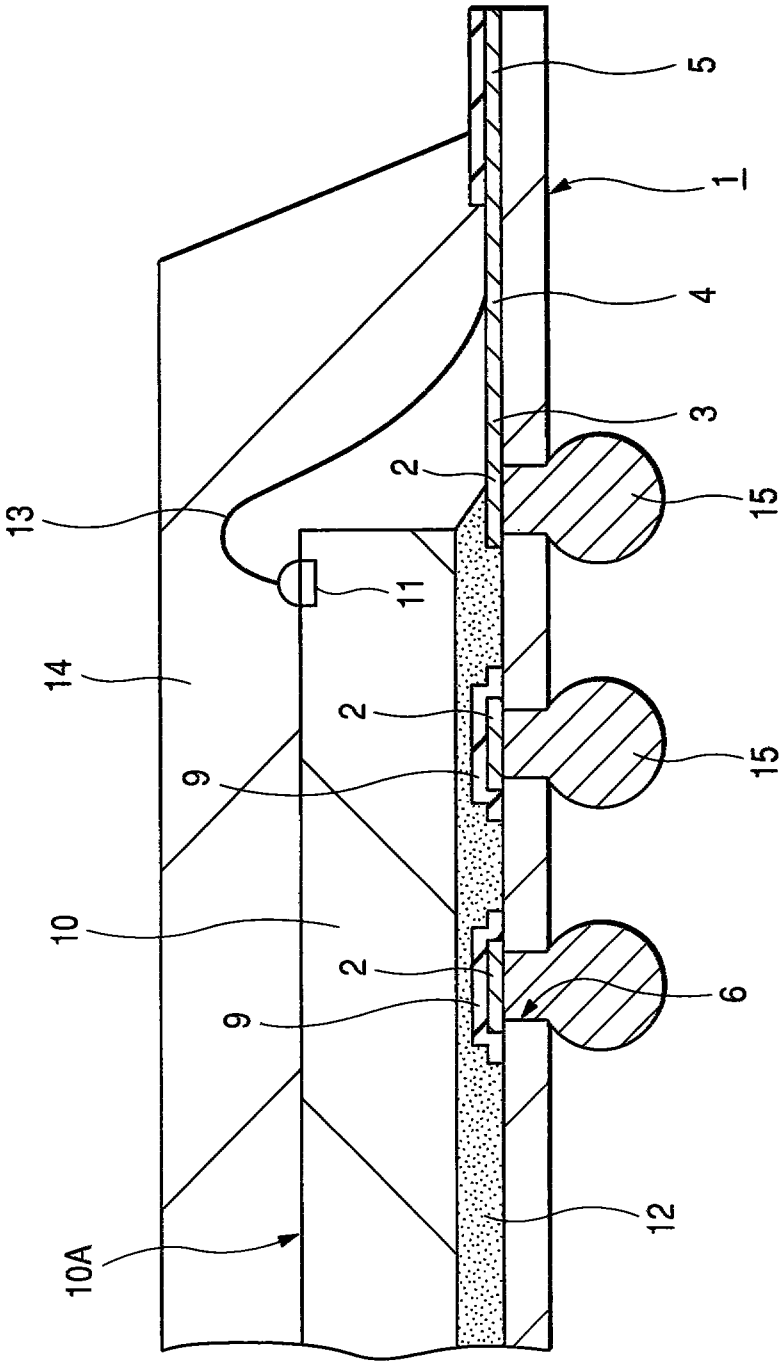


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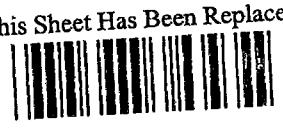


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FIG. 3

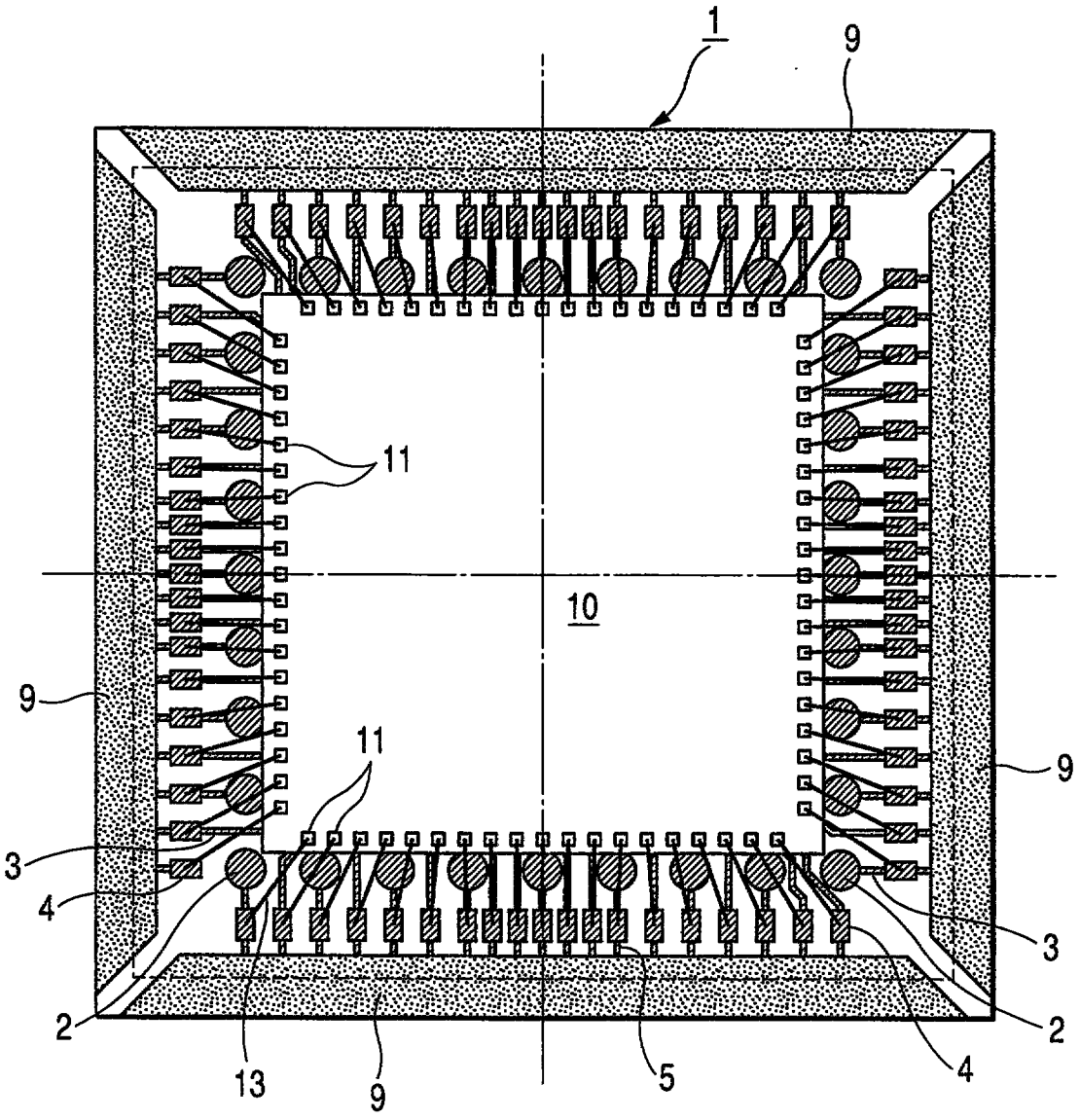


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FIG. 4

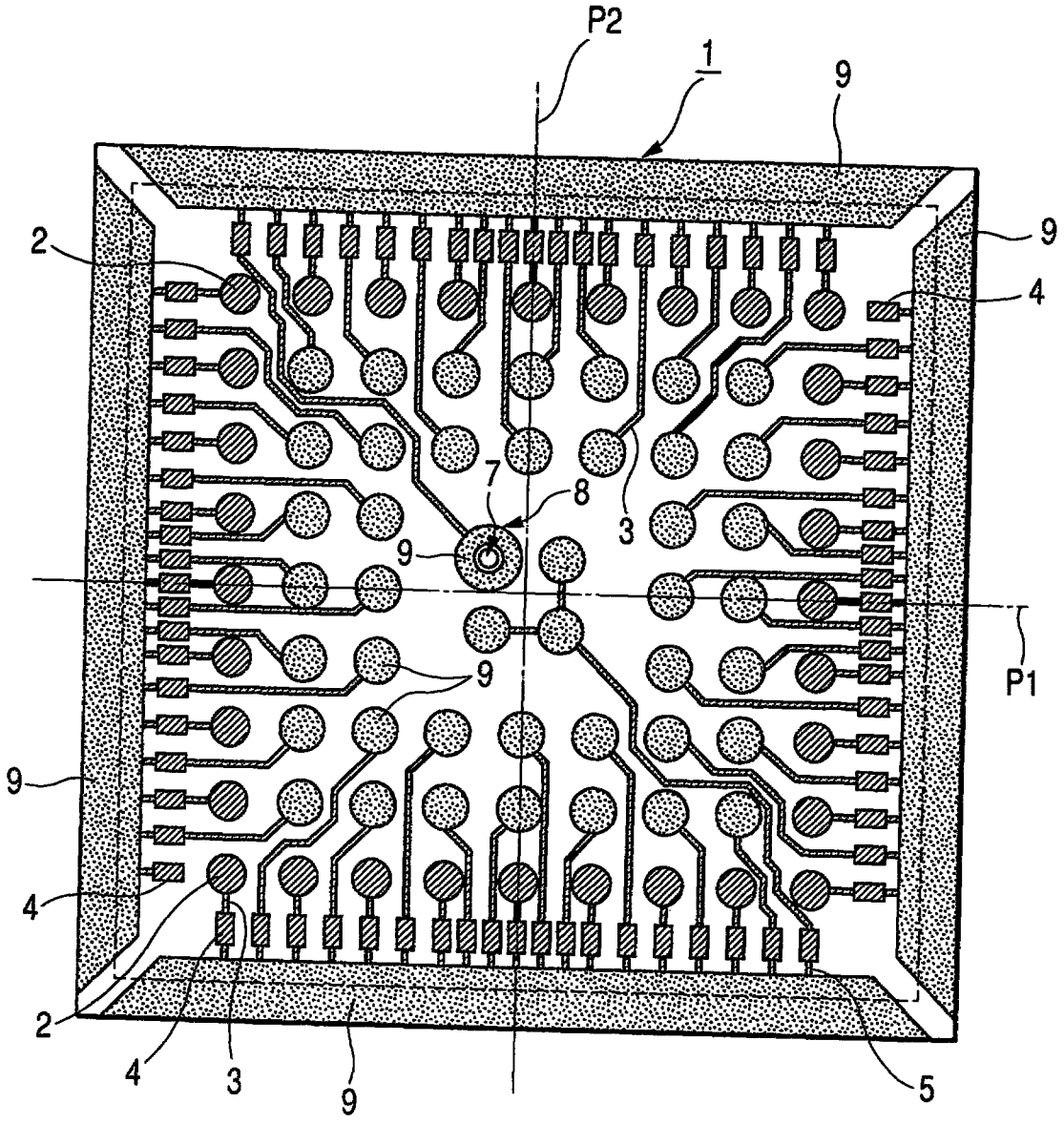


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FIG. 5



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FIG. 6

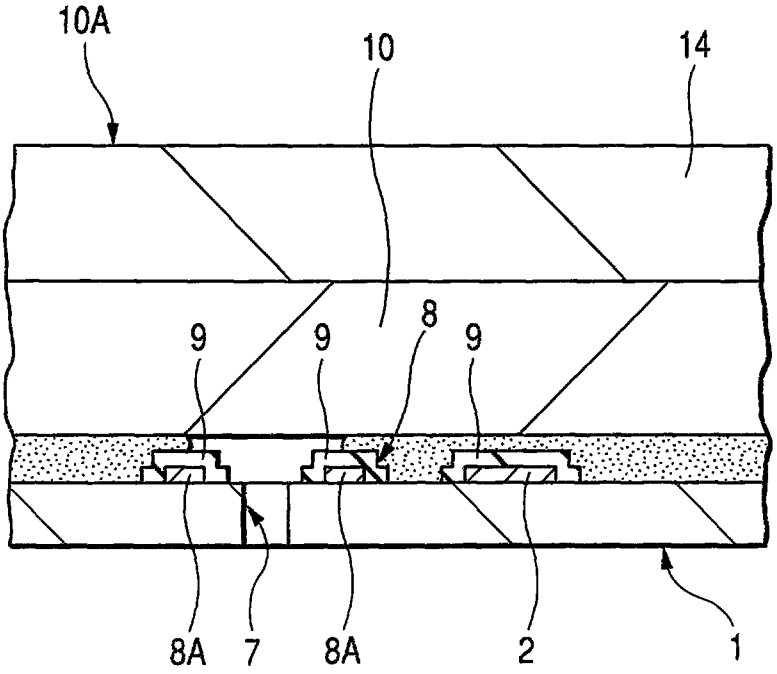
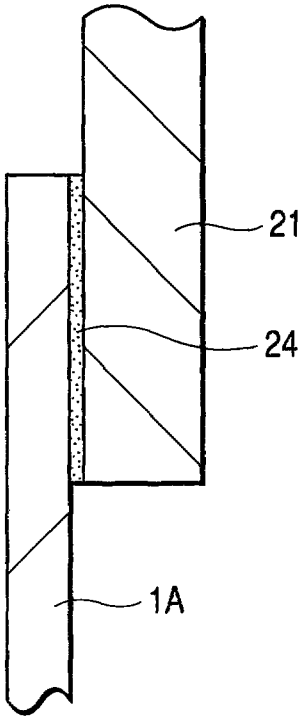
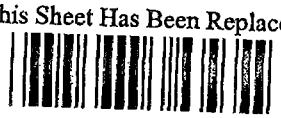


FIG. 8

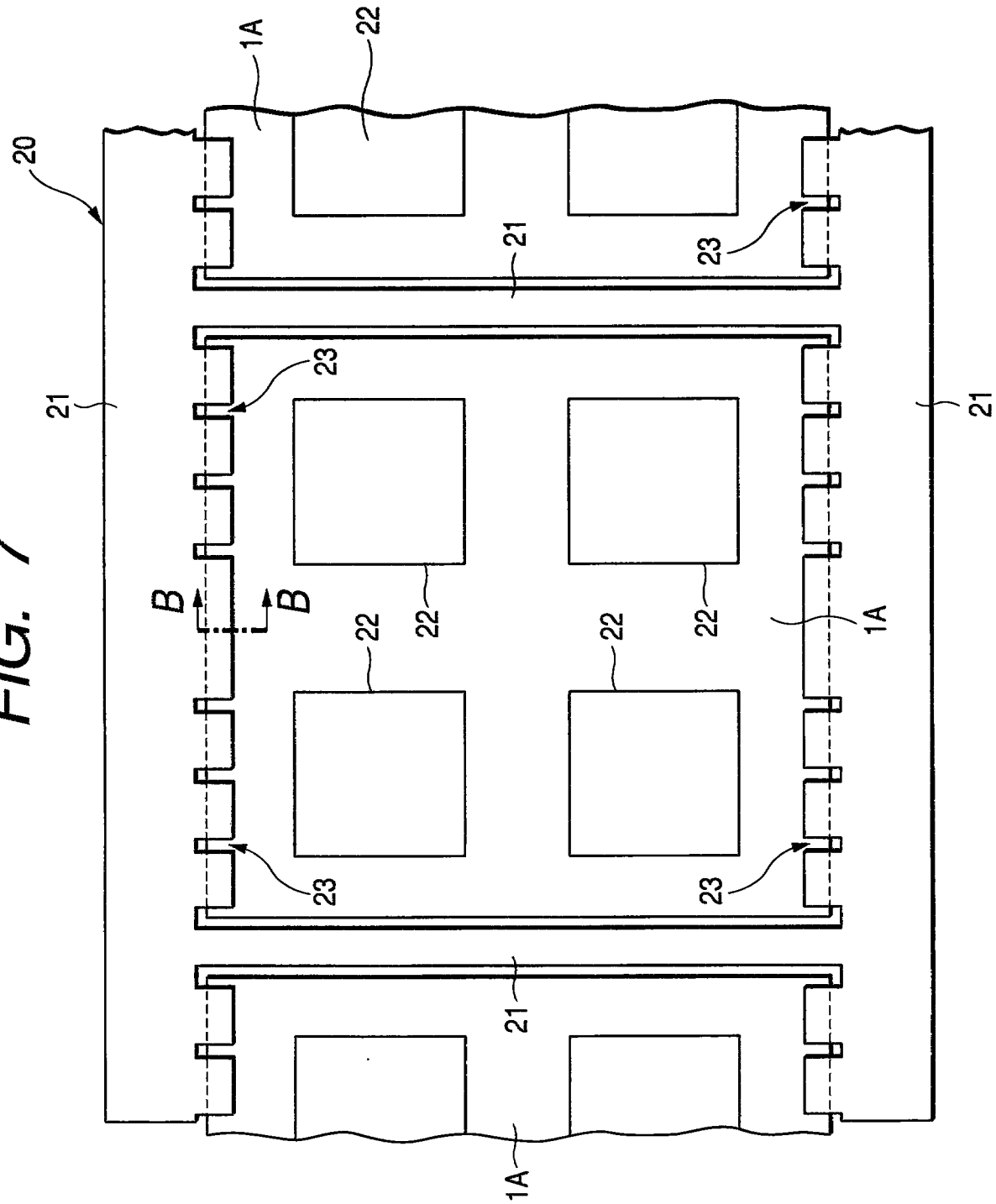


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FIG. 7



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FIG. 9(A)

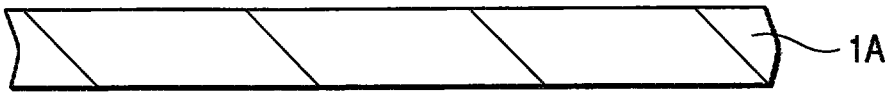


FIG. 9(B)

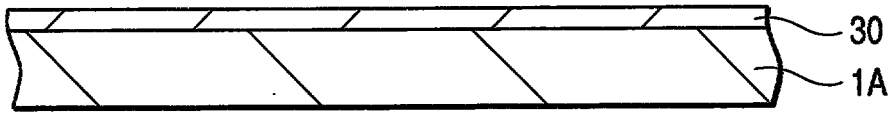


FIG. 9(C)

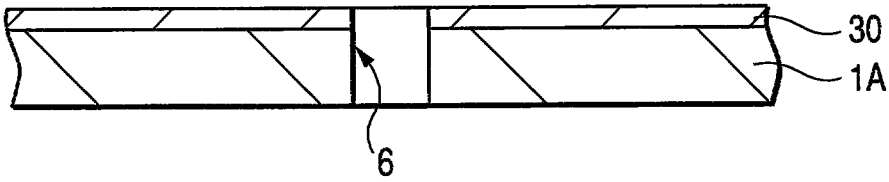


FIG. 9(D)

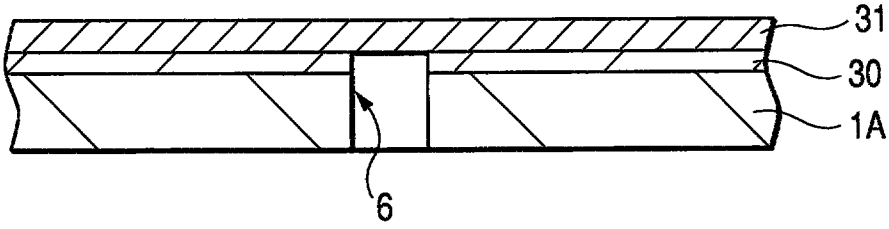
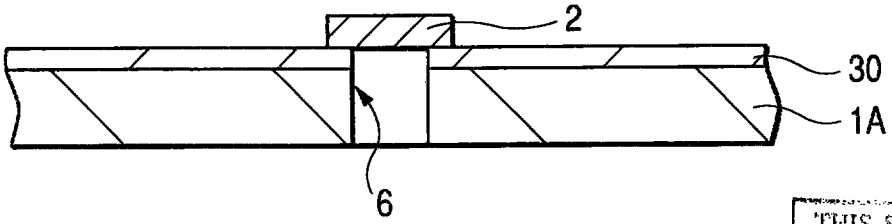


FIG. 9(E)



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FIG. 10(F)

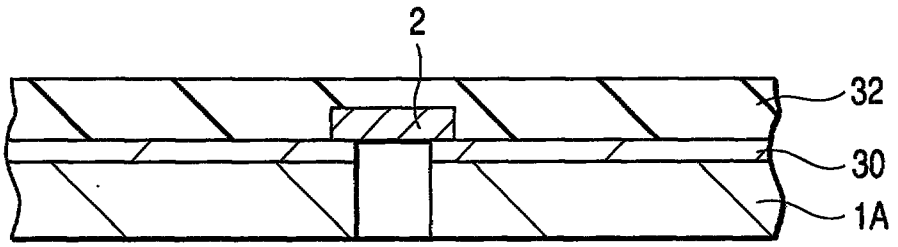
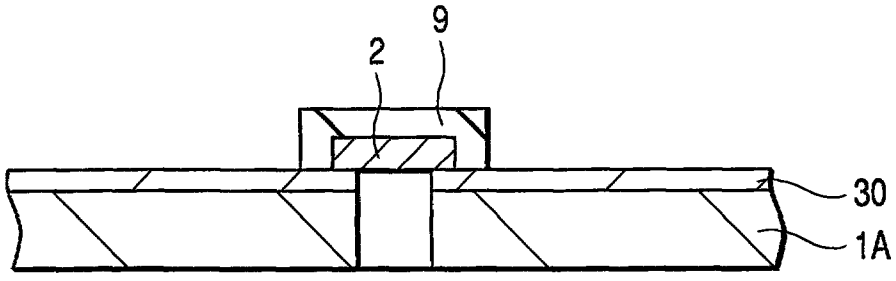


FIG. 10(G)



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FIG. 11

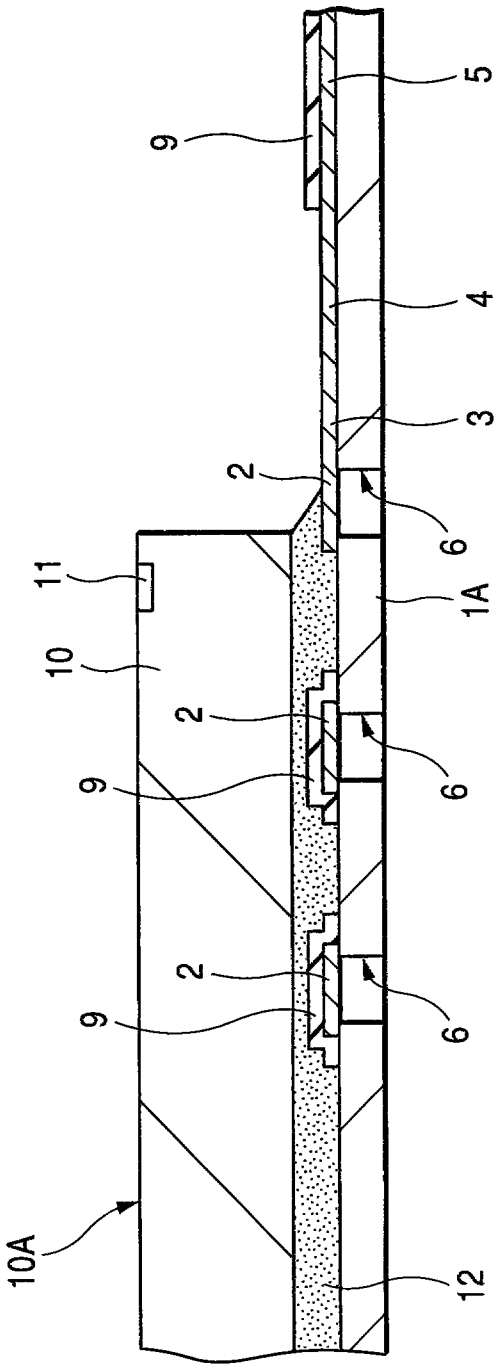
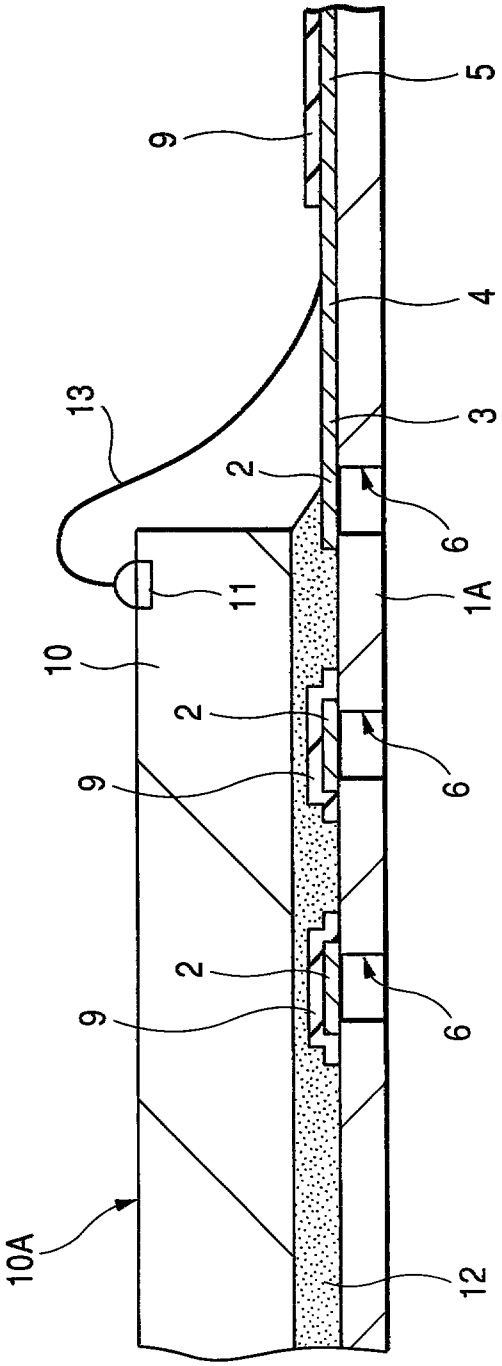


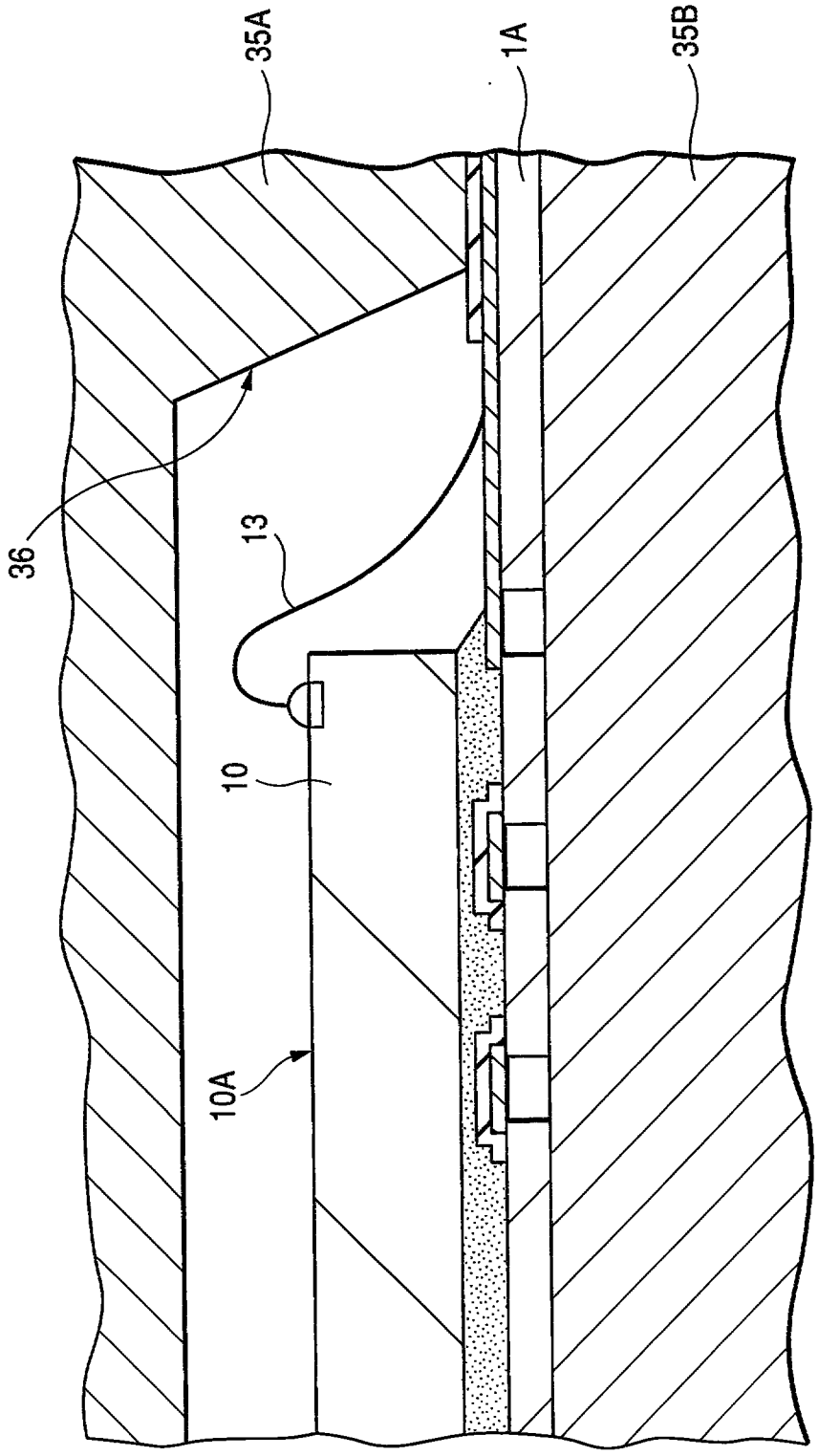
FIG. 12



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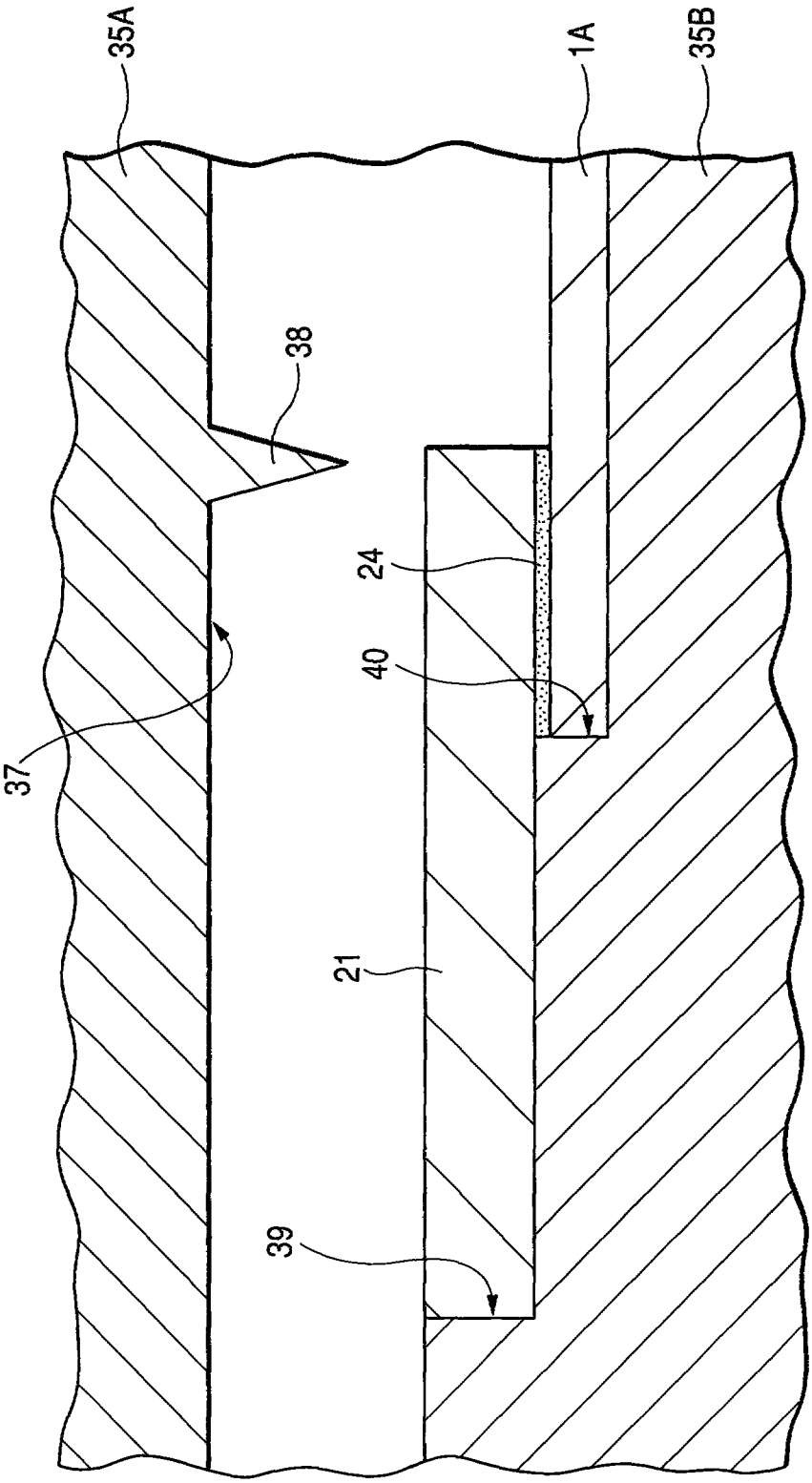
FIG. 13



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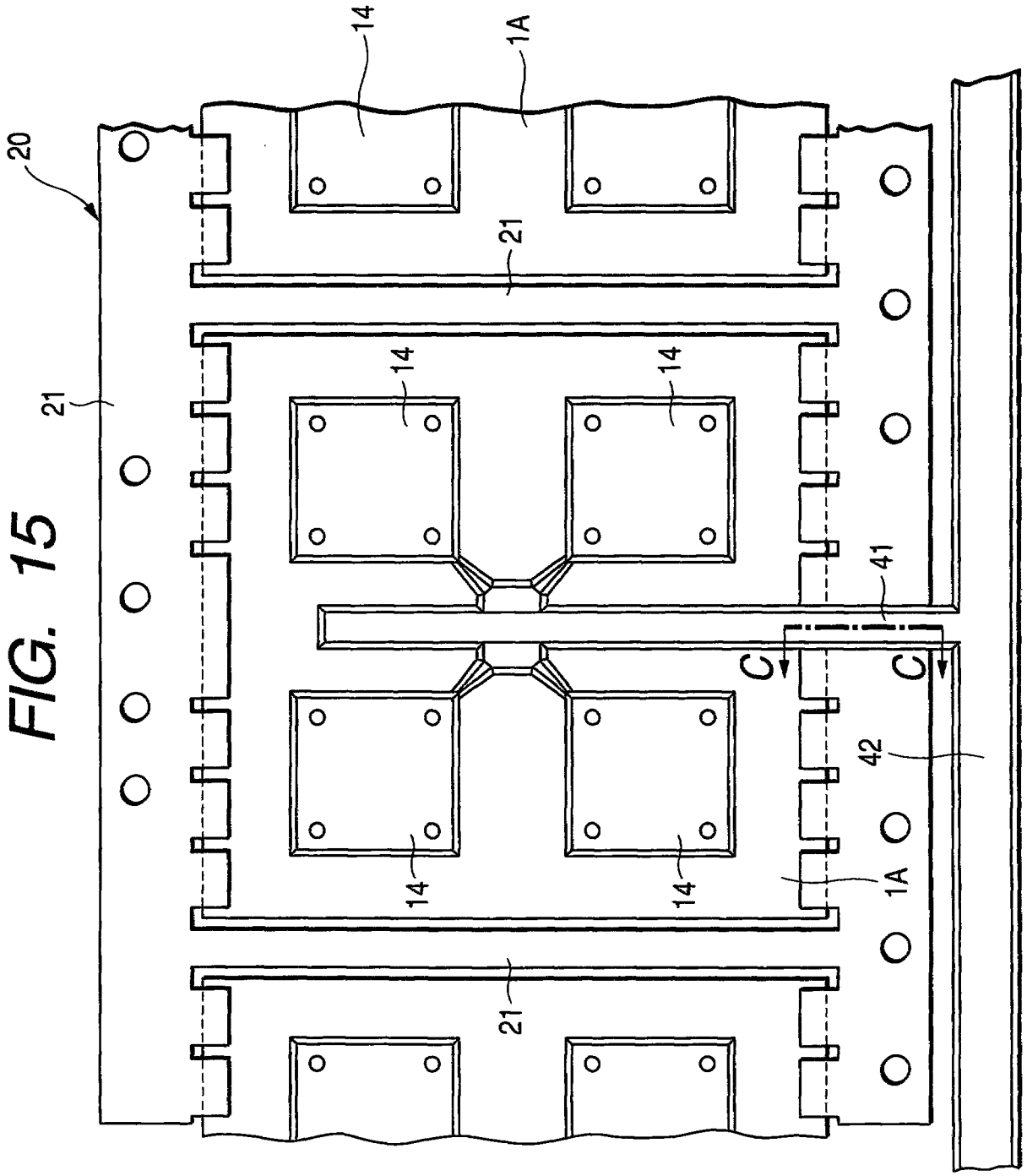
FIG. 14



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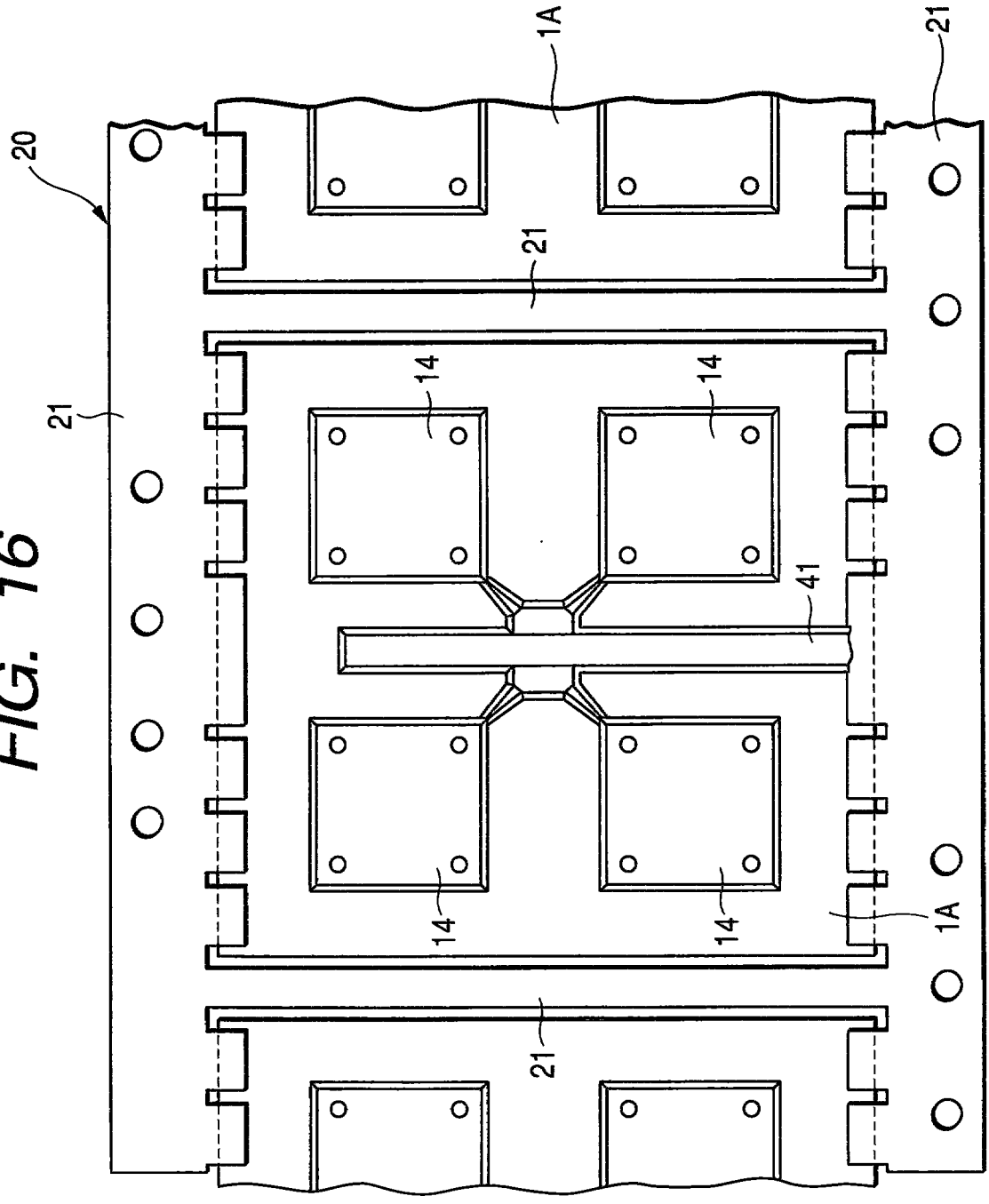
FIG. 15



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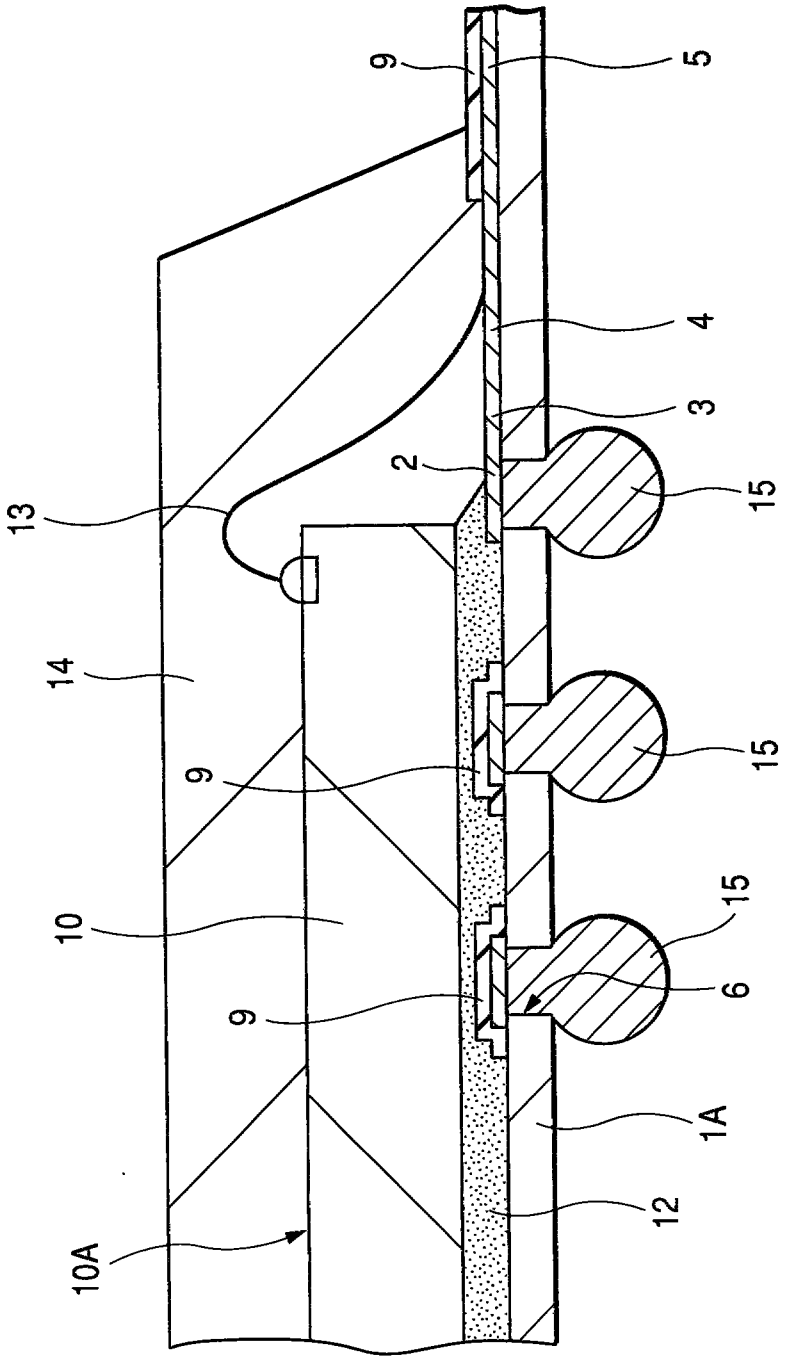
FIG. 16



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FIG. 17



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FIG. 18

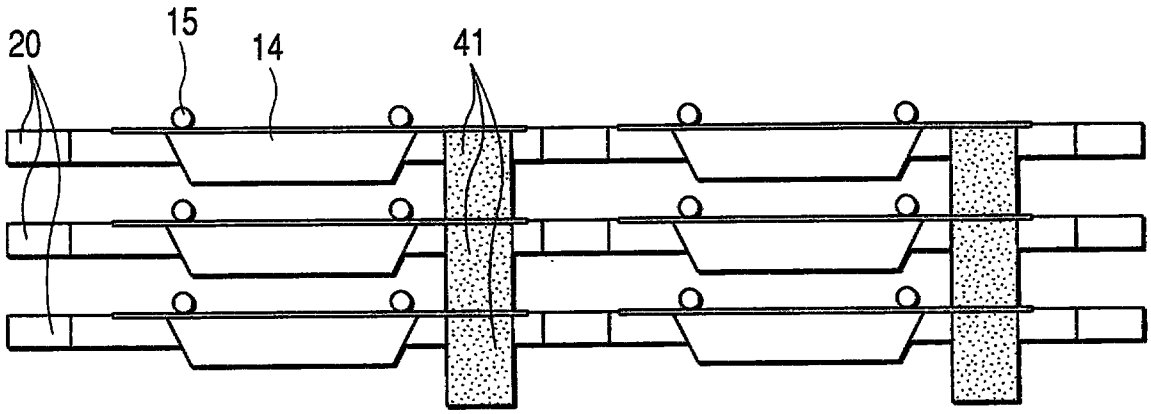


FIG. 19

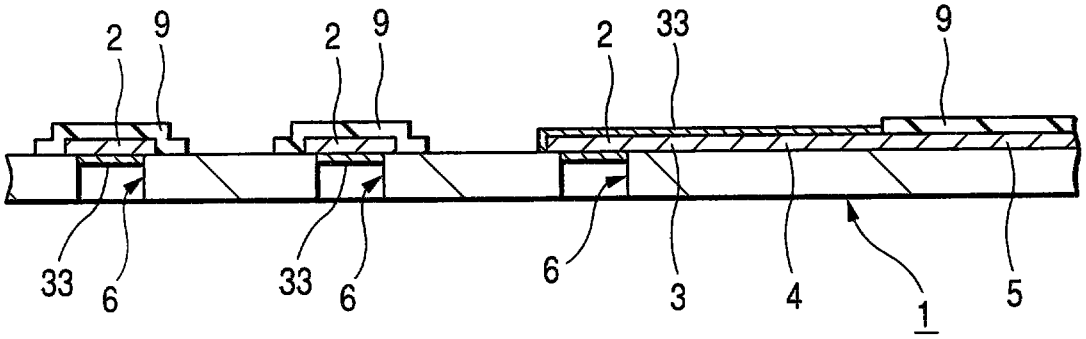
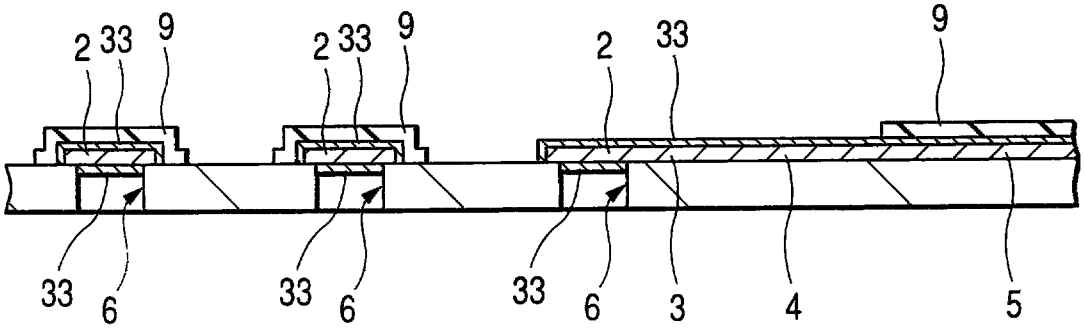


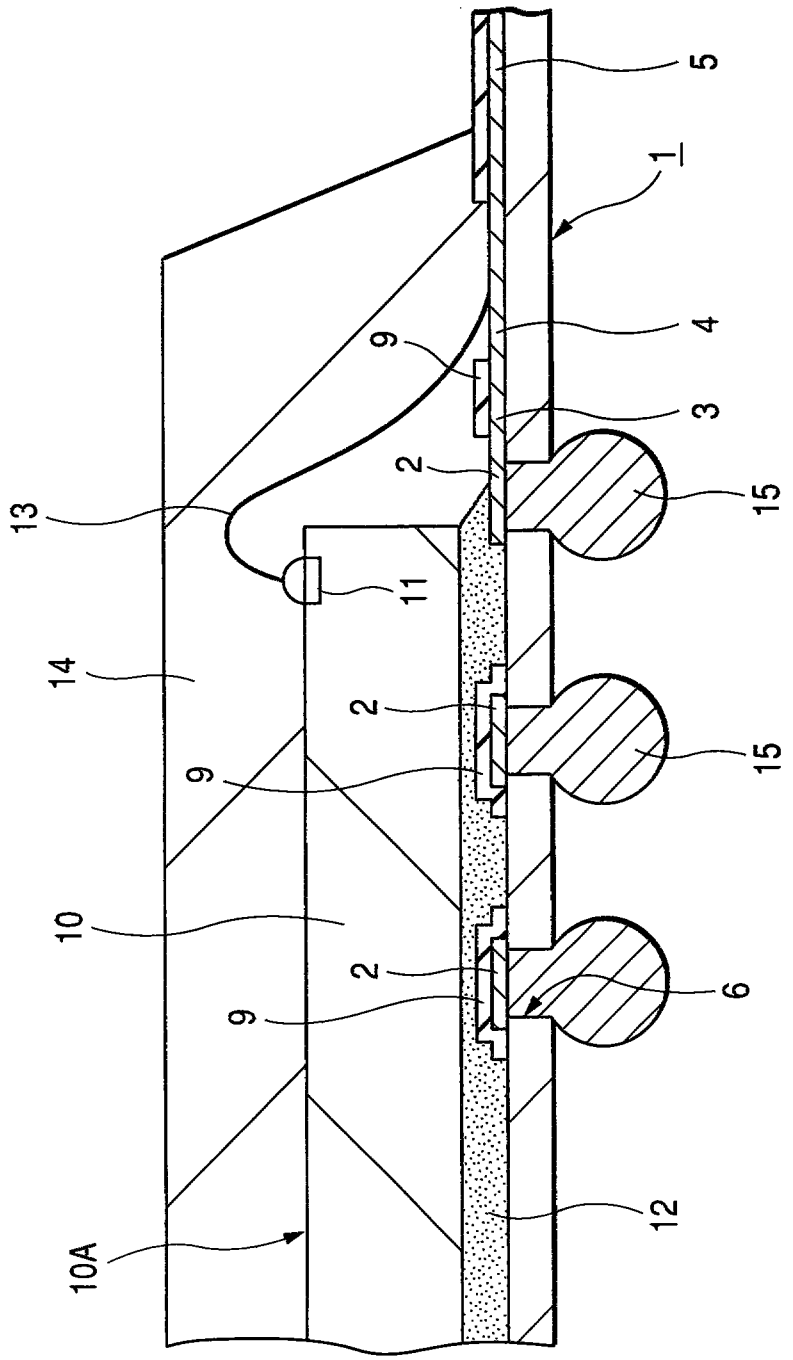
FIG. 20



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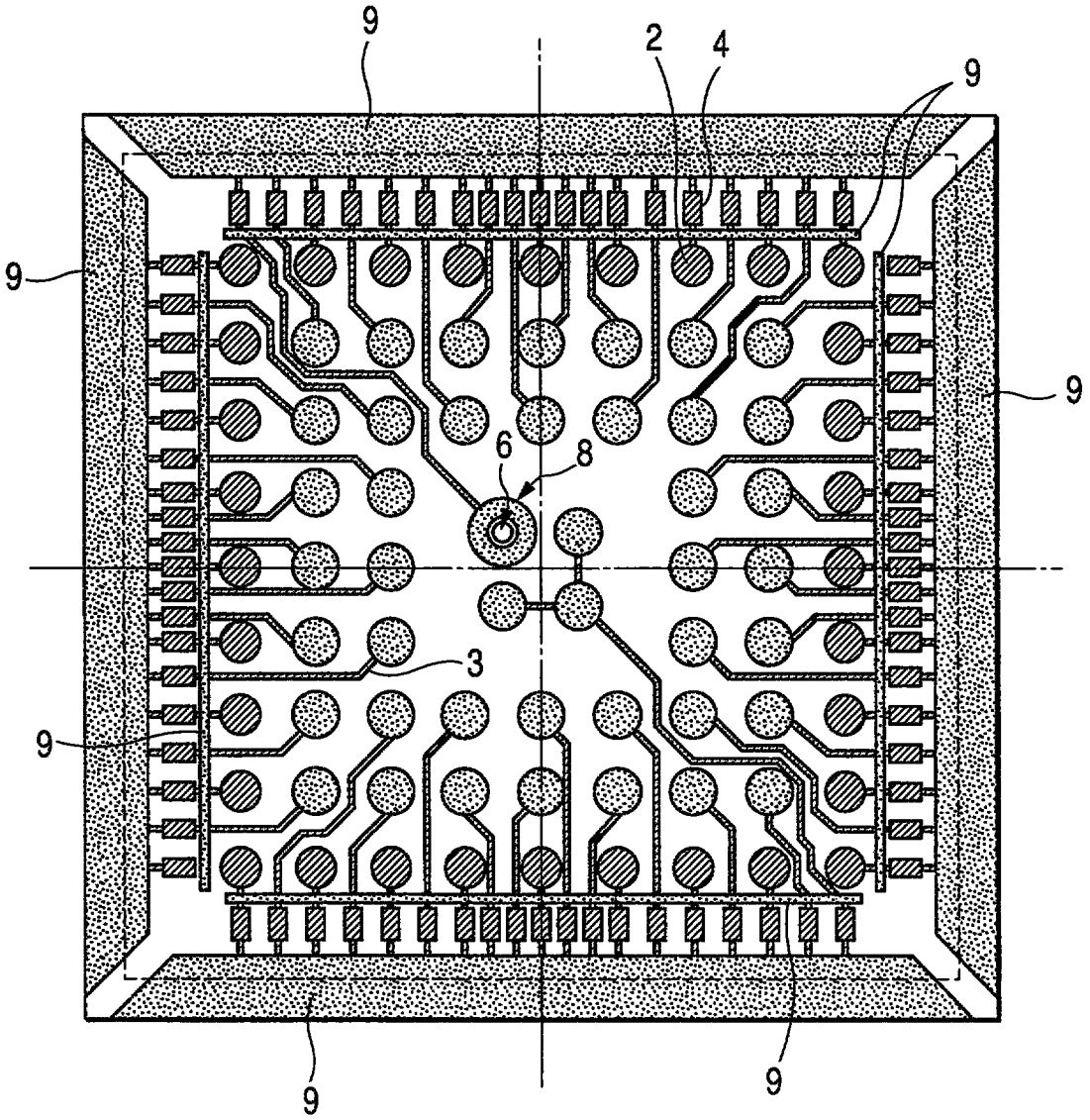
FIG. 21



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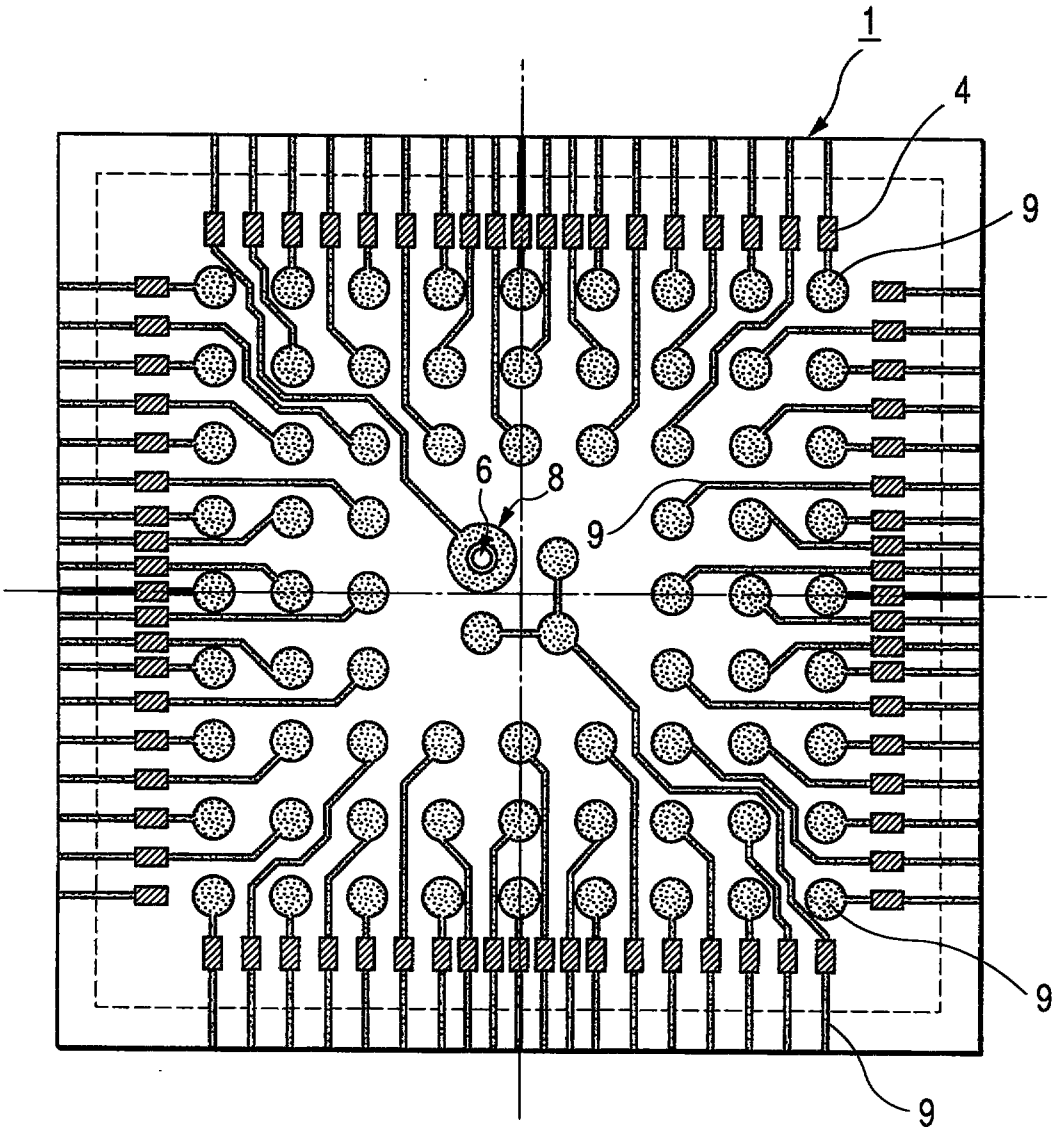
FIG. 22



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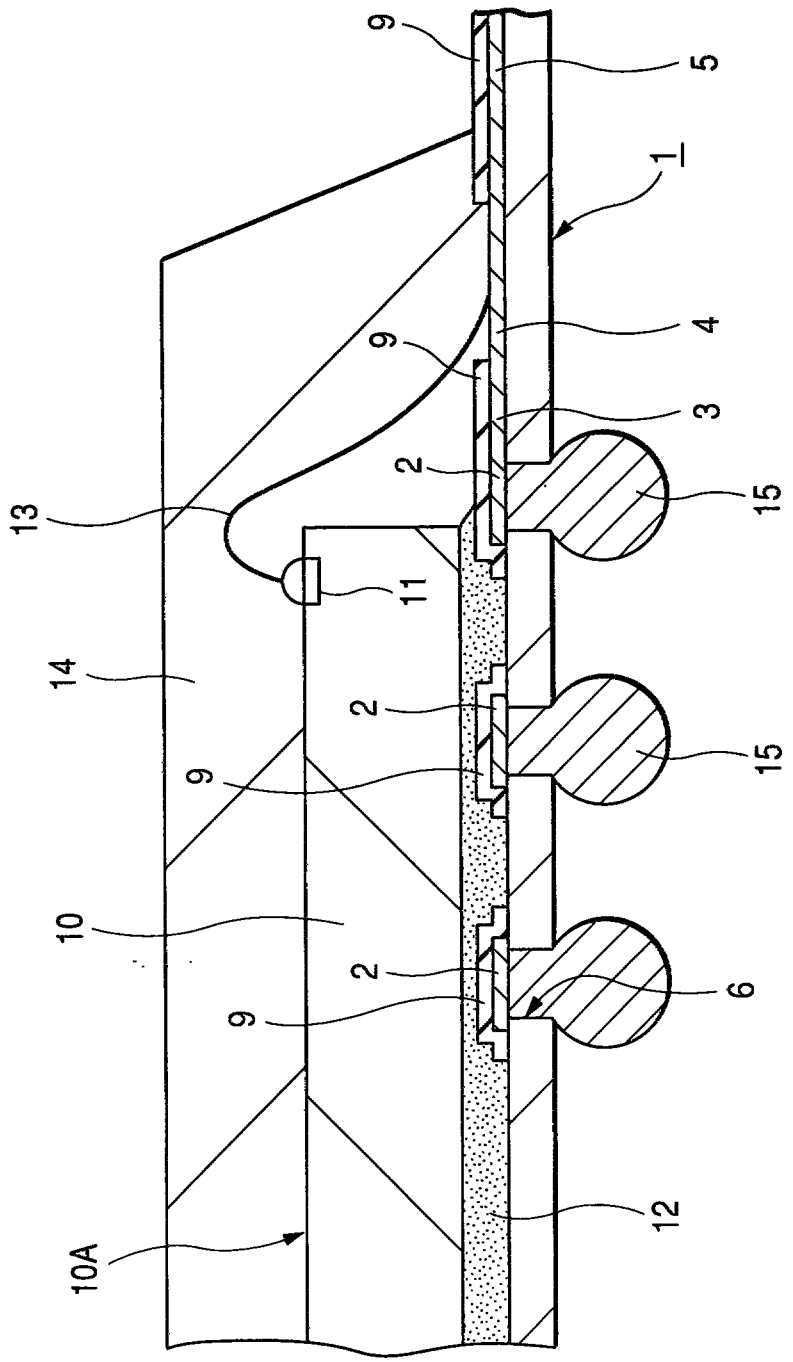
FIG. 23



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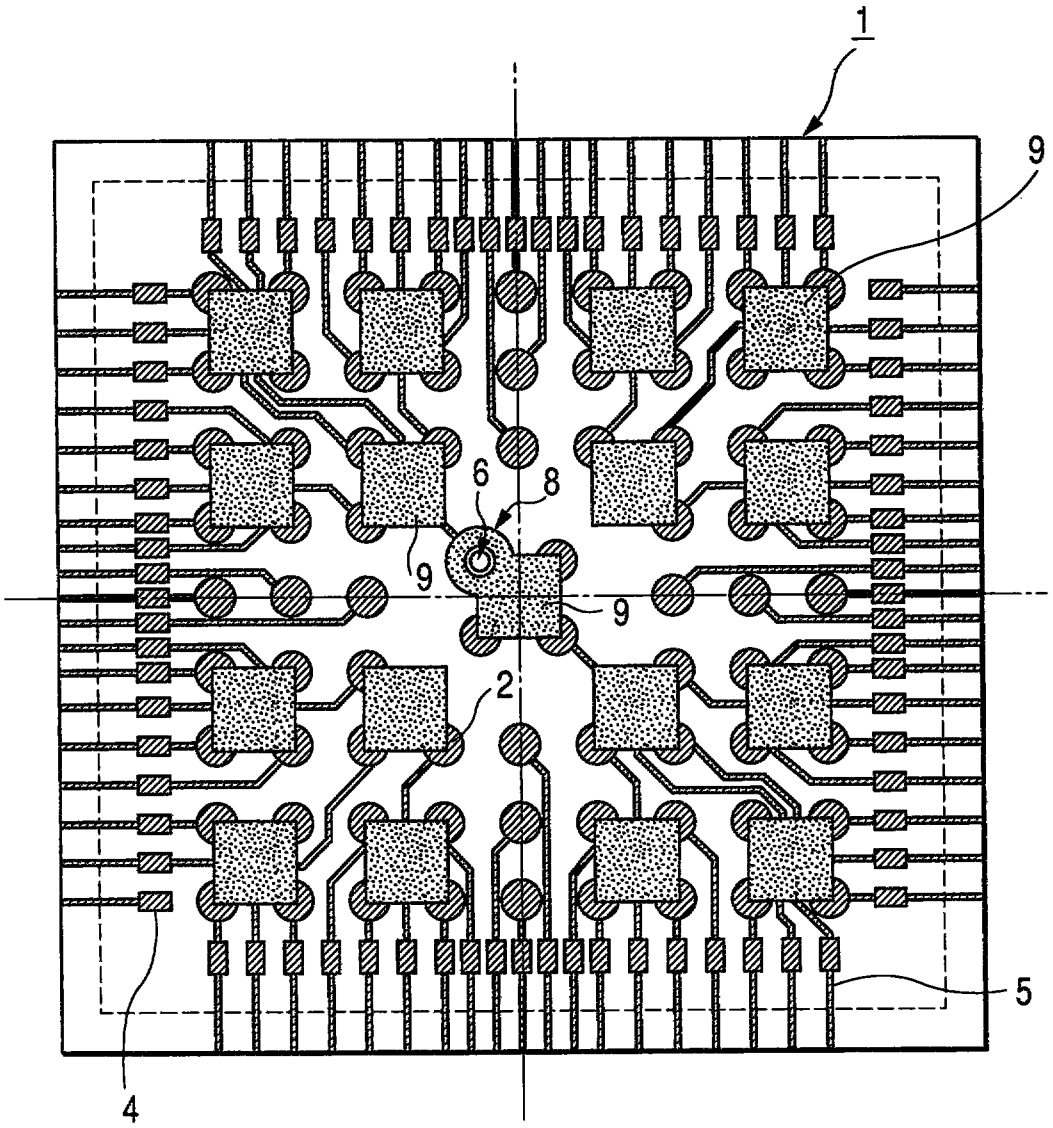
FIG. 24



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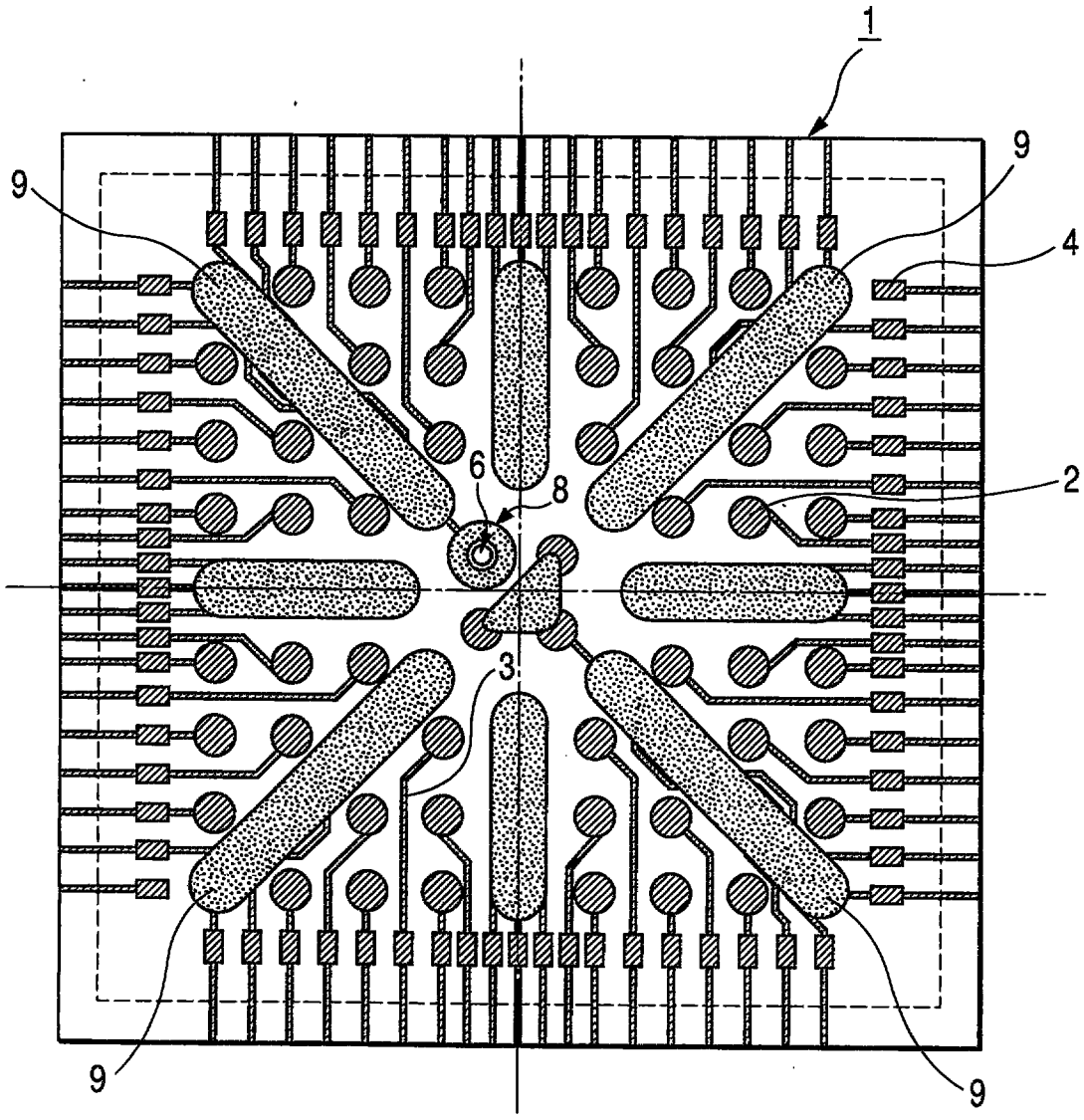
FIG. 25



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FIG. 26



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REPLACEMENT SHEET
30 SEP 1998

SPECIFICATION

TITLE OF THE INVENTION

Semiconductor device and its manufacturing method

BACKGROUNG OF THE INVENTION

This invention relates to the technique that is applied for a semiconductor device, especially for a semiconductor device with the base substrate that comprises flexible films.

As suitable semiconductor device for high-pin-count package, the semiconductor equipment of the BGA(BALL GRID ARRAY) structure has been developed. This semiconductor device of the BGA structure mounts a semiconductor chip on a chip mount area of a main surface of a base substrate by using adhesive material and has several bump electrodes positioned in an array to the side of the back that is opposed to said main surface of a base substrate.

The above base substrate is made of the rigid resin substrate that is impregnated glass fiber with for example, an epoxy resin, a polyimide resin, maleimide resin, etc.. Electrode pads for wire connection are arranged in a peripheral area that surrounds the periphery of the chip mount area of the main surface of the base substrate. And, several electrode pads for bump connection are arranged in the back of the base substrate. The bump electrodes comprise the solder materials of for example, the Pb-Sn composition, fix and connect to the electrode pads for bump connection electrically and

REPLACEMENT SHEET
30 SEP 1998

mechanically.

The above semiconductor chip comprises the structure mainly of the semiconductor substrate that includes for example, monocrystal silicon. To the semiconductor chip, a logical circuit system, a storage circuit system or those mixture circuit systems are formed. And, several external terminals (bonding pad) are allocated to the main surface (element formation face) of the semiconductor chip. These external terminals are electrically connected to electrode pads for wire connection arranged on the main surface of the base substrate through wires.

The above semiconductor chip, the wires, the electrode pads for wire connection, etc. are sealed in the resin sealing body formed on the main surface of the base substrate. The resin sealing body is formed by the method of a transfer mold which is suitable for the mass production.

The semiconductor device of the BGA structure composed like this is mounted on the surface of a printed circuit board by the melting connection of the bump electrodes to the electrode pads formed on the surface of the printed circuit board.

And, it is stated in for example, the NIKKEI electronics (number on February 28, 1994, from the 111th page to the 117th page) of NIKKEI BP company publication about the semiconductor device of the above BGA structure.

REPLACEMENT SHEET
30 SEP 1998

SUMMARY OF THE INVENTION

The semiconductor device of the BGA structure using a flexible film as a base substrate has been developed in recent years. The semiconductor device of this BGA structure can plan to make it thinner type, to make it high-pin-count package and to miniaturize it comparing with a semiconductor device using a rigid resin substrate as a base substrate. However, these inventors, etc. have found the following problems in developing semiconductor equipment using a flexible film as a base substrate.

The base substrate that comprises flexible films is generally made in the following process. First, a connection hole is formed to the bump connection area of a flexible film. Then, the metal foil that comprises of for example, copper (Cu) is attached to the one-sided surface of a flexible film through an adhesive material. Then, electric conductor layers that comprise electrode pads for bump connection, an electric conductor, an electrode pad for wire connection and an electric conductor for plating etc. is formed by doing patterning to the metal foil. Then, the insulation layer that protects the electric conductor layer is formed. Then, processing of plating to form a plating layer to the electrode pad for bump connection and wire connection is done. Plating processing is done by the method of electrolytic plating. This plating processing is sometimes done in the step before forming an insulation layer. The plating

REPLACEMENT SHEET
30 SEP 1998

layer is formed on for example, gold (Au)/ nickel (Ni) film or the gold(Au)/ palladium (Pd)/nickel(Ni) film.

The above insulation layer is formed by following process for example. First, a photosensitive resin film is formed to the one-sided surface of a flexible film. Then, after doing baking processing, by using a photograph printing technique, processing of photosensitive processing, development processing and cleaning are done. The insulation layer is formed to almost all areas of the one-sided surface of the flexible film containing electric conductor layers except electrode pads for wire connection. That is, insulation layers are formed to almost all areas of the one-sided surface of the flexible film. Therefore, the warp and distortion, etc. arise in the base substrate. This deformation of a base substrate causes a transfer trouble in the manufacturing process (assembly process) of a semiconductor device. And, this deformation of a base substrate becomes a cause that in the process that mounts a semiconductor chip, the wetting performance of an adhesive material is deteriorated.

As for a deformation of the above base substrate, it is the main factor that the thermal expansion coefficient and the hardening shrinkage rate of an insulation layer are large. But in case an insulation layer is not formed, the following problems arise.

(1)Electrode pads for bump connection are arranged to the chip mount area of a main surface of a base substrate.

REPLACEMENT SHEET
30 SEP 1998

Therefore, when mounting a semiconductor chip through the adhesive insulation material to the chip mount area of a main surface of the base substrate, it is difficult to control the thickness of an adhesive material. And, because a semiconductor chip touches electrode pads for bump connection, a short circuit arises between them.

(2)Electrode pads for bump connection are arranged to the chip mount area of the main surface of the base substrate. Bump electrodes arranged to the side of the back of a base substrate are connected to these electrode pads for bump connection through connection holes formed in the chip mount area of a base substrate. That is, bump electrodes are arranged in the area under a semiconductor chip.

The electrode pads for bump connection arranged to the chip mount area of the above base substrate are integrated and are electrically connected through electric conductors to the electrode pads for wire connection arranged to the peripheral area that surrounds the periphery of the chip mount area of the main surface of a base substrate. That is, in the peripheral area of the main surface of the base substrate, electric conductors are arranged to the area between a semiconductor chip and electrode pads for wire connection. Therefore, when connecting the external terminals of a semiconductor chip and pads for wire connection with wires, other electric conductors that adjoin electric conductors electrically connected to the

REPLACEMENT SHEET
30 SEP 1998

wires and these wires sometimes cross themselves. In case it sufficiently has the height of a wire connection, it is no problem. However, there is some possibility of causation of a short circuit with wires and other electric conductors, when wires and other electric conductors do not become parallel at the corner of a semiconductor chip. And, it has possibility that in case wires and other electric conductors cross each other on the side of electrode pads for wire connection, a short circuit with wires and other electric conductors also arise.

It is an object of the present invention to provide a technique that is possible to suppress a deformation (warp and distortion) of a base substrate in the semiconductor device with the base substrate that comprises flexible films.

It is another object of the present invention to provide a technique that is possible to suppress a deformation of a base substrate in the semiconductor device with the base substrate that comprises flexible films and to prevent a short circuit with the electric conductors of the base substrate and the semiconductor chip.

It is another object of the present invention to provide a technique, in the semiconductor device with the base substrate that comprises of flexible films, that is possible to suppress a deformation of a base substrate and to prevent the electric conductor layer of a base substrate and wires from short-circuiting.

REPLACEMENT SHEET
30 SEP 1988

These and other objects, features and advantages of the invention will become more apparent upon a reading of the following description and appended drawings.

Summary of the invention disclosed in this application is explained as follows.

(1)Semiconductor device that arranged electric conductor layers in a main surface of a base substrate that comprises flexible films and mounted a semiconductor chip by using a adhesive material on the above main surface of a base substrate. And insulation layers are portioned into block construction on said electric conductor layers of the main surface of the base substrate. Insulation layers are portioned into block construction for example, every electric conductor layers.

(2)Semiconductor device that arranged electric conductor layers in a chip mount area of a main surface of a base substrate that comprises flexible films and mounted a semiconductor chip by using an adhesive material on the above chip mount area of a main surface of a base substrate. And insulation layers are portioned into block construction on said electric conductor layers of the main surface of the base substrate. Insulation layers are portioned into block construction for example, every electric conductor layers.

(3) Semiconductor device that arranged a semiconductor chip in a chip mount area of a main surface of base substrate

REPLACEMENT SHEET
30 SEP 1998

being made of flexible film by using an adhesive material. Electrode pads for wire connection formed in a peripheral area that surrounds said chip mount area. Electric conductors being arranged between said semiconductor chip and said electrode pads for wire connection in said peripheral area. External terminals of said semiconductor chip and said electrode pads for wire connection are electrically connected through wires. And insulation layers are portioned into block construction on said electric conductors.

By means of (1) mentioned above, as a stress by contraction of expansion and hardening of an insulation film is relieved, a deformation (warp and distortion) of a base substrate can be suppressed.

By means of (2) mentioned above, as a semiconductor chip does not touch electric conductor layers, when a semiconductor chip is mounted on the chip mount area of the main surface of the base substrate by using an adhesive material, a short circuit with electric conductor layers and a semiconductor chip can be prevented.

By means of (3) mentioned above, as wires do not touch electric conductors, the electric conductor of a base substrate and the wires can be prevented from short-circuiting.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is the plan view of a semiconductor device that is

REPLACEMENT SHEET
30 SEP 1998

one embodiment of this invention;

Fig. 2 is an enlarged sectional view cut at the position of the A-A line that is shown in Fig. 1;

Fig. 3 is the main part enlarged sectional view of Fig. 2;

Fig. 4 is the plan view of a state that the resin sealing body of the above semiconductor device was removed;

Fig. 5 is the plan view of a base substrate;

Fig. 6 is the main part enlarged sectional view of the above semiconductor device;

Fig. 7 is the main part plan view of the frame structure that is used in the manufacturing process of the above semiconductor device;

Fig. 8 is an enlarged sectional view cut at the position of the B-B line that is shown in Fig. 7;

Fig. 9 is a main part cross-sectional view to explain a method of manufacturing the above frame structure;

Fig.10 is a main part cross-sectional view to explain a method of manufacturing the above frame structure.

Fig. 11 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device;

Fig. 12 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device.

Fig. 13 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device.

Fig. 14 is a main cross-sectional view to explain a method

REPLACEMENT SHEET
30 SEP 1998

of manufacturing the above semiconductor device.

Fig. 15 is a main part plan view to explain a method of manufacturing the above semiconductor device.

Fig. 16 is a main part plan view to explain a method of manufacturing the above semiconductor device;

Fig. 17 is a main part cross-sectional view to explain a method of manufacturing the above semiconductor device;

Fig. 18 is the outline structure figure that shows a state that the above frame structure was stacked to the multisteps;

Fig. 19 is a main part cross-sectional view to explain a method of manufacturing the above frame structure;

Fig. 20 is a main part cross-sectional view to explain a method of manufacturing the above frame structure;

Fig. 21 is a main part cross-sectional view that shows the first formation example of a semiconductor device that is one embodiment of this invention.

Fig. 22 is the plan view of the base substrate that shows the first formation example of a semiconductor device that is one embodiment of this invention.

Fig. 23 is the plan view of the base substrate that shows the second formation example of a semiconductor device that is one embodiment of this invention.

Fig. 24 is the main part cross-sectional view of a semiconductor device using the base substrate that is shown in Fig. 23.

REPLACEMENT SHEET
30 SEP 1998

Fig. 25 is the plan view of the base substrate that shows the third formation example of a semiconductor device that is one embodiment of this invention.

Fig. 26 is the plan view of the base substrate that shows the fourth formation example of a semiconductor device that is one embodiment of this invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

As follows, it is explained with an embodiment of this invention applying for the semiconductor device of the BGA structure. And, the same code is put on the thing that has the same function in several drawings to explain an embodiment, and an explanation of its repeat is omitted.

Fig. 1 is a plan view of a semiconductor device that is one embodiment of this invention. Fig. 2 shows an enlarged sectional view cut at the position of the A-A line that is shown in Fig. 1. Fig. 3 is an enlarged sectional view of an essential part of Fig. 2. Fig. 4 is a plan view of a state that a resin sealing body was removed. Fig. 5 is a plan view of a base substrate. Fig. 6 is an enlarged sectional view of an essential part of the above semiconductor device.

As it is shown in Fig. 1, Fig. 2 and Fig. 3, the semiconductor device becomes the following structure. Semiconductor chip 10 is mounted by using adhesive material 12 on the chip mount area of a main surface of base substrate

REPLACEMENT SHEET
30 SEP 1998

1. And several bump electrodes 15 are positioned in an array to the side of the back that is opposed to the main surface of base substrate 1. Bump electrodes 15 are formed in the solder material of for example, 63 weight % Pb-37 weight % Sn composition. The semiconductor device of this embodiment is a surface-mounted type BGA(Ball Grid Array) package and it is called as the CSP(CHIP SIZE PACKAGE) which has a chip mounting area almost equal to the size of the semiconductor chip.

The plane shape of above base substrate 1 is formed in the square-form. This base substrate 1 is made of flexible film that comprises the insulation resins of for example, epoxy system or the insulation resin of a polyimide system. Base substrate 1 is set at the thickness of 50 micron [μ M] of for example.

The electric conductor layers that comprise electrode pads 2 (bump land) for bump connections, electric conductors 3 and electrode pads 4 for wire connection, electric conductors 5 for plating, etc. are arranged on the main surface of above base substrate 1. Several electrode pads 2 for bump connection and electrode pads 4 for wire connection are provided, and several electric conductors 3 and electric conductors 5 for plating are provided. That is, several electric conductor layers are arranged on the main surface of base substrate 1. Electrode pads 2 for bump connection are integrated with electrode pads 4 for wire connection through electric conductors 3 and are

REPLACEMENT SHEET
30 SEP 1998

electrically connected each other. Electric conductors 5 for plating are integrated with electrode pads 4 for wire connection and are electrically connected each other. Electrode pad 2 for bump connection, electric conductors 3 , electrode pads 4 for wire connection and electric conductors 5 for plating etc. are formed by doing etching processing on a metal foil after sticking metal foil, for example, the Cupper(Cu) foil to main surface of a flexible film by using adhesive materials. These electrode pads 2 for bump connection and electric conductors 3, electrode pads 4 for wire connection and electric conductors 5 for plating are set at the thickness of 18 micron [μ Ms] for example.

The plane shape of above semiconductor chip 10 is formed in the square-form. This semiconductor chip 10 becomes structure mainly of the semiconductor substrate that comprises for example, monocrystal silicon. To semiconductor chip 10, a logical circuit system, a storage circuit system or those mixture circuit systems are formed. These circuit systems are formed by connecting several semiconductor elements formed to the side of main surface (element formation face) 10A of semiconductor chip 10 through the electric conductors.

Several external terminals (bonding pad) 11 arranged along each side of semiconductor chip 10 are arranged on main surface 10A of above semiconductor chip 10. Each of this several external terminals 11 are formed to the top layer of

REPLACEMENT SHEET
30 SEP 1993

electric conductor layers formed on the main surface of the semiconductor substrate, and are made of for example, aluminum (Al) film or an aluminum alloy film. And, each of several external terminals 11 are electrically connected to circuit systems formed to semiconductor chip 10.

A great part of above several electrode pads 2 for bump connection are arranged in the chip mount area of the main surface of base substrate 1. Other (remainder) electrode pads 2 for bump connection are arranged to the peripheral area that surrounds the periphery of the chip mount area of the main surface of base substrate 1. Several bump electrodes 15 arranged to the side of the back of base substrate 1 fix on the back of each of these several electrode pads 2 for bump connection through connection holes 6 formed in base substrate 1, and they are connected electrically and mechanically. And, in this embodiment, the plane shape of electrode pads 2 for bump connection are formed in the circle-form.

As it is shown in Fig. 2, Fig. 3 and Fig. 4, each of said electrode pads 4 for wire connection are arranged to the peripheral area of main surface of base substrate 1 and are arranged along each side of semiconductor chip 10. Each of electrode pads 4 for wire connection are electrically connected to each of several external terminals 11 arranged on main face 10A of semiconductor chip 10 through wires 13. For example, the Au wires are used as wires 13. Wires 13 are connected by

REPLACEMENT SHEET
30 SEP 1998

the method of bonding that used an ultrasonic in combination with thermo compression bonding for example.

Electric conductors 3 integrated with electrode pads 2 for bump connection arranged to the chip mount area of main surface of base substrate 1 exist and extend in the chip mount area and the peripheral area of main surface of base substrate 1. And, electric conductors 3 integrated with electrode pads 2 for bump connection arranged to the peripheral area of main surface of base substrate 1 exist and extend in the peripheral area of main surface of base substrate 1. That is, in the peripheral area of main surface of base substrate 1, electric conductors 3 are arranged to the area between semiconductor chip 1 and electrode pads 4 for wire connection.

Above semiconductor chip 10, electric conductors 3, electrode pads 4 for wire connection and wires 13, etc. are sealed in resin sealing body 14. Resin sealing body 14 is formed in the resin of an epoxy system to which for example, phenol system hardener, silicone rubber and a filler were added for the purpose of planning a lower stress. Resin sealing body 14 is formed by the method of a transfer mold suitable for the mass production. The transfer molding method uses a molded die assembly with a pot, a runner, a gate, a cavity, etc.. And it is a method of injecting a resin in the cavity through a runner and a gate from the pot and forming a resin sealing body.

Each of electric conductors 5 for plating is arranged

REPLACEMENT SHEET
30 SEP 1998

outside electrode pads 4 for wire connection in the peripheral area of 1 surface of base substrate 1. Each of these electric conductors 5 for plating are arranged along each side of semiconductor chip 10. A part of electric conductors 5 for plating are arranged to the inside of resin sealing body 14, and other parts are arranged to the outside of the resin sealing body.

As it is shown in Fig. 2, Fig. 3 and Fig. 5, insulation layers 9 are arranged to the over surface of each of several electrode pads 2 for bump connection arranged to the chip mount area of main surface of above base substrate 1. These insulation layers 9 are divided and arranged for every electrode pads 2 for bump connection in the chip mount area of main surface of base substrate 1. Insulation layers 9 are divided into several part so that it is scattered in the chip mount area of main surface of base substrate 1. That is, the semiconductor device of this embodiment divides insulation layers 9 into several parts in the chip mount area of main surface of base substrate 1 and arranges this divided insulation layer 9 on electrode pads 2 for bump connection. And, the plane shape of insulation layer 9 arranged on electrode pads 2 for bump connection in the embodiment is formed in the circle-form.

On the over surface of each of electric conductors 5 for plating arranged to the peripheral area of one surface of above base substrate 1, insulation layers 9 are arranged. These

REPLACEMENT SHEET
30 SEP 1998

insulation layers 9 exist and extend along each side of base substrate 1 and are divided into every side of base substrate 1. Insulation layers 9 are divided into several to dot in the peripheral area of base substrate 1. That is, the semiconductor device of this embodiment divides insulation layer 9 into several in the peripheral area of one surface of base substrate 1 and is arranging these insulation layers 9 on electric conductors 5 for plating.

The part of insulation layers 9 arranged on above electric conductors 5 for plating are arranged to the inside of resin sealing body 14, and other parts are arranged outside resin sealing body 14. That is, insulation layers 9 lie between electric conductors 5 for plating and resin sealing body 14.

As it is shown in Fig. 5 and Fig. 6, vent hole 7 is provided in the chip mount area of above base substrate 1. Like this, by providing vent hole 7 in the chip mount area of base substrate 1, the out gas that occurs at the time of hardening of adhesive material 12 when applying adhesive material 12 on the chip mount area of one surface of base substrate 1 and mounting semiconductor chip 10 on it can be emitted to the outside. And, the steam that occurs in adhesive material 12 by the heat at the time of surface-mounting that mounts a semiconductor device on the surface of a mounting substrate or the heat at the time of a temperature cycle test that is an environmental test after product completion of a semiconductor device can be

REPLACEMENT SHEET
30 SEP 1998

emitted to the outside.

On the chip mount area of main surface of above base substrate 1, dam 8 that surrounds the periphery of vent hole 7 is built. Dam 8 of this embodiment is composed of conduction film 8A and insulation layers 9 arranged on the conduction film 8A.

Above vent hole 7 is arranged to the position that deviated from center line P1 of the X direction (horizontal direction in the figure) of base substrate 1 and center line P2 of the Y direction (vertical direction in the figure) of base substrate 1 as it is shown in Fig. 5. That is, vent hole 7 is arranged to the position that deviated from the center of base substrate 1. In case a semiconductor device is looked at from the side of the back of base substrate 1, like this, the arrangement to the position that deviated from the center of base substrate 1 of vent hole 7 can clear a direction as an index. And, because a direction can be cleared as an index, vent hole 7 can be used as an index.

Then, the frame structure that is used in the manufacturing process of the above semiconductor device is explained.

While frame structure 20 is not limited to this, it is composed of the matrix frame structure that arranged unidirectionally several areas specified in for example, frame body 21 like the indication in Fig. 7(main part plan view).Film

REPLACEMENT SHEET
30 SEP 1998

base material 1A is arranged in each area specified in frame body 21. Film base material 1A of this embodiment prepares four(4) resin sealing areas 22. That is, film base material 1A to form four(4) products in each area specified in frame body 21 is arranged. And, the electric conductor layer pattern that is shown in Fig. 5 to resin sealing area 22 is formed.

Above frame body 21 is formed by doing manufacture of etching manufacture or press punching on a board material. The thing that comprises for example, the Cu system alloy materials is used as a board material.

As it is shown in Fig. 7 and Fig. 8 (cross-sectional view cut at the position of the B-B line that is shown in Fig. 7), the above film base material 1A is fixed to two(2) portions of adhesion area where parts of frame body 21 is opposed each other by using adhesive material. Slit 23 is prepared in the adhesion area of each of frame body 21. This slit 23 puts a specified space on the longitudinal direction of frame structure 20, and several are arranged. Like this, by preparing slit 23 in the adhesion area of frame body 21, because a stress by difference between the materials of frame body 21 and film base material 1A can be relieved, transformation of a warp, distortion, etc. of film base material 1A can be suppressed.

Then, a method of manufacturing above frame structure 20 is explained by using Fig. 9 and Fig. 10 (main part cross-sectional view to explain a manufacturing method).

REPLACEMENT SHEET
30 SEP 1998

First, as it is shown in Fig. 9-(A), film base material 1A is prepared. Film base material 1A is made of the insulation resin of for example, epoxy system or the insulation resin of a polyimide system. Then, as it is shown in Fig. 9-(B), adhesive material 30 is attached to the side of one surface of above film base material 1A. It can be attached by a heat pressurization without using adhesive material 30.

Then, while connection hole 6 is being formed to the bump connection area of above film base material 1A, as it is shown in Fig. 9-(C), and vent hole 7 is formed to the chip mount area of film base material 1A, it is not being illustrated. Connection hole 6 and vent hole 7 are formed by for example, die assembly, laser manufacture, etc.. Then, as it is shown in Fig. 9-(D), metal foil (the Cu foil for example) 31 is attached to the side of one surface of above film base material 1A through connection material 30. After attaching metal foil 31 to film base material 1A, connection hole 6 and vent hole 7 can be formed by a die assembly or laser manufacture, etc.

Then while electrode pads 2 for bump connection are formed on one surface of film base material 1A, as patterning is done on above metal foil 31 and is shown in Fig. 9-(E), and electric conductors 3 and electrode pads 4, electric conductors 5, etc. for plating for wire connection are formed, it is not being illustrated. That is, a electric conductor layer pattern is formed in this process. And, conduction film 8A that also surrounds the

REPLACEMENT SHEET
30 SEP 1998

periphery of vent hole 7 in the chip mount area of one surface of film base material 1A is formed, it is not being illustrated also.

Then as it is shown in Fig. 10-(F), photosensitive resin film 32 of a uniform film thickness is formed to the whole surface on film base material 1A including the above electric conductor layer pattern. After applying a photosensitive resin, photosensitive resin film 32 is formed by the method of screen printing. Then, after doing baking processing, a photograph printing technique, that is, processing of photosensitive processing, development processing and cleaning, etc. are done, and as it is shown in Fig. 10-(G), insulation layer 9 of a specified pattern is formed. In this process, as it is shown in Fig. 5, insulation layers 9 divided into several are arranged on the electric conductor layers. And, dam 8 that also comprises insulation layers 9 arranged on conduction film 8A and this conduction film 8A in this process also is formed. In case insulation layers 9 are arranged to the whole surface on film base material 1A, by difference between material characteristics such as film base material 1A, electric conductor layers and insulation layers 9, it warps in base substrate 1, and transformation of a distortion, etc. arises. But by dividing and arranging insulation layers 9 like this embodiment, a deformation of base substrate 1 can be suppressed because that a stress by shrinkage of expansion and hardening of insulation layers 9 are relieved.

REPLACEMENT SHEET
30 SEP 1998

Then, the plating layer (for example, the Au/Ni layer, the Au/Pd/Ni, Pd/Ni layer and the Sn/Ni layer, etc.) that is possible to be bonded is formed by the plating processing by the method of electrolytic plating is formed on the electric conductor layer which is not covered by said insulation layers. The frame structure that is shown in Fig. 7 is formed after this by cutting film base material 1A an individual piece and attaching it to the adhesion area of frame body 21 by using adhesive material 24. A transfer of film base material 1A in the manufacturing process (assembly process) of a semiconductor device improves, and formation of frame structure 20 that has film base material 1A to the area specified in frame body 21 like this that attached film base material 1A to the adhesion area of frame body 21 improves handling.

Then, a method of manufacturing the above semiconductor device is explained.

First, frame structure 20 that is shown in Fig. 7 is prepared. Frame structure 20 has film base material 1A in the area specified in frame body 21. Resin sealing area 22 is arranged to film base material 1A, and the electric conductor layer pattern that is shown in Fig. 5 is formed to this resin sealing area 22.

Then, a semiconductor chip 10 is mounted through adhesive material 12 on the chip mount area of main surface of above film base material 1A, as it is shown in Fig. 11 (main part cross-

REPLACEMENT SHEET
30 SEP 1998

sectional view). Adhesive material 12 is supplied to the chip mount area of one surface of film substrate 1A by the multi-point potting method. The heat curable insulation resin of for example, epoxy system or a polyimide system is used as adhesive material 12. And as an adhesive material 12, the thermoplastic insulation resin of for example, epoxy system or polyimide system is also fine. Out gas that occurs at the time of hardening of adhesive material 12 because vent hole 7 that is shown in Fig. 6 is provided to the chip mount area of film base material 1A in this process can be set free in the outside. And, the inflow to vent hole 7 of adhesive material 12 because of building dam 8 that surrounds the periphery of vent hole 7 that is shown in Fig. 6 on the chip mount area of one surface of film base material 12 can be stemmed and can be stopped. Therefore, the prevention of a blockage of vent hole 7 by adhesive material 12 and the going round inwardly of adhesive material 12 to the side of the back of film base material 1A can be prevented. And, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, semiconductor chip 10 does not touch electrode pads 2 for bump connection because insulation layers 9 are arranged on electrode pads 2 for bump connection. And, even if it is mounted in the state that semiconductor chip 10 tilted and the film thickness of adhesive material 12 thins, semiconductor chip 10 touches insulation layers 9 and semiconductor chip 10 does not touch electric

REPLACEMENT SHEET
30 SEP 1998

conductors 3 because it is supported by this insulation layers 9.

Then, as it is shown in Fig. 12 (main part cross-sectional view), external terminal 11 of above semiconductor chip 10 and electrode pads 4 for wire connection of film component 1A are electrically connected with wires 13. The Au wires are used as wires 13.

Then, above frame structure 20 is set to a molding die assembly. As it is shown in Fig. 13 (main part cross-sectional view), resin sealing area 22, semiconductor chip 10, wires 13, etc. of film base material 1A are arranged in cavity 36 that is formed in upper die 35A and lower die 35B of a molding die assembly. As it is shown in Fig. 14 (main part cross-sectional view), the molding die assembly prepares sub-runner (trunk runner) 37 and protrusion 38, and further, it is not being illustrated , each of an inflow gate, the main runner (main runner) and a pot are arranged. The pot is connected to cavity 36 through each of the main runner, sub-runner 37 and an inflow gate.

The lower die 35B of the above molding die assembly has stepped portion 39 in which frame body 21 of frame structure 20 is installed and stepped portion 40 in which film base material 1A is installed. That is, frame body 21 of frame structure 20 is installed in stepped portion 39 of lower die 35B, and film base material 1A of frame structure 20 is installed in stepped portion 40 of lower die 35B. Vertical matching of upper die 35A and lower

REPLACEMENT SHEET
30 SEP 1998

die 35B is done in the structure of frame body 21- adhesive material 24- film base material 1A.

While it is not being in detail illustrated, above sub-runner 37 crosses stepped portion 39 in which frame body 21 of frame structure 20 is installed and stepped portion 40 in which film base material 1A is installed and exists from the outside of frame structure 20 to inside of it and connects to the cavity 36 through the inflow gate. The above main runner exists and extends along the longitudinal direction of frame structure 20 outside of it and connects to the one end of said sub-runner 37 withdrawn outside frame structure 20. And, protrusion 38 is provided for ease cutting of a resin stiffened in the inside of sub-runner 37. This protrusion 38 is positioned on the area of the stepped portion that is formed in frame body 21 of frame structure 20 and film base material 1A.

Then a resin tablet is put into the above pot. This resin tablet is pressurized in the plunger of transfer mold equipment, and a resin is supplied in cavity 36 through each of the main runner, sub-runner 37 and an inflow gate from the pot. Thus, resin sealing body 14 is formed. After this, frame structure 20 is taken out from the molding die assembly. The state of frame structure 20 unloaded from a molded die assembly is shown in Fig. 15 (main part plan view). In Fig. 15, code 41 is a sub-runner resin stiffened in sub-runner 37 of a molding die assembly, and code 42 is main-runner resin 42 stiffened in the inside of

REPLACEMENT SHEET
30 SEP 1998

main-runner of a molding die assembly. Main-runner resin 42 is existing along the longitudinal direction of frame structure 20. Sub-runner resin 41 is existing from the outside of frame body 21 to the inside of it. And Fig. 14 shows a cross-sectional view at the position of the C-C line that is shown in Fig. 15 .

Then, sub-runner stiffened resin 41 and main runner stiffened resin 42 that is in the outside above frame body 21 are removed. Sub-runner resin 41 that is in the inside of above frame body 21is left. This state is shown in Fig. 16 (main part plan view).

Then, as it is shown in Fig. 17, bump electrodes 15 are connected to the back of electrode pads 2 for bump connection passing through connection holes 6 formed in film base material 1A. Bump electrodes 15 are supplied by carrying ball on the substrate for example, and is connected by melting in the infrared ray reflow, etc.. A transfer state after forming bump electrodes 15 is shown in Fig. 18 (outline structure figure). In case frame structure 20 is stacked to the several steps, a space between frame structure 20 of an upper step and a lower step can be secured in sub-runner stiffened resin 41 provided in frame structure 20 of an upper step. Therefore, bump electrodes 15 of a semiconductor device manufactured in frame structure 20 of a lower step can be protected. Because it can carry in the state that frame structure 20 was stacked to the several steps, a transfer of frame structure 20 improves. And, production rationality in

REPLACEMENT SHEET
30 SEP 1998

the manufacturing process of a semiconductor device improves.

Then, the cutting to the specified shape (base substrate shape) of film base material 1A almost completes a semiconductor device with base substrate 1 that comprises film base materials 1A. The semiconductor device is shipped as a product after this. The semiconductor device shipped as a product is installed on the surface of printed circuit board.

And, bump electrodes 15 can be connected in the state of an individual piece by cutting film base material 1A after forming resin sealing body 14.

And, plating processing can go in the step before forming insulation layers 9. In case plating processing is done in the step after forming insulation layers 9 like this embodiment, as it is shown in Fig. 19 (main part cross-sectional view), plating layers 33 are formed on electrode pads 2 for bump connection, electric conductors 3 and electrode pads 4 for wire connection arranged to the peripheral area of main surface of base substrate (film base material 1A) 1 and to the back of electrode pads 2 for bump connection. That is, plating layers 33 are not formed between a electric conductor layers and insulation layers 9. In case plating processing is done in the step before forming insulation layers 9, as it is shown in Fig. 20 (main part cross-sectional view), plating layers 33 are formed on the electrode pads 2 for bump connection , electric conductors 3, electrode pads 4 for wire connection, electric conductors 5 for plating arranged to the

REPLACEMENT SHEET
30 SEP 1998

periphery of the chip mount area of main surface of base substrate (film base material 1A) 1, and to the back of electrode pads 2 for bump connection. That is, plating layers 33 are formed between electric conductor layers and insulation layers 9.

As it was explained above, according to this embodiment, the following effects are obtained.

(1)By dividing and arranging insulation layers 9 on the electric conductor layers, because a stress by shrinkage of expansion and hardening of insulation layers 9 are relieved, transformation of a warp, distortion, etc. of base substrate (film base material 1A) 1 can be suppressed.

And, because a deformation of base substrate 1 can be suppressed, the yield in the manufacturing process of a semiconductor device improves.

(2)By building dam 8 that surrounds the periphery of vent hole 7, the inflow to vent hole 7 of adhesive material 12 can be stemmed and can be stopped. As a result the prevention of a blockage of vent hole 7 by adhesive material 12 and the going round inwardly of adhesive material 12 to the side of the back of film base material 1A can be prevented.

(3)In case a semiconductor device is looked at from the side of the back of base substrate 1, the arrangement of vent hole 7 to the position that deviated from the center of base substrate 1 can clear a direction as an index.

REPLACEMENT SHEET
30 SEP 1998

(4)By forming insulation layers 9 by the method of printing, low cost of a semiconductor device can be planned as compared with a case that insulation layers 9 formed to the sheet-form is attached and is formed,.

And production rationality of a semiconductor device improves because the pattern shape of insulation layers 9 can be set at freedom.

(5)By using frame structure 20 that film base material 1A was arranged in the area specified in frame body 21, a transfer of film base material 1A in the manufacturing process of a semiconductor device improves, and handling of the manufacturing of a semiconductor device improves.

(6) An alien substance that occurs at the time of sealing and cutting can be reduced by the formation of resin sealing body 14 in the transfer molding method using a molding die assembly with stepped portion 39 that frame body 21 of frame structure 20 is installed and stepped portion 40 that film base material 1A of frame structure 20 is installed in a sub-runner path, because the resin burr that adheres to film base material 1A and frame body 21 can be prevented.

(7)In the state that there is runner resin 41 in frame body 21 of frame structure 20, bump electrodes 15 are connected. In case from this, frame structure 20 is stacked to the multisteps, a protection can be done for bump electrodes 15 of a semiconductor device formed in frame structure 20 of a lower

REPLACEMENT SHEET
30 SEP 1998

position because of the sub-runner resin 41 that is in frame structure 20 of an upper position can keep a space between frame structure 20 of an upper case and frame structure 20 of a lower position. Therefore, a transfer of frame structure 20 improves because it can carry in the state that frame structure 20 was stacked to the multisteps. And, production rationality in the manufacturing process of a semiconductor device improves.

(8)Because insulation layers 9 are arranged on electrode pads 2 for bump connection, when intercalating adhesive material 12 on the chip mount area of main surface of base substrate (film base material 1A) 1 and mounting semiconductor chip 10, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, semiconductor chip 10 does not touch electrode pads 2 for bump connection. Therefore, a short circuit with electrode pads 2 for bump connection and semiconductor chip 10 is prevented, that is, a short circuit with electric conductor layers and semiconductor chip 10 can be also prevented.

And, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, semiconductor chip 10 touches insulation layers 9 and supports it by this insulation layers 9. As a result, a short circuit with electric conductors 3 and semiconductor chip 10 is prevented, that is, a short circuit with electric conductor layers and semiconductor chip 10 can be prevented.

REPLACEMENT SHEET
30 SEP 1998

(9) Transformation of a warp, distortion, etc. of film base material 1A can be suppressed by preparing slit 23 in the adhesion area of frame body 21, because a stress by difference between the materials of frame body 21 and film base material 1A can be reduced.

And, while in the above embodiment, an example of forming insulation layers 9 on electrode pads 2 for bump connection in the chip mount area of base substrate 1 was explained, insulation layers 9 can be formed on electric conductors 3. And, insulation layers 9 can be formed on electrode pads 2 for bump connection and on electric conductors 3. In case of these, when intercalating adhesive material 12 on the chip mount area of main surface of base substrate (film base material 1A) 1 and mounting semiconductor chip 10, likewise with the above embodiment, even if it is mounted in the state that semiconductor chip 10 tilted, and the film thickness of adhesive material 12 thins, a short circuit with electrode pads 2 for bump connection and an electric conductors 3 can be prevented, that is, a short circuit with electric conductor layers and semiconductor chip 10 can be prevented.

And, as it is shown in Fig. 21 (main part cross-sectional view of a semiconductor device) and Fig. 22 (plan view of a base substrate), insulation layers 9 can be divided into several on base substrate 1 to arrange insulation layers 9 on electric conductors 3 that was the peripheral area of main surface of base

REPLACEMENT SHEET
30 SEP 1998

substrate 1 and was formed to the area between semiconductor chip 10 and electrode pads 4 for wire connection. In this case, because wires 13 do not touch to electric conductors 3, a short circuit with other electric conductors 3 that adjoin electric conductors 3 electrically connected to wires 13 and these wire 13 can be prevented, that is, electric conductor layers and wires 13 can be prevented from short-circuiting.

And, as it is shown in Fig. 23 (plan view of a base substrate) and Fig. 24 (main part cross-sectional view of a semiconductor device), insulation layers 9 are divided into every electric conductor layers on base substrate 1. And then, insulation layers 9 can be formed to all areas of electric conductor layers (electrode pads 2 for bump connection, electric conductors 3 and electric conductors 5 for plating) except electrode pads 4 for wire connection. In this case, even if a conductive foreign material adheres between electric conductor layers in the manufacturing process of a semiconductor device, a short circuit between electric conductor layers can be prevented because a conductive foreign material does not touch a electric conductor layers.

And, as it is shown in Fig. 25 (plan view of a base substrate) insulation layers 9 can be divided into several on base substrate 1, and this divided insulation layers 9 can be arranged on the electric conductor layers. As for each of several insulation layers 9, a plane is formed in the square-form, a specified space is put, and a matrix-form arranges it.

REPLACEMENT SHEET
30 SEP 1998

And, as it is shown in Fig. 26 (plan view of a base substrate), insulation layers 9 can be divided into several on base substrate 1, and this divided insulation layers 9 can be arranged on the electric conductor layers. Each of several insulation layers 9 is formed to the long plate form and is radially arranged in the state that a specified space was put.

And, even though a spherical bump electrode 15 was explained as an example electrode that is arranged to the side of the back of base substrate 1 while in the above embodiment, as an electrode of this invention, a protruding portion electrode like a stud bump or even electrode that is formed by the method of ball bonding can be used.

While this invention was concretely explained on the basis of the above embodiment, this invention is not limited to the above embodiment only, and it is possible to change it variously in the range that does not deviate from the gist of the invention.

If the effect that is obtained by a representative in the invention that is disclosed in this application is easily explained as follows.

In the semiconductor device with the base substrate that comprises of flexible films, a deformation (warp and distortion) of a base substrate can be suppressed.

In the semiconductor device with the base substrate that comprises of flexible films, a deformation of a base substrate can be suppressed and a short circuit with the electric conductor of

REPLACEMENT SHEET
30 SEP 1998

a base substrate and a semiconductor chip can be prevented.

In the semiconductor device with the base substrate that comprises of flexible films, a deformation of a base substrate can be suppressed and the electric conductor layers of a base substrate and wires can be prevented from short-circuiting.

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REPLACEMENT SHEET
30 SEP 1998

What is claimed is;

1. A semiconductor device comprising :

a film substrate having a first surface and a second surface that is opposed on the first surface ;

a plurality of electric conductor layers formed on the first surface of said substrate;

a semiconductor chip mounted through an adhesive material on the first surface of said substrate and arranged on said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers;

a resin member formed on said first surface and sealing said semiconductor chip, said electric conductor layers and said bonding wires;

an insulation layer formed between said electric conductor layers and said semiconductor chip;

wherein said insulation layer has plural parts which are separated each other in a plane view in the area on which said

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REPLACEMENT SHEET
30 SEP 1998

semiconductor chip is mounted.

2.A semiconductor device according to claim 1, wherein said substrate comprises a flexible film.

3.A semiconductor device according to claim 1, wherein said substrate has a plurality of connection holes that reache said second surface from said first surface at the position that corresponds to the under area of said electric conductor layers, and wherein said bump electrodes are connected to said electric conductor layers through said connection holes.

4.A semiconductor device according to claim 1, wherein each of said electric conductor layers having a first part that is positioned in the area under said semiconductor chip and a second part that is positioned in the area outside of said semiconductor chip, the second part begin continuously formed with said first part, and wherein said bonding wires are connected to the second parts of said electric conductor layers.

5.A semiconductor device according to claim 1, wherein said insulation layer comprises a photosensitive resin film.

6.A semiconductor device comprising :

a film substrate having a first surface and a second

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REPLACEMENT SHEET
30 SEP 1998

surface that is opposed on the first surface ;

a semiconductor chip mounted through an adhesive material on the first surface of said substrate, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main face;

a plurality of electric conductor layers formed on said first surface of said substrate, and formed between said semiconductor chip and said substrate;

each of said electric conductor layers having a first part that is positioned in the area under said semiconductor chip and a second part that is positioned in the area outside of said semiconductor chip, the second part being continuously formed with said first part, and the first part having bump land at the one end;

a plurality of bonding wires to which the second parts of said electric conductor layers and said external terminals are electrically connected;

a plurality of bump electrodes arranged on said second surface and electrically connected to said electric conductor layers;

said substrate having a plurality of connection holes that reach said second surface from said first surface at the position that corresponds to said bump lands of electric conductor layers, said bump electrode being connected to said bump lands

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REPLACEMENT SHEET
30 SEP 1998

through said connection holes;

a resin member formed on said first surface and sealing said semiconductor chip, said electric conductor layers and said bonding wires;

a plurality of insulation layer patterns formed between said semiconductor chip and each of bump lands of electric conductor layers;

wherein said insulation layer patterns are separated each other in a plane view.

7.A semiconductor device according to claim 6 , wherein said substrate comprises a flexible film.

8.A semiconductor device according to claim 7 , wherein each of said insulation layer patterns comprises a photosensitive resin film.

9.A semiconductor device having a semiconductor chip mounted through an adhesive material on a surface of a flexible film that the plural number of electric conductor layer is arranged to a main surface of a base substrate composed of the flexible film,

wherein said semiconductor chip is mounted on said plural number of electric conductor layer,

an insulation layer is formed between said plural number

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REPLACEMENT SHEET
30 SEP 1998

of electric conductor layer and said semiconductor chip,

said insulation layer is divided into the plural number of part in the area under said semiconductor chip.

10.A semiconductor device having a semiconductor chip mounted through an adhesive material on the chip mount area of the main surface of a base substrate in which a vent hole is formed to the chip mount area of the main surface of a base substrate composed of flexible films,

wherein a dam that surrounds the periphery of said vent hole is formed in the chip mount area of said main surface of a base substrate.

11.A semiconductor device according to claim 10,

wherein said vent hole is arranged to the position that deviated from the center of said base substrate.

12.A semiconductor device according to claim 10,

wherein said adhesive material comprises thermo hardening resins.

13.A method for manufacturing a semiconductor device comprising the steps of:

A) preparing a lead frame made of metal that supplies the

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REPLACEMENT SHEET
30 SEP 1998

plural number of area partitioned by a frame body.

B) supplying film substrate to said plural number of area, said substrate has first surface, second surface that is opposed on said first surface and the plural number of electric conductor layer formed on the first surface;

C) mounting a semiconductor chip through an adhesive material on the first surface of said plural number of substrate, this semiconductor chip has the plural number of semiconductor element and the plural number of outside terminal formed on its main surface and is mounted on said plural number of electric conductor layer.

D) electrically connecting the plural number of outside terminal of said semiconductor chip and said plural number of electric conductor layer by using the plural number of wire.

E) sealing said semiconductor chip, said plural number of electric conductor layer and said plural number of wire by resin.

F) forming the plural number of bump electrode on the second surface of said substrate.

14.A method for manufacturing a semiconductor device according to claim 13, further comprising the step for cutting said lead frame made of metal to said plural number of area in order to form the plural number of resin molded semiconductor package after said step F).

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REPLACEMENT SHEET

3 0 SEP 1998

15. A method for manufacturing a semiconductor device according to claim 13,

wherein said step E) comprises a transfer mold using a die assembly and further including a step for leaving a stiffened runner resin positioned inside of said frame body and removing stiffened runner resin positioned outside of said frame body.

16. A method for manufacturing a semiconductor device according to claim 13,

wherein said step B) includes a step for fixing said substrate to the frame body of a lead frame made of metal by an adhesive material.

17. A method for manufacturing a semiconductor device according to claim 16,

wherein said frame body having slits in the adhesion area of said frame body and said substrate.

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30 SEP 1998

ABSTRACT OF THE DISCLOSURE

Ball Grid Array type semiconductor package is disclosed. A semiconductor chip is mounted through an adhesive material on a surface of a flexible film substrate. The plural of bump electrode are arranged in array to the opposite side of said substrate and the semiconductor chip is sealed by resin.

Concretely, an insulation layer is formed to cover an electric conductor layer pattern formed on the surface of the substrate, and the semiconductor chip is mounted through an adhesive material on the insulation layer.

The above insulation layer is divided into the plural number of part that is mutually discontinuous in the area under the above semiconductor chip. By this divided insulation layer, the short circuit between above semiconductor chip and above electric conductor layer pattern is prevented and the deformation of the substrate that comprises the above flexible films is suppressed.

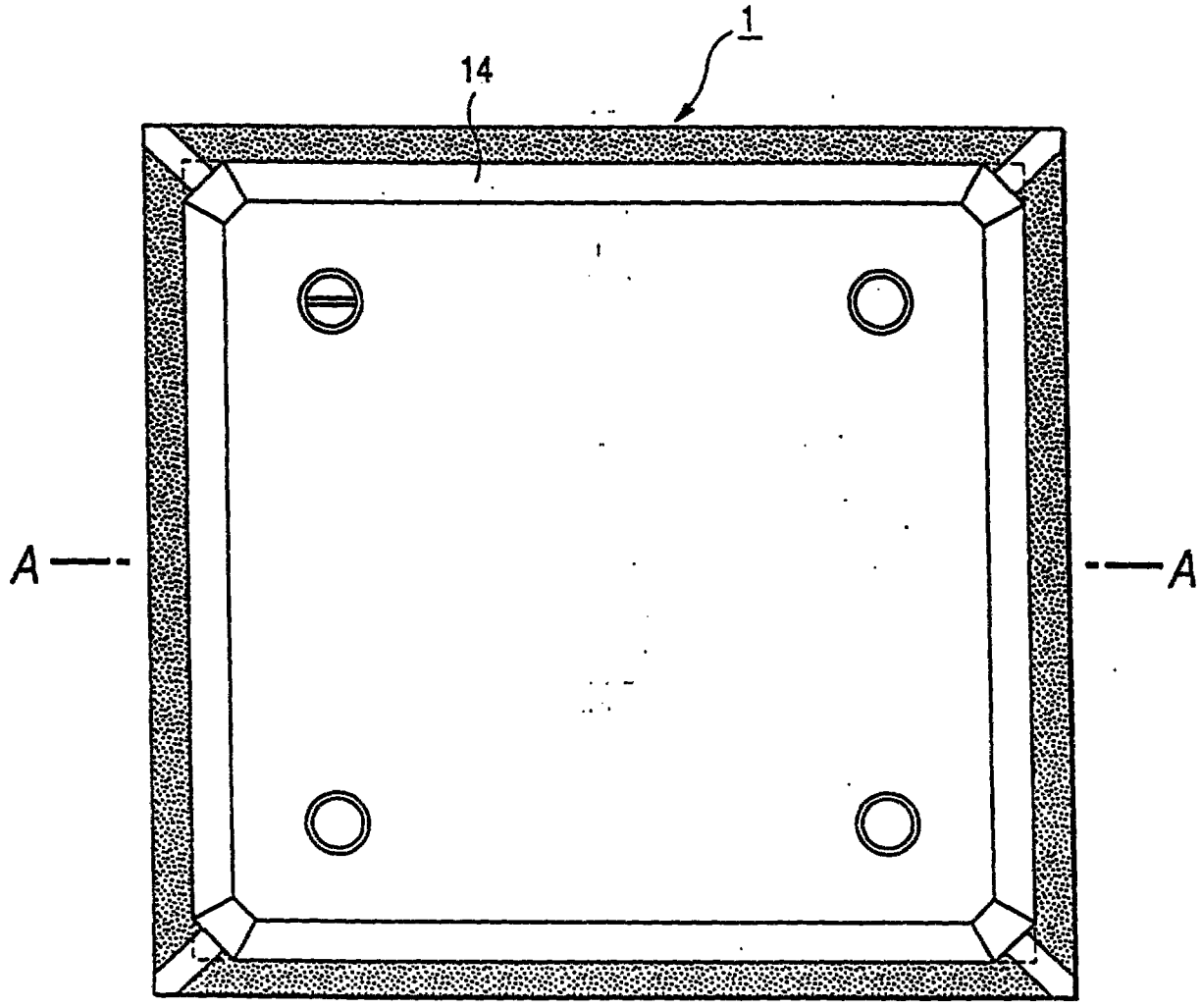
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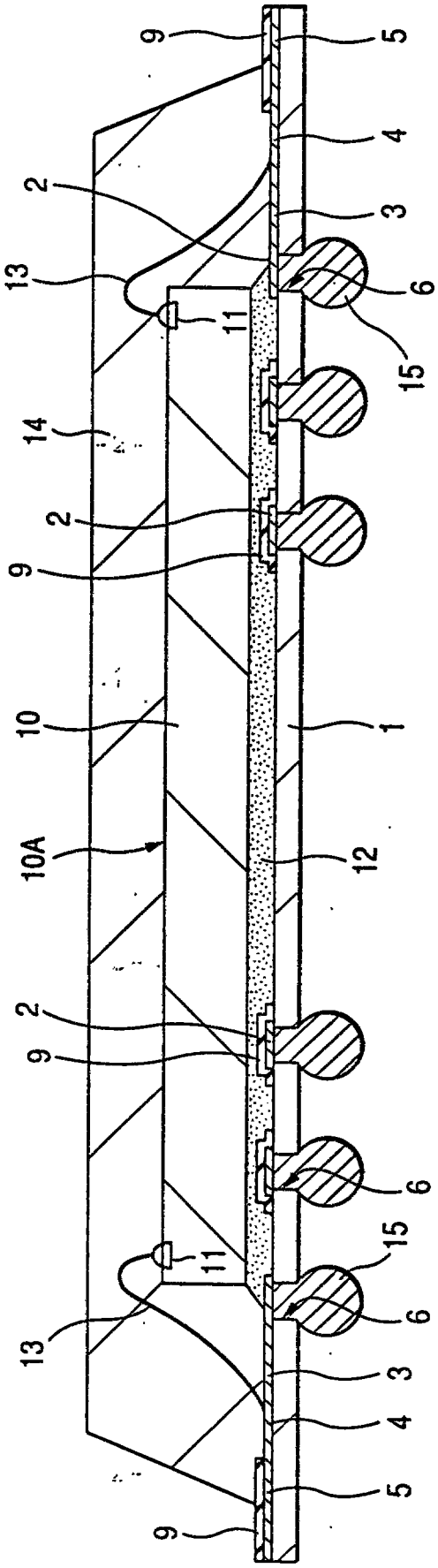
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30 SEP 1998

FIG. 1



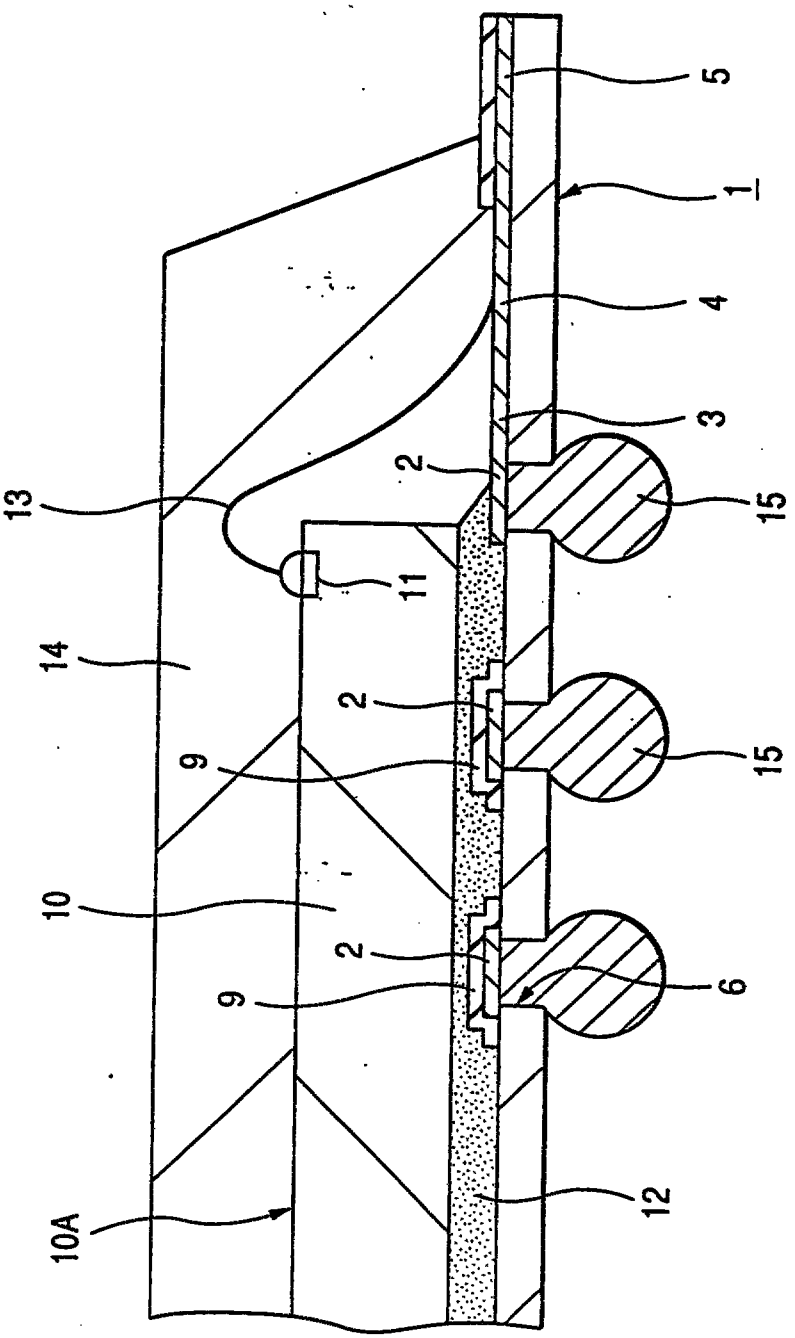
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30 SEP 1998

FIG. 2



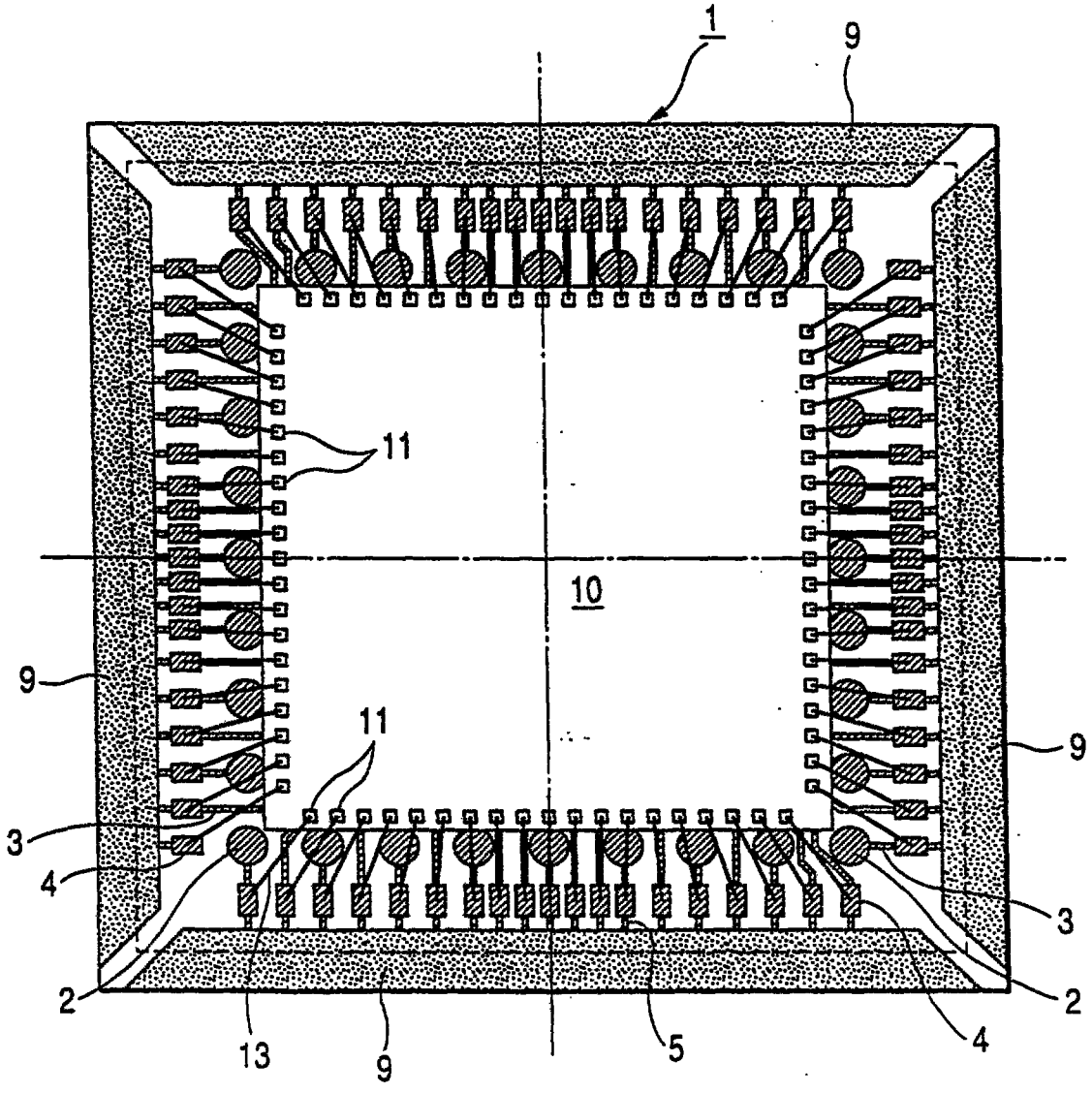
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30 SEP 1998

FIG. 3



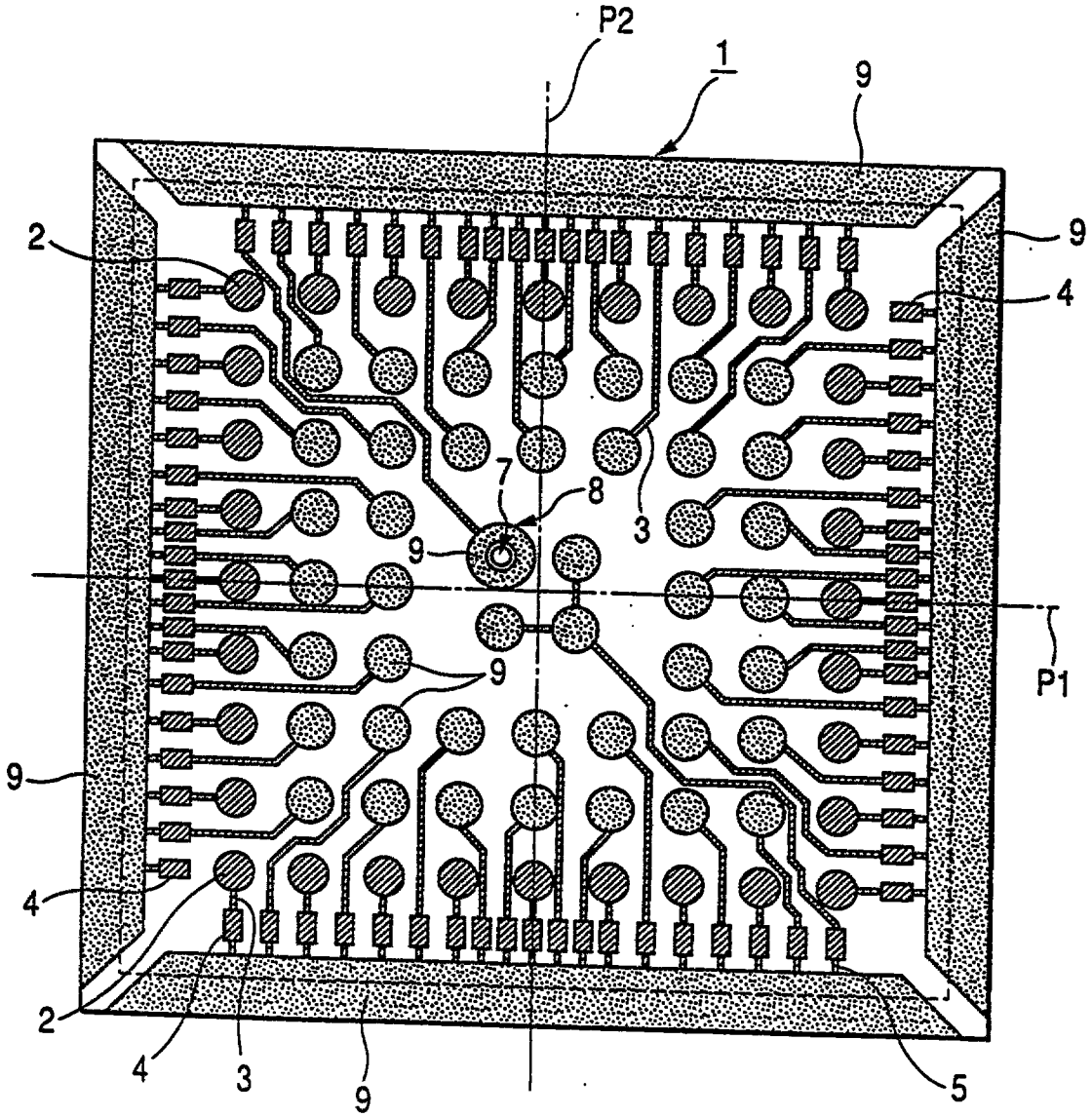
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30 SEP 1998

FIG. 4



REPLACEMENT SHEET
30 SEP 1998

FIG. 5



REPLACEMENT SHEET
30 SEP 1998

FIG. 6

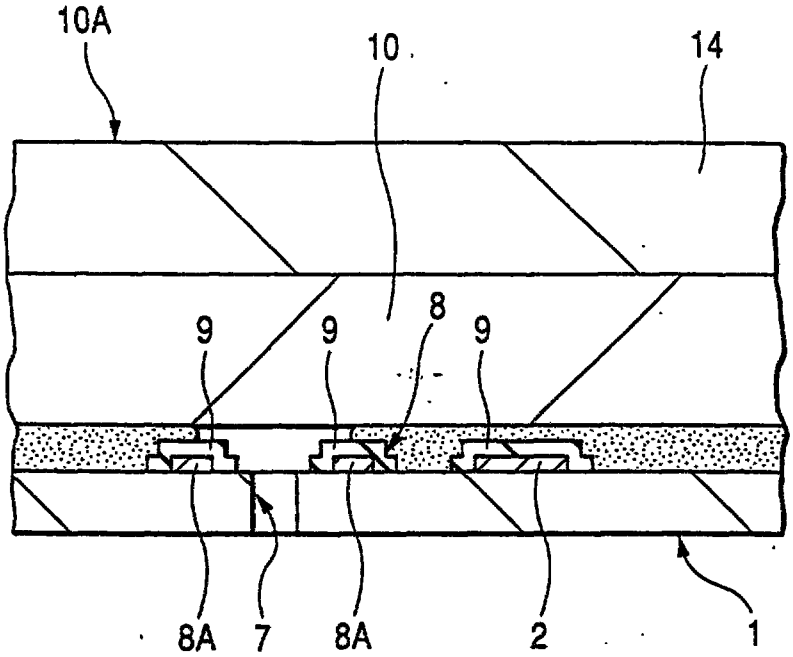
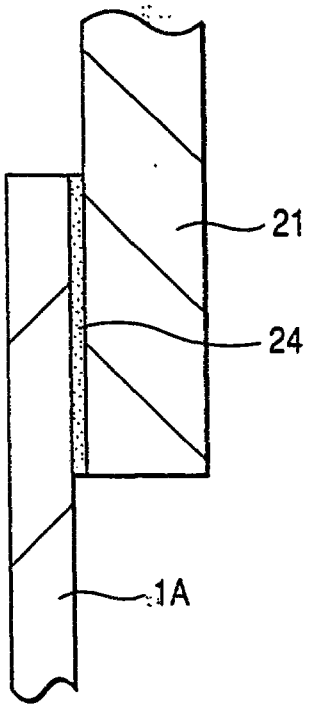
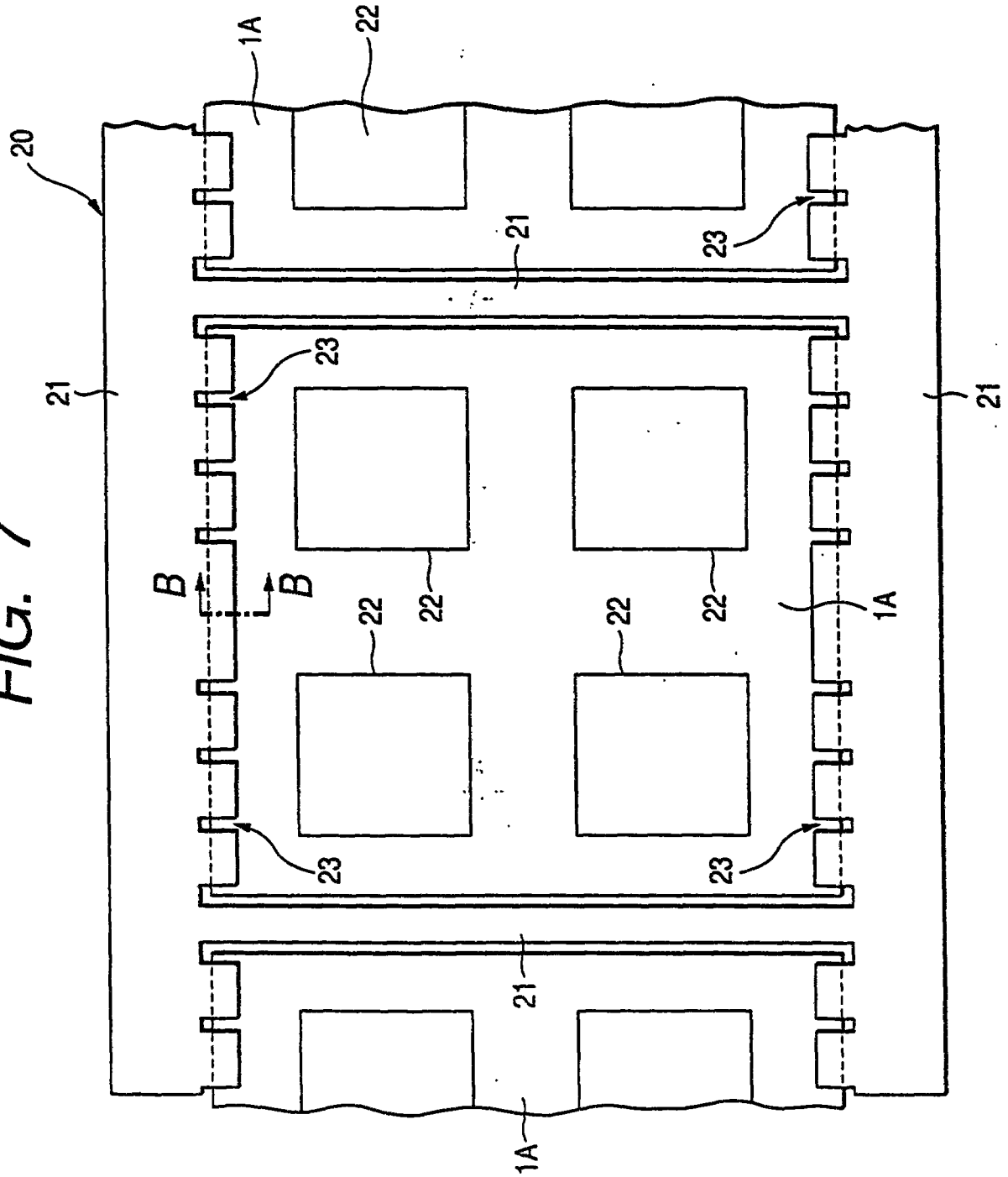


FIG. 8



REPLACEMENT SHEET
30 SEP 1998

FIG. 7



REPLACEMENT SHEET
30 SEP 1998

FIG. 9(A)



FIG. 9(B)

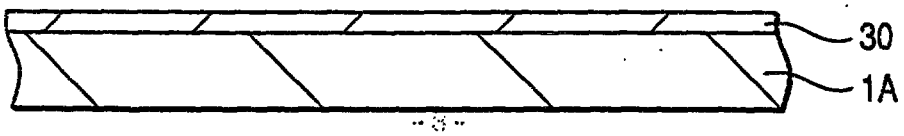


FIG. 9(C)

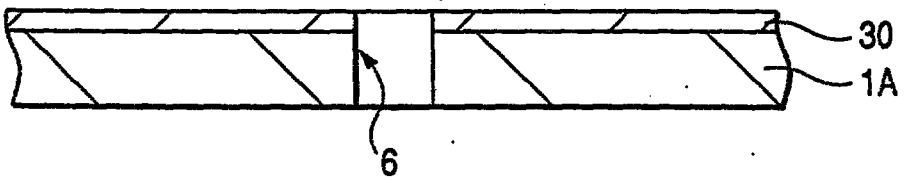


FIG. 9(D)

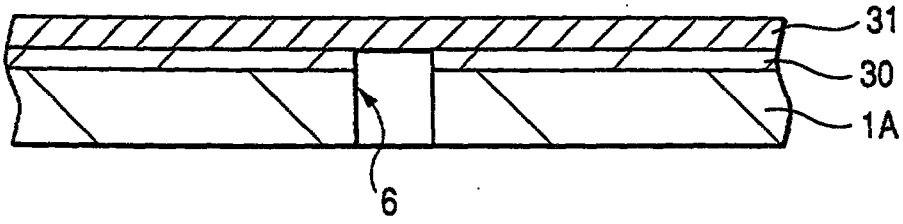
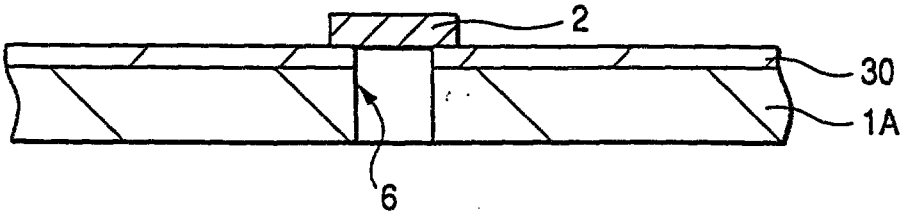


FIG. 9(E)



REPLACEMENT SHEET
30 SEP 1998

FIG. 10(F)

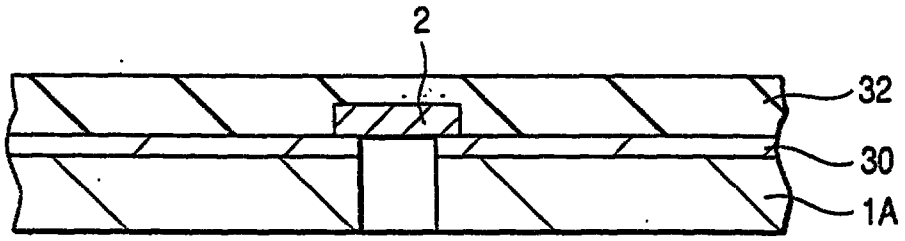
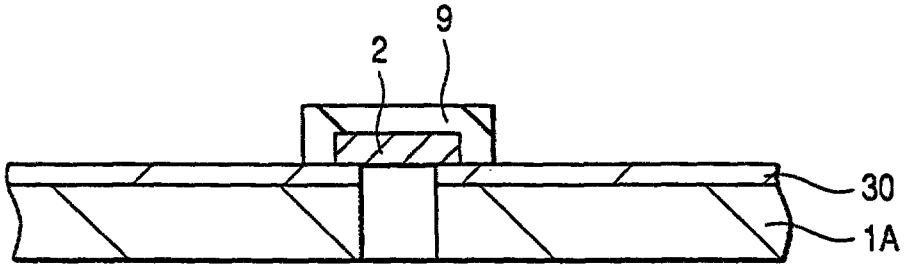


FIG. 10(G)



REPLACEMENT SHEET
30 SEP 1999

FIG. 11

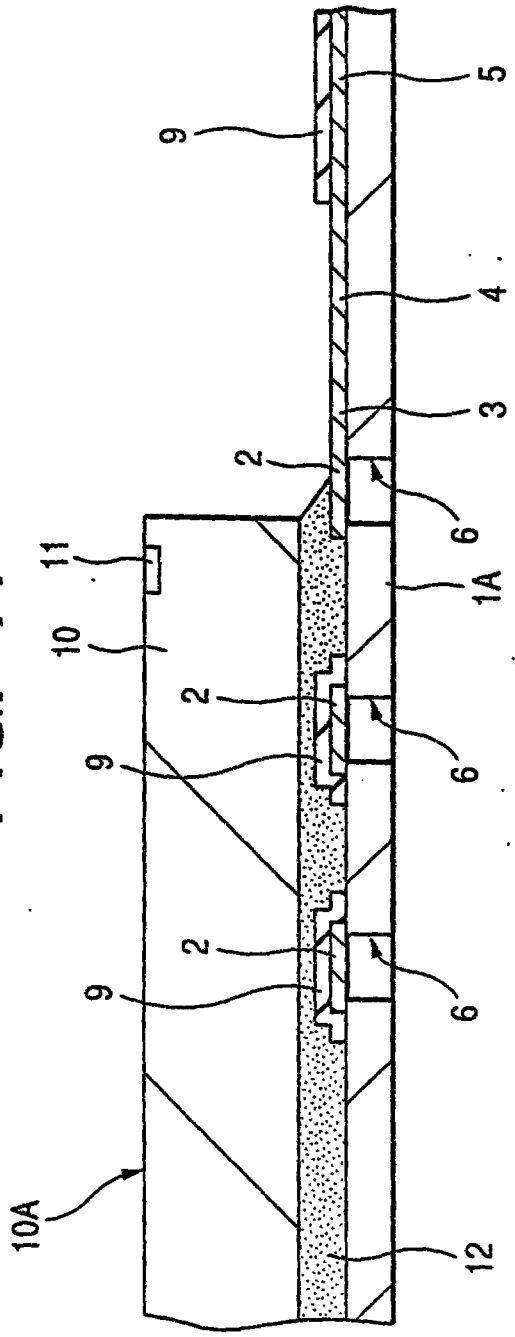
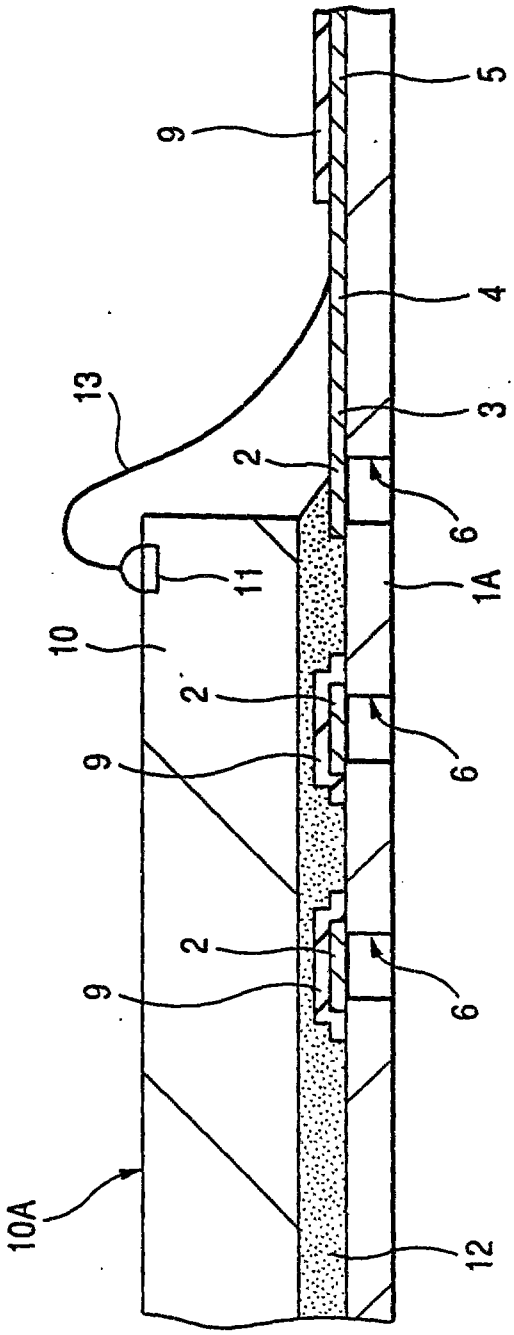
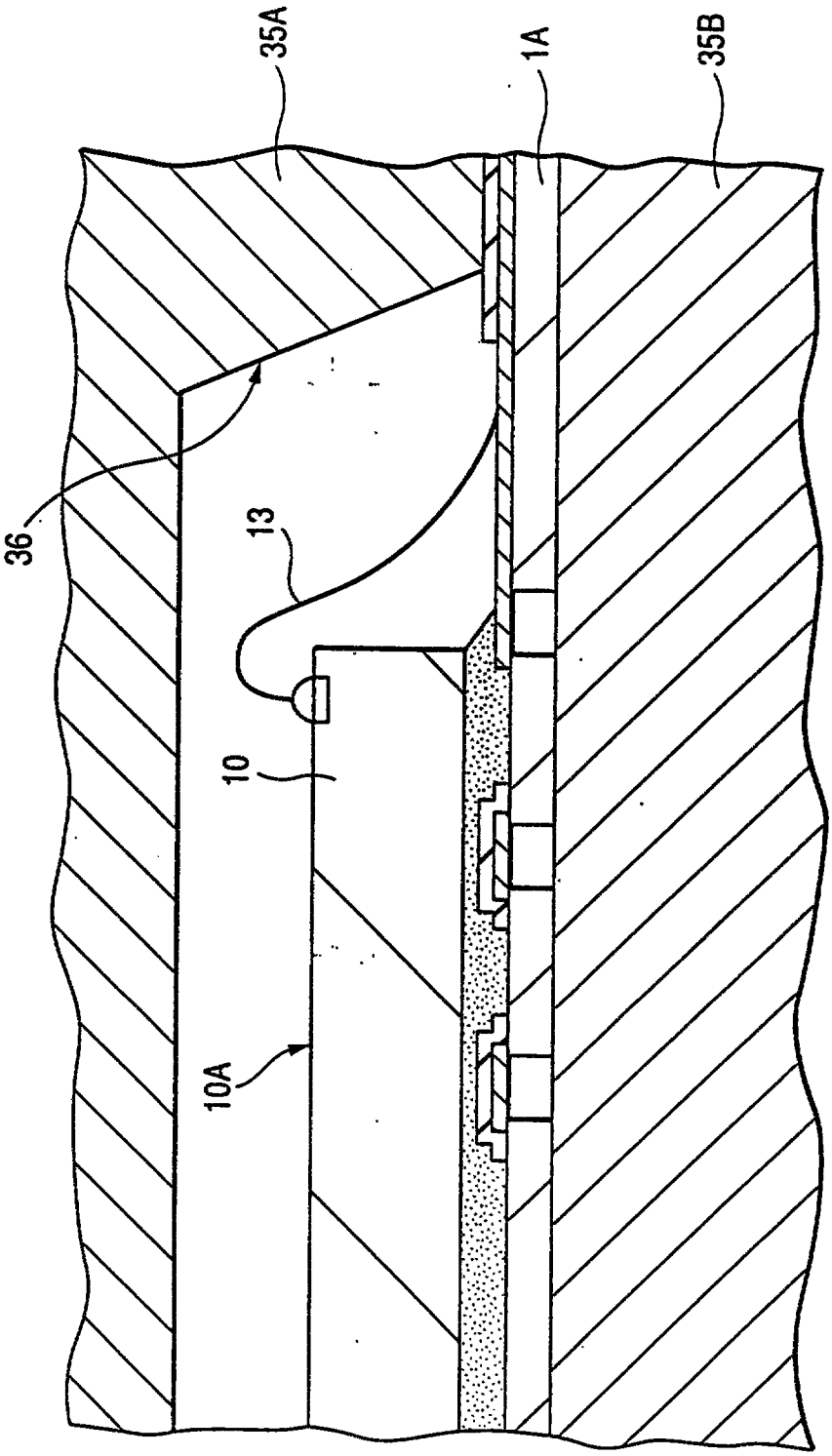


FIG. 12



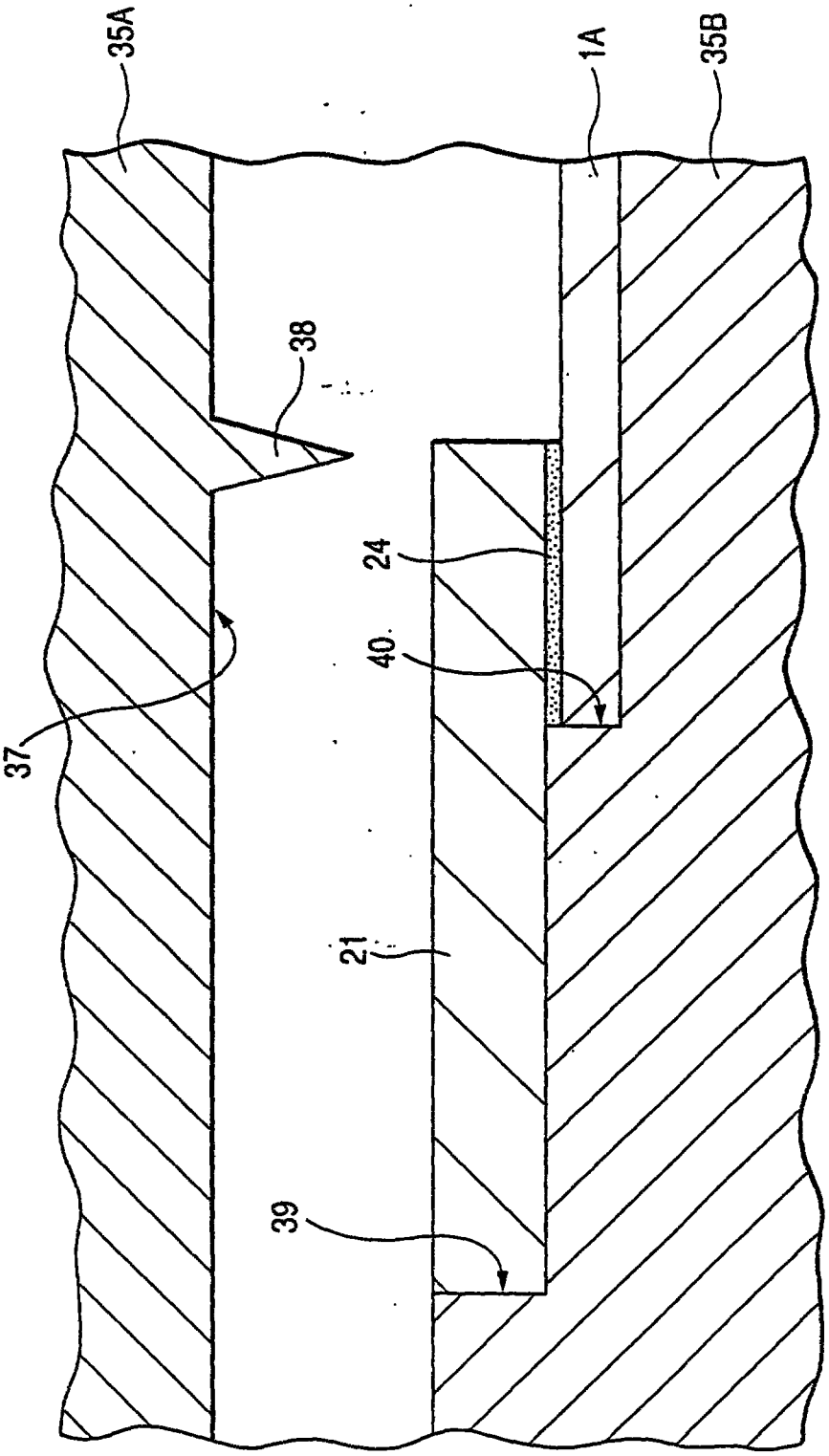
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FIG. 13



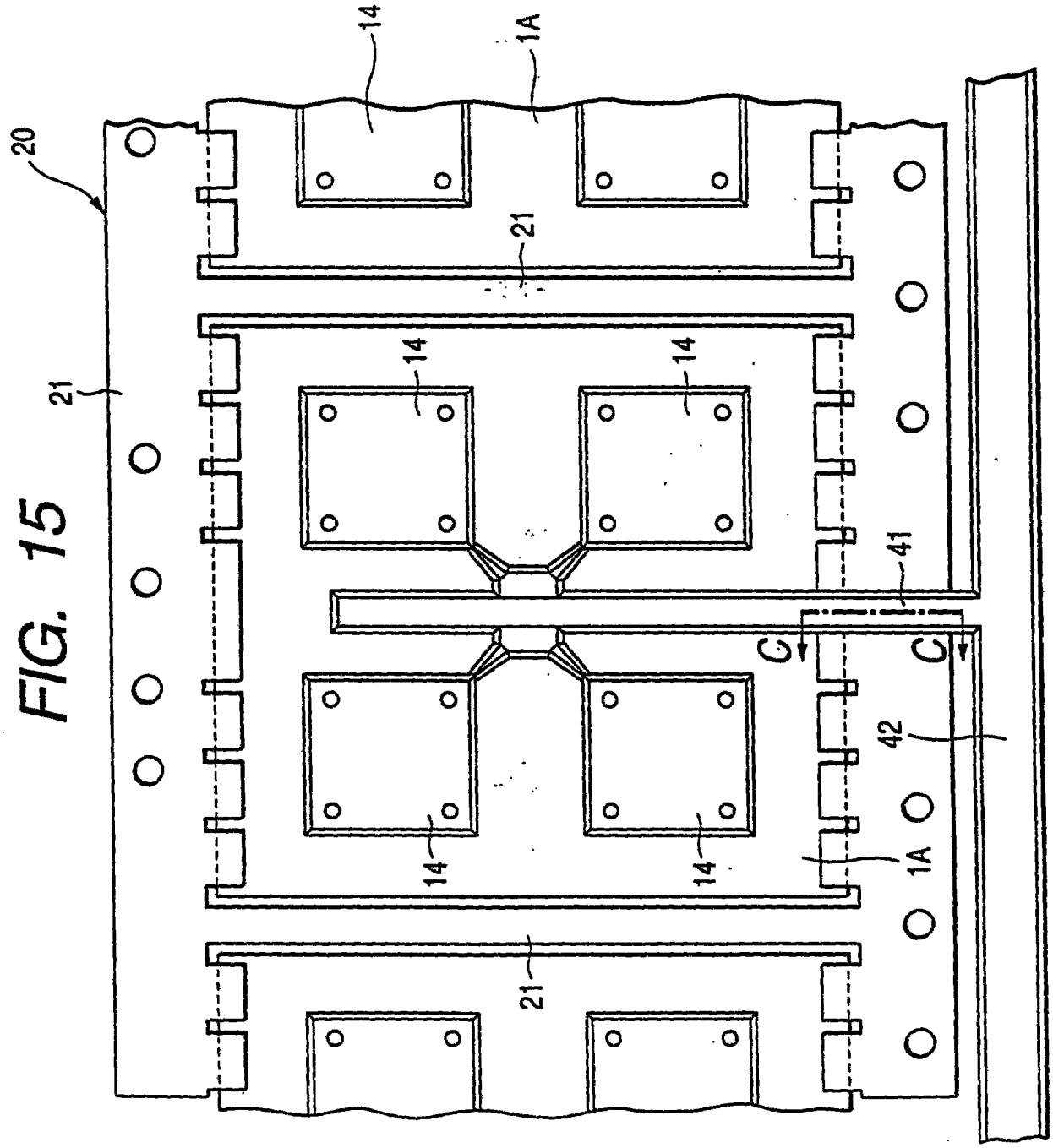
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FIG. 14



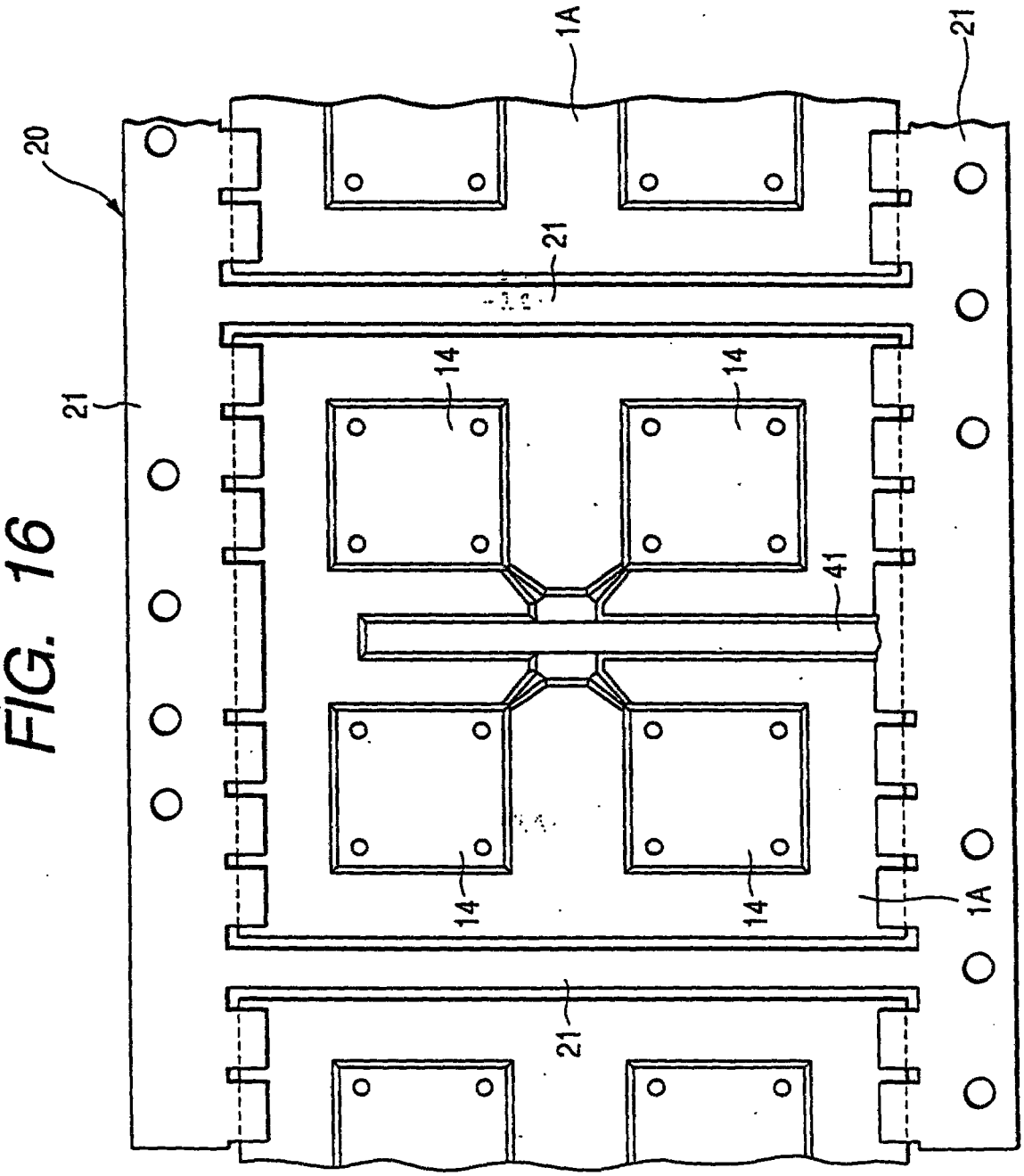
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FIG. 15



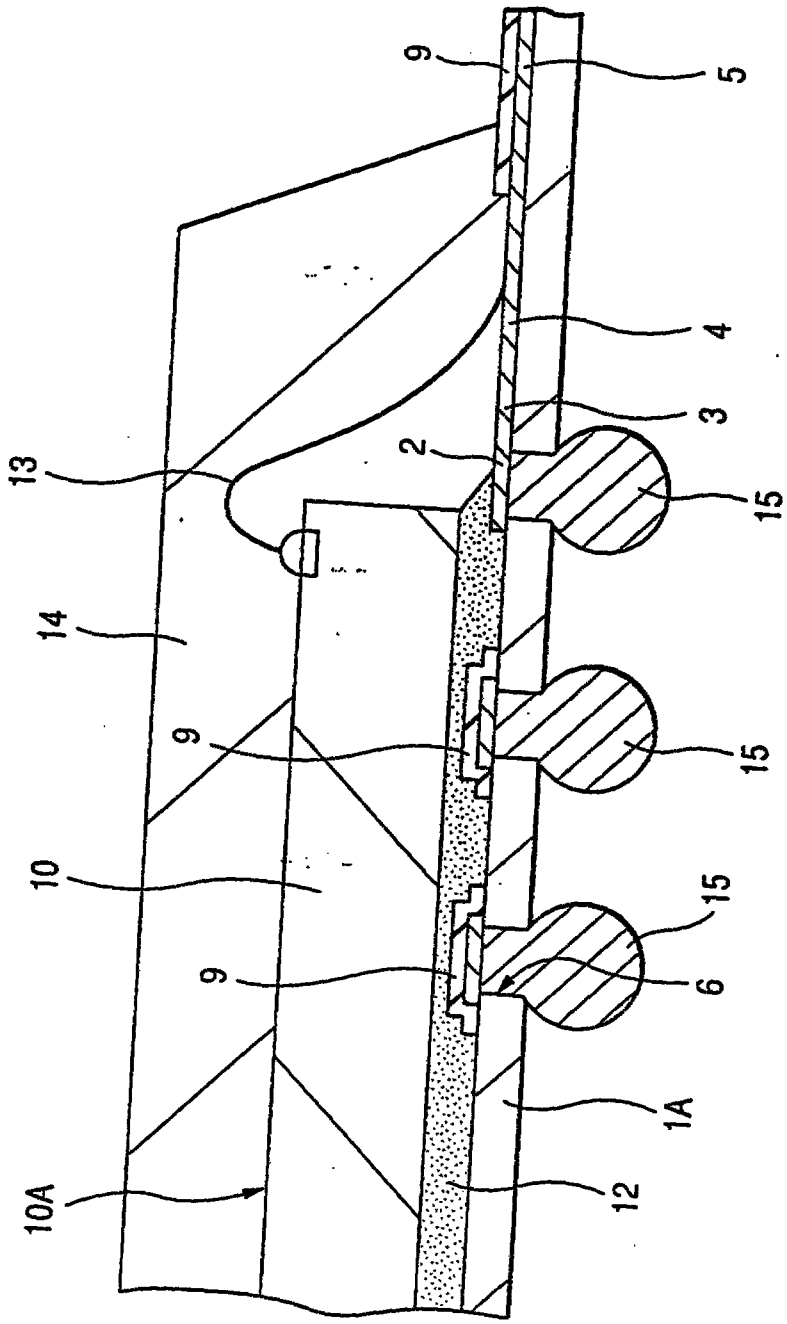
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FIG. 16



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FIG. 17



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FIG. 18

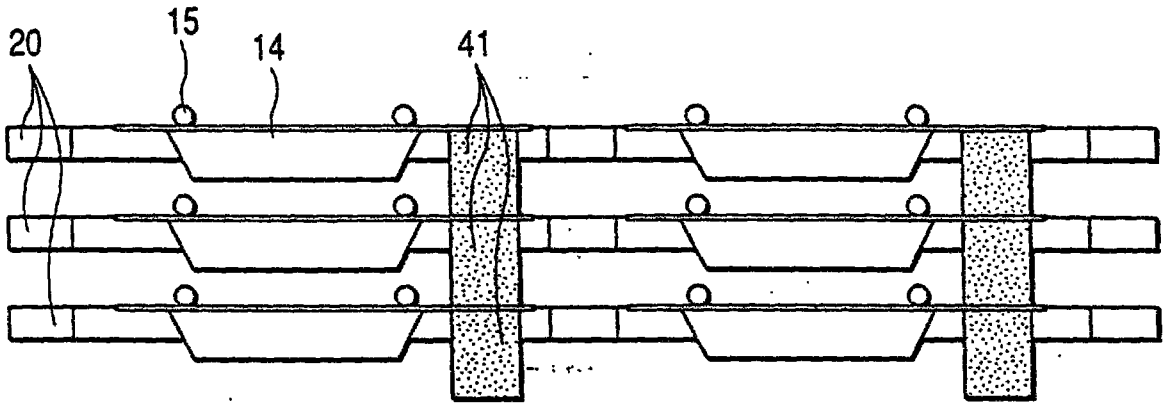


FIG. 19

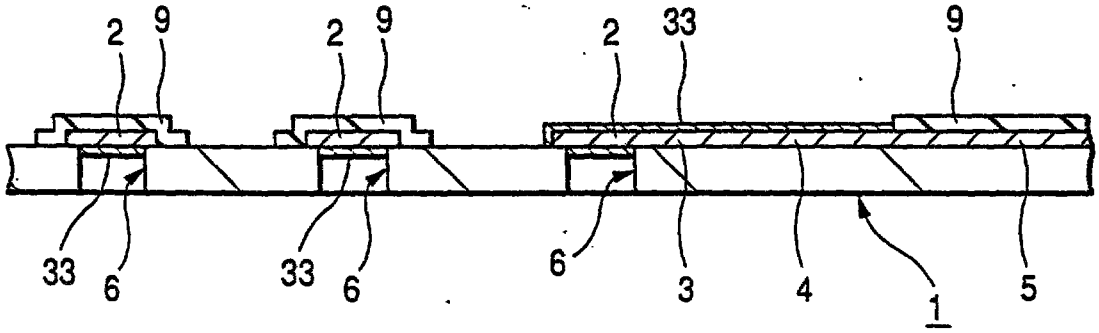
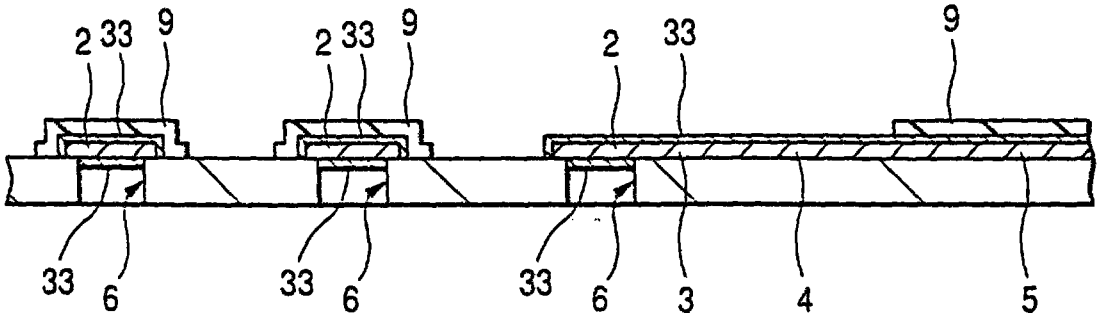
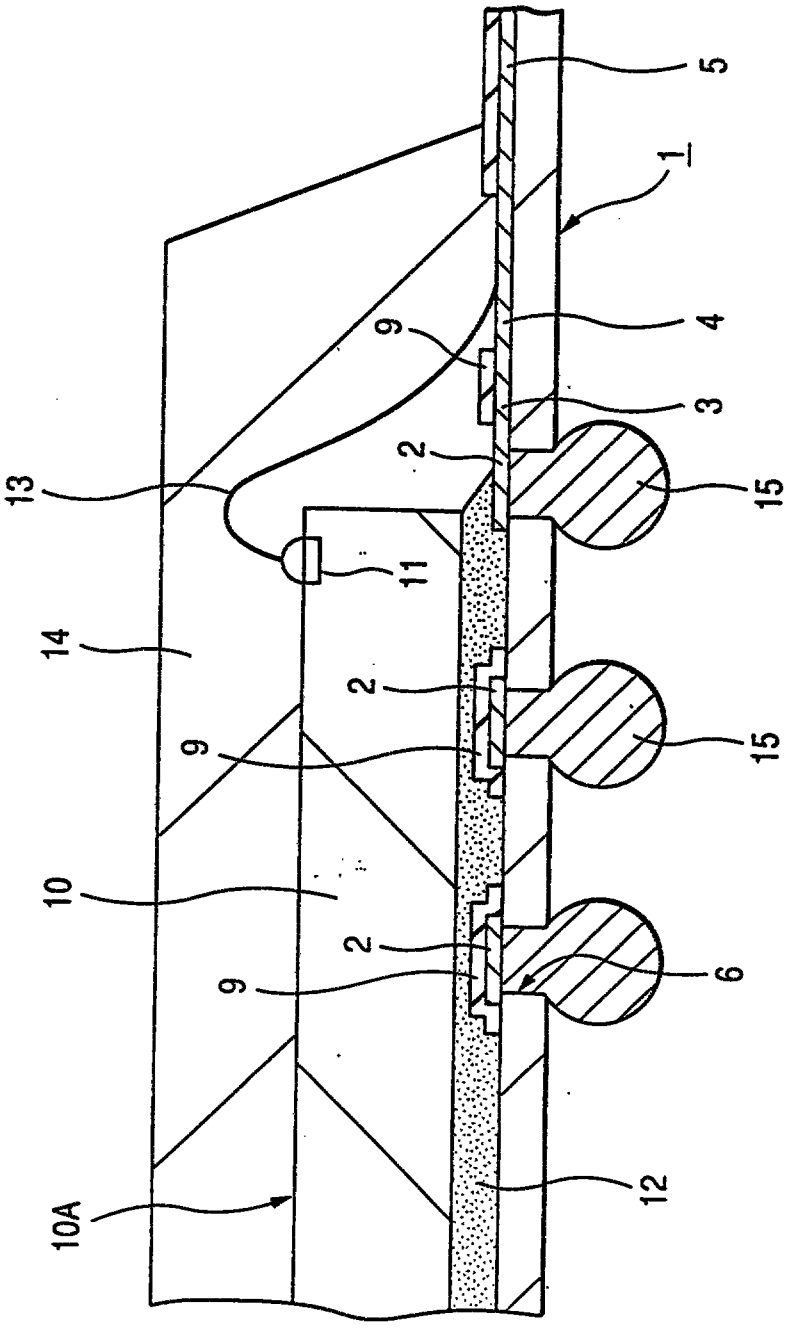


FIG. 20



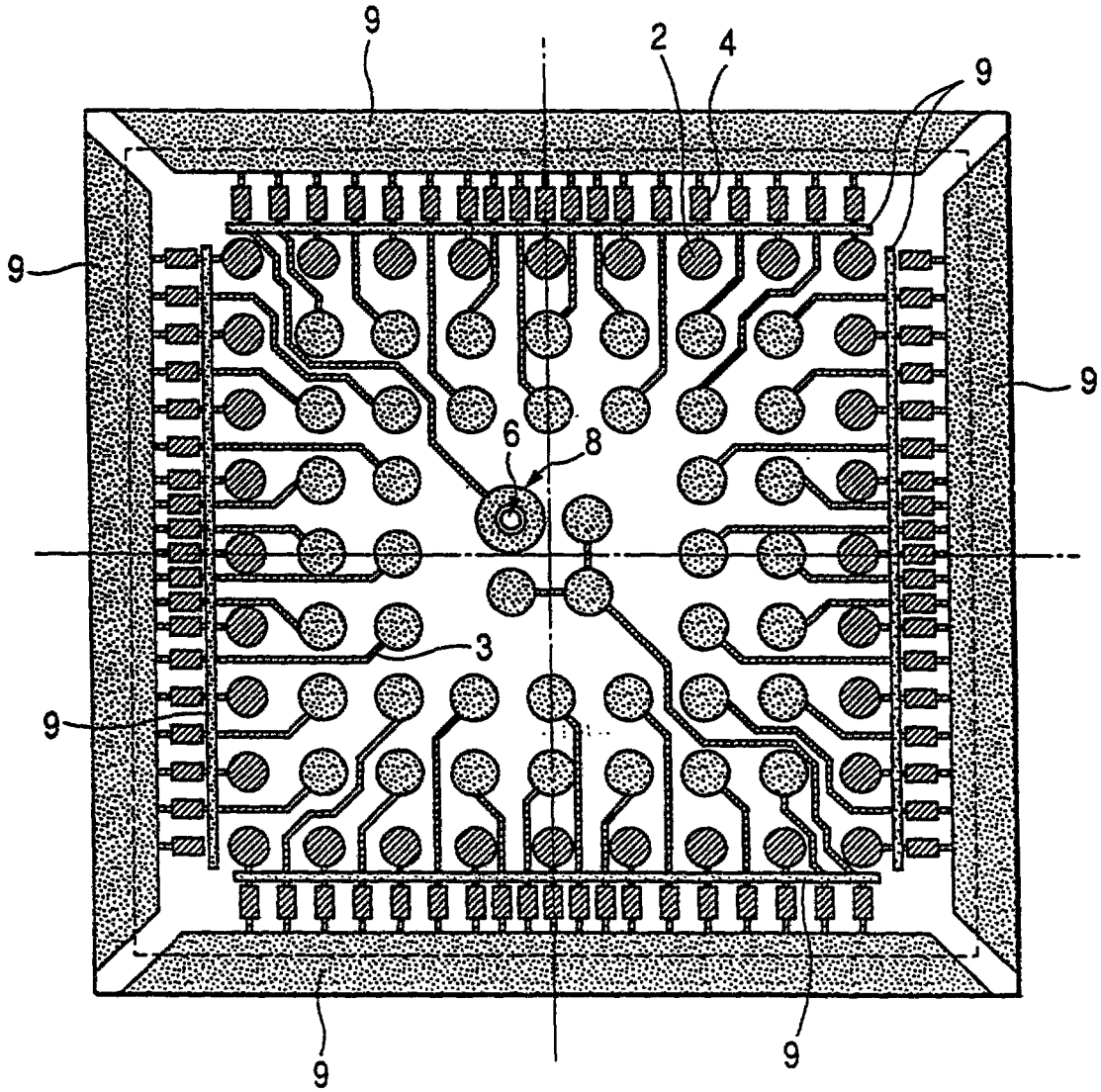
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FIG. 21



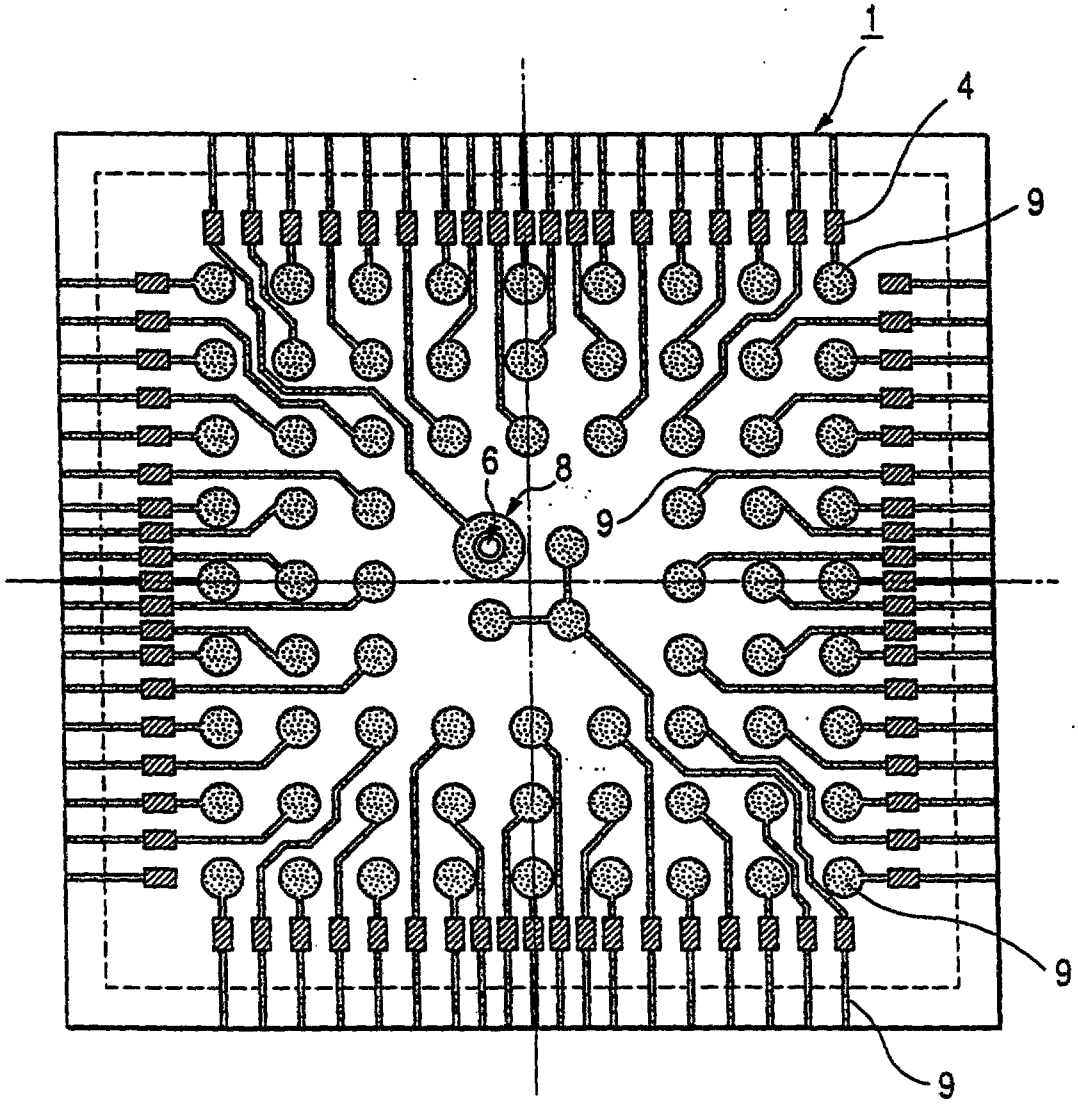
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FIG. 22



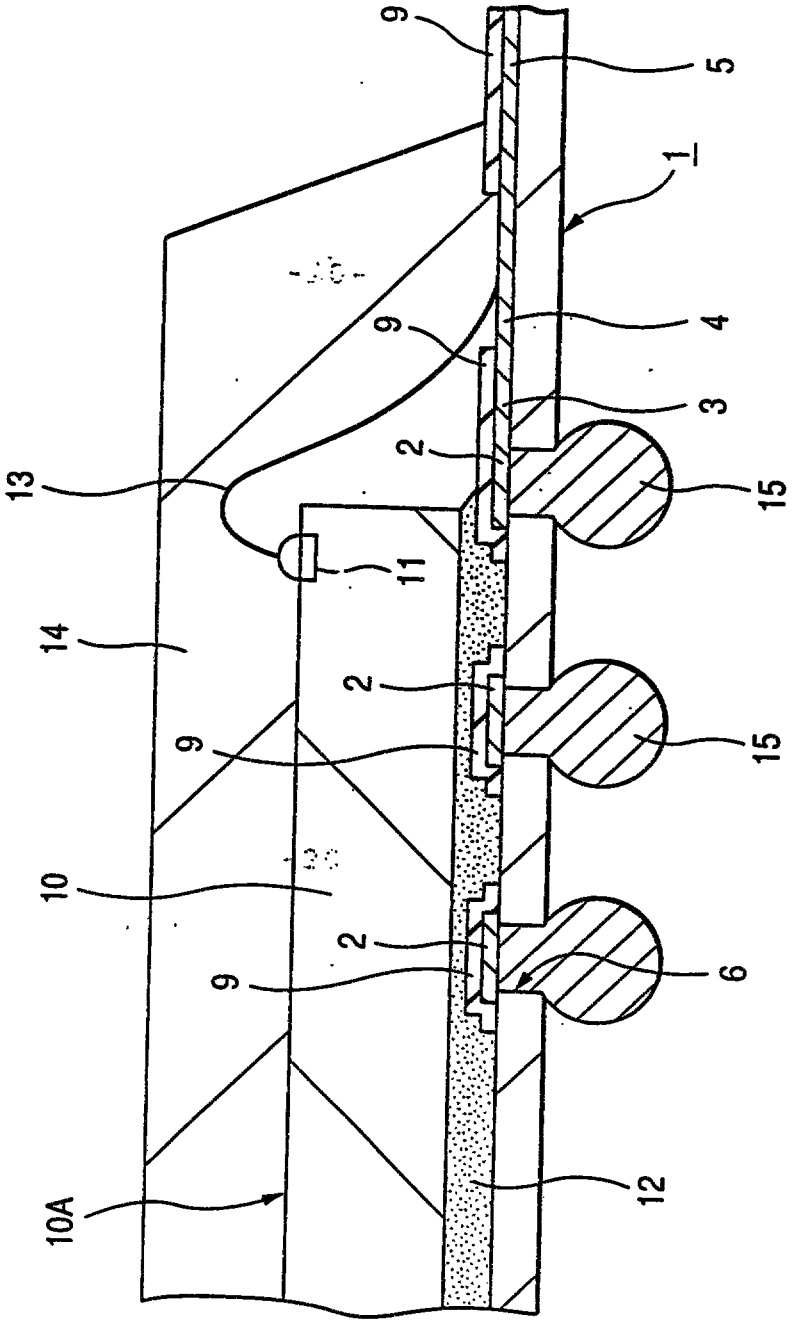
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FIG. 23



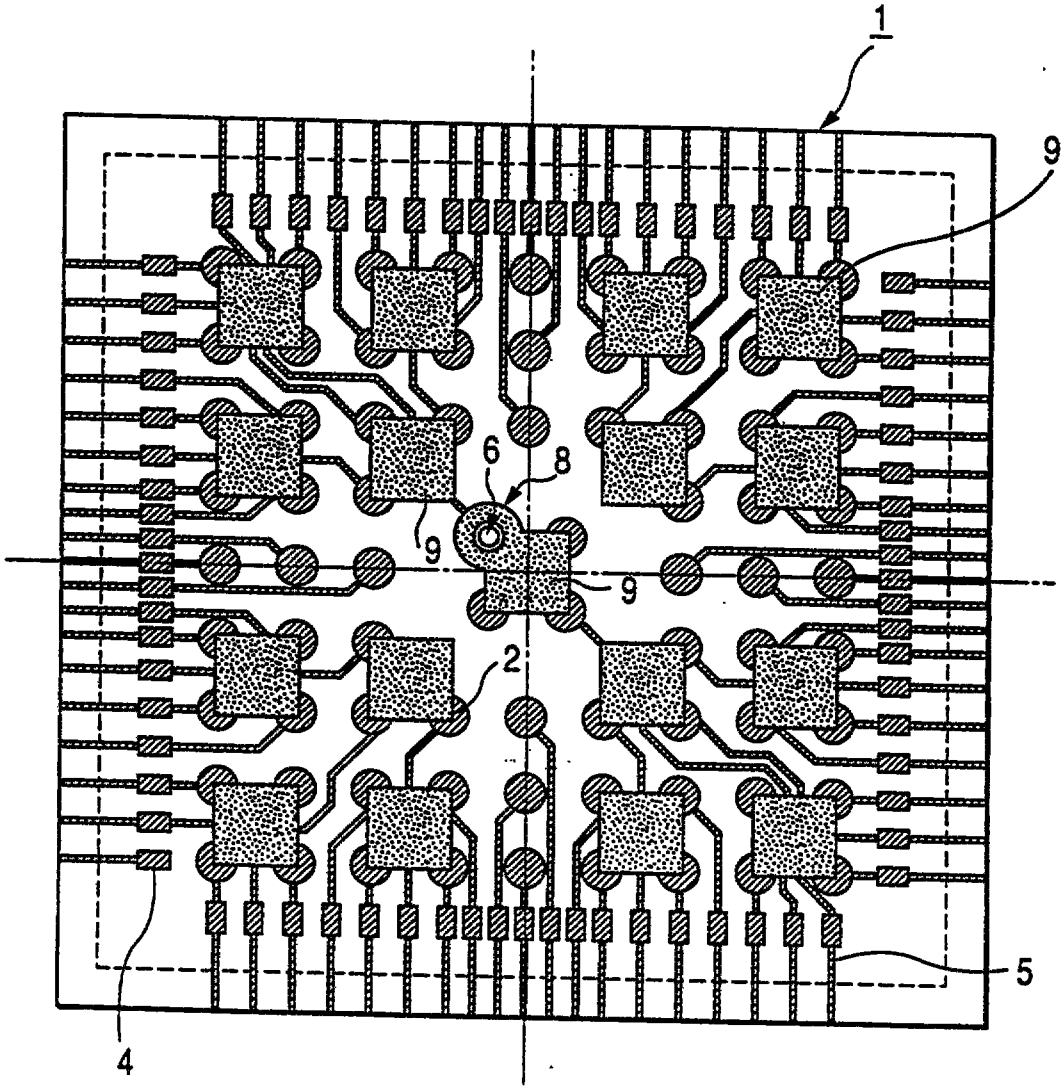
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FIG. 24



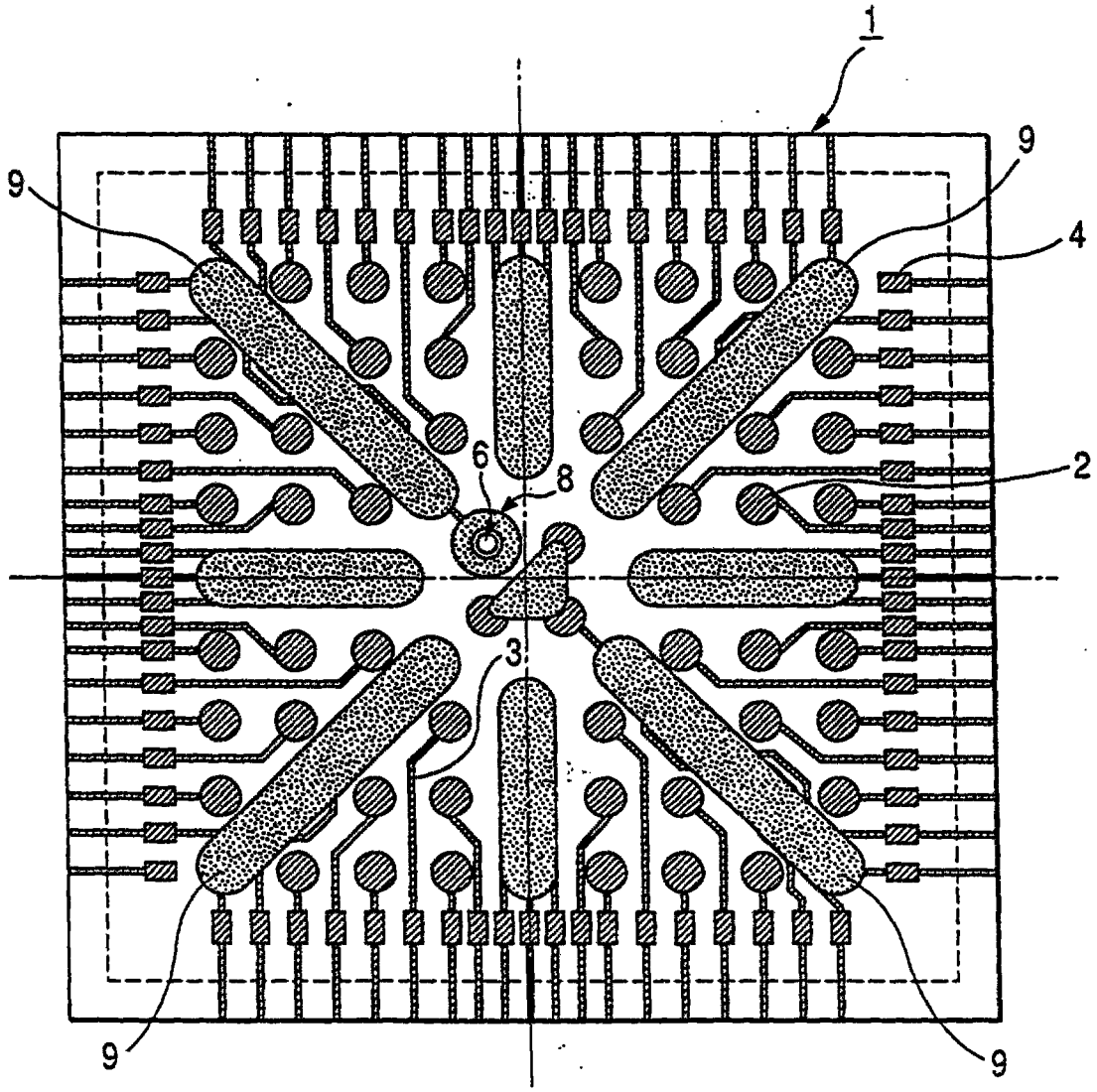
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FIG. 25



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30 SEP 1998

FIG. 26



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SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

ABSTRACT OF THE DISCLOSURE

Ball Grid Array type semiconductor package is disclosed. A semiconductor chip is mounted through an adhesive material on a surface of a flexible film substrate. The plural of bump electrode are arranged in array to the opposite side of said substrate and the semiconductor chip is sealed by resin.

Concretely, an insulation layer is formed to cover an electric conductor layer pattern formed on the surface of the substrate, and the semiconductor chip is mounted through an adhesive material on the insulation layer.

The above insulation layer is divided into the plural number of part that is mutually discontinuous in the area under the above semiconductor chip. By this divided insulation layer, the short circuit between above semiconductor chip and above electric conductor layer pattern is prevented and the deformation of the substrate that comprises the above flexible films is suppressed.

Figure 1

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REPLACEMENT SHEET
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1. A semiconductor device comprising:

a base substrate which is made of film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of insulation layers formed between said electric conductor layers and said semiconductor chip;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers; and

a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires;

wherein said insulation layers are separated each other in a plane view in an area on which said semiconductor chip is mounted.

2. A semiconductor device according to claim 1, further comprising:

a plurality of land pads formed on each end of said electric conductor layers and arranged in said area;

wherein each said insulation layers are formed on each of said land pads so as to cover a part of each of said land pads.

3. A semiconductor device according to claim 1, further comprising:

a plurality of land pads formed on each end of said electric conductor layers and arranged in said area;

wherein each said insulation layers are covered each of said land pads.

4. A semiconductor device according to claim 1, wherein said base substrate having square-form in a plane view, said insulation layer is divided into multiplicity correspond to a side of said base substrate.

5. A semiconductor device according to claim 1, wherein said base substrate is made of insulation resin of epoxy.

6. A semiconductor device according to claim 1, wherein said base substrate is made of insulation resin of a polyimide.

REPLACEMENT SHEET
01 DEC 1999

7. A semiconductor device according to claim 1, wherein said base substrate has a plurality of connection holes that reaches from said first surface to said second surface,

and wherein one end of said connection hole is electrically connected to one of said electric conductor layers, another end of said connection hole being electrically connected to one of said bump electrodes.

8. A semiconductor device according to claim 1, further comprising:

an insulation layer between said semiconductor chip and said wire where said wire is connected with said electric conductor layer, said insulation layer being arranged around said semiconductor chip.

9. A semiconductor device according to claim 1, further comprising:

a plurality of insulation layers formed on said first surface of said base substrate and at the peripheral area of said semiconductor chip, so as to cover said plurality of electric conductor layers.

10. A semiconductor device comprising:

a base substrate which is made of film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of insulation layers formed on said first surface of said base substrate and at the peripheral area of said semiconductor chip, so as to cover said plurality of electric conductor layers;

a plurality of bonding wires electrically connect between said external terminals and said electric conductor layers, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers; and

a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires;

wherein said insulation layers are separated each other in a plane view.

11. A semiconductor device according to claim 10, wherein said base substrate having square-form in a plane view, said insulation layer is divided at a corner area of said base substrate.

REPLACEMENT SHEET
01 DEC 1999

12. A semiconductor device according to claim 10, wherein said base substrate having square-form in a plane view, said insulation layer is divided into multiplicity correspond to each side of said base substrate.

13. A semiconductor device according to claim 10, wherein said base substrate is made of insulation resin of epoxy.

14. A semiconductor device according to claim 10, wherein said base substrate is made of insulation resin of a polyimide.

15. A semiconductor device according to claim 10, wherein said base substrate has a plurality of connection holes that reaches from said first surface to said second surface,

and wherein one end of said connection hole is electrically connected to one of said electric conductor layers, another end of said connection hole being electrically connected to one of said bump electrodes.

16. A semiconductor device according to claim 10, further comprising:

an insulation layer between said semiconductor chip and said wire where said wire is connected with said electric conductor layer, said insulation layer being arranged around said semiconductor chip.

17. A semiconductor device according to claim 10, further comprising:

a plurality of insulation layers formed between said electric conductor layers and said semiconductor chip in an area on which said semiconductor chip is mounted;

wherein said insulation layers are separated each other in a plane view.

18. A semiconductor device according to claim 10, wherein said insulation layers are sealed by said resin member so that part of said insulation layer and said resin member being overlapped.

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SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

ABSTRACT OF THE DISCLOSURE

Ball Grid Array type semiconductor package is disclosed. A semiconductor chip is mounted through an adhesive material on a surface of a flexible film substrate. The plural of bump electrode are arranged in array to the opposite side of said substrate and the semiconductor chip is sealed by resin.

Concretely, an insulation layer is formed to cover an electric conductor layer pattern formed on the surface of the substrate, and the semiconductor chip is mounted through an adhesive material on the insulation layer.

The above insulation layer is divided into the plural number of part that is mutually discontinuous in the area under the above semiconductor chip. By this divided insulation layer, the short circuit between above semiconductor chip and above electric conductor layer pattern is prevented and the deformation of the substrate that comprises the above flexible films is suppressed.

Figure 1

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30 JAN 2002

19. A semiconductor device comprising:

a base substrate comprised of film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of insulation layers formed between said electric conductor layers and said semiconductor chip;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers, and a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires;

wherein said insulation layers are separated from each other in a plane view in an area on which said semiconductor chip is mounted.

20. A semiconductor device according to claim 19, further comprising:

a plurality of electrode pad respectively formed on each end of said electric conductor layers and arranged in said area on which said semiconductor chip is mounted;

wherein individual ones of said insulation layers are formed on individual ones of said electrode pads so as to cover each of said electrode pads.

REPLACEMENT SHEET

30 JAN 2002

21. A semiconductor device according to claim 19, further comprising:

a plurality of electrode pads respectively formed on each end of said electric conductor layers and arranged in said area on which said semiconductor chip is mounted;

wherein each of said electrode pads is covered with one of said insulation layers.

22. A semiconductor device according to claim 19, wherein said base substrate is comprised of insulation resin of epoxy.

23. A semiconductor device according to claim 19, wherein said base substrate is comprised of insulation resin of a polyimide.

24. A semiconductor device according to claim 19, wherein said base substrate has a plurality of connection holes that reach from said first surface to said second surface, and wherein one end of each of said connection holes is electrically connected to one of said electric conductor layers, and another end of each of said connection holes is electrically connected to one of said bump electrodes.

25. A semiconductor device according to claim 19, wherein said insulation layers are arranged to prevent a short-circuit between said semiconductor chip and said electric conductor layers.

26. A ball grid array type semiconductor package comprising:

a base substrate comprised of a flexible film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electrode pads formed on said first surface of said flexible base substrate, wherein the electrode pads are completely separated from one another in a plane view;

a semiconductor chip mounted through an adhesive material

REPLACEMENT SHEET

30 JAN 2002

on said first surface of said base substrate and arranged over said plurality of electrode pads, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of insulation layers formed to respectively cover each of said electrode pads, wherein the plurality of insulation layers are also completely separated from one another in a plane view;

a plurality of bonding wires to which the plurality of electrical conductors to permit electrical contact between the plurality of electrode pads and said external terminals; and

a plurality of bump electrodes arranged on said second surface and electrically connected with said electrode pads.

27. A semiconductor device comprising:

a flexible base substrate comprised of film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers, a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires; and

means for preventing short-circuiting between the semiconductor chip and the plurality of electrical conductor layers and for preventing deformation of the flexible base substrate during manufacture of the semiconductor device,

REPLACEMENT SHEET
30 JAN 2002

wherein said means comprises a plurality of insulation layers formed between said electric conductor layers and said semiconductor chip, and wherein said plurality of insulation layers are separated from one another in a plane view in an area in which the semiconductor chip is mounted.

28. A semiconductor device comprising:

a base substrate which is comprising of film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of insulation layers formed on said first surface of said base substrate and at a peripheral area of said semiconductor chip, so as to cover said plurality of electric conductor layers;

a plurality of bonding wires electrically connected between said external terminals and said electric conductor layers, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers; and

a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires;

wherein said insulation layers are separated from each other in a plane view.

29. A semiconductor device according to claim 28 wherein said

REPLACEMENT SHEET

30 JAN 2002

base substrate has a square-form in a plane view, and said insulation layer is divided at a corner area of said base substrate.

30. A semiconductor device according to claim 28, wherein said base substrate has a square-form in a plane view, and said insulation layer is divided to correspond to each side of said base substrate.

31. A semiconductor device according to claim 28, wherein said base substrate is comprised of insulation resin of epoxy.

32. A semiconductor device according to claim 28, wherein said base substrate is comprised of insulation resin of a polyimide.

33. A semiconductor device according to claim 28, wherein said base substrate has a plurality of connection holes that reach from said first surface to said second surface,

and wherein one end of said connection hole is electrically connected to one of said electric conductor layers, and another end of each said connection hole is electrically connected to one of said bump electrodes.

34. A semiconductor device according to claim 28, further comprising:

an insulator between said semiconductor chip and said wire where said wire is connected with said electric conductor layer, and said insulator being arranged around said semiconductor chip.

35. A semiconductor device according to claim 28, further comprising:

a plurality of insulation layers formed between said electric conductor layers and said semiconductor chip in an area on which said semiconductor chip is mounted;

wherein said insulation layers are separated from each

REPLACEMENT SHEET

30 JAN 2002

other in a plane view.

36. A semiconductor device according to claim28 wherein said insulation layers are sealed by said resin member so that part of said insulation layer and said resin member are overlapped.

37. A semiconductor device comprising:

a base substrate comprised of film and having a first surface and a second that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a plurality of insulation layers formed between said electric conductor layers and said semiconductor chip;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers, and

a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires;

wherein said insulation layers are separated from each other in a plane view in an area on which said semiconductor chip is mounted, and

wherein the semiconductor device further comprises a plurality of electric conductor layers for plating formed at the peripheral area of said semiconductor chip, wherein each of said electric conductor layers for plating extends continuous with one of said electric conductor layers and reaches to a side of said base substrate; and a plurality of insulation layers formed over said first surface of said base

REPLACEMENT SHEET

30 JAN 2002

substrate and at said peripheral area of said semiconductor chip, so as to cover said plurality of electric conductor layers for plating.

38. A semiconductor device according to claim 37, wherein said insulation layer is divided into sections corresponding to each side of said base substrate.

39. A semiconductor device comprising:

a base substrate comprised of flexible film and having a first surface and a second surface that is opposed to said first surface;

a plurality of electric conductor layers formed on said first surface of said base substrate;

a semiconductor chip mounted through an adhesive material on said first surface of said base substrate and arranged over said plurality of electric conductor layers, said semiconductor chip having a plurality of semiconductor elements and a plurality of external terminals formed on its main surface;

a first insulation layer formed between said electric conductor layers and said semiconductor chip;

a plurality of bonding wires to which said external terminals and said electric conductor layers are electrically connected, respectively;

a plurality of bump electrodes arranged on said second surface and electrically connected with said electric conductor layers, and

a resin member sealing said semiconductor chip, said electric conductor layers and said bonding wires;

wherein the semiconductor device further comprises a plurality of electric conductor layers for plating formed at the peripheral area of said semiconductor chip, wherein each of said electric conductor layers for plating extends continuous with one of said electric conductor layers and reaches to a side of said base substrate; and a second insulation layer formed on said first surface of said base substrate and

REPLACEMENT SHEET
30 JAN 2002

at the outside of resin member, so as to cover said plurality of electric conductor layers for plating;

wherein said second insulation layer is separated from said first insulation layer in a plane view; and

wherein an insulation layer made of same material of said first insulation layer is not formed on the second surface of the base substrate.

REPLACEMENT SHEET
30 JAN 2002

SEMICONDUCTOR DEVICE AND ITS MANUFACTURING METHOD

ABSTRACT OF THE DISCLOSURE

Ball Grid Array type semiconductor package is disclosed. A semiconductor chip is mounted through an adhesive material on a surface of a flexible film substrate. The plural of bump electrode are arranged in array to the opposite side of said substrate and the semiconductor chip is sealed by resin.

Concretely, an insulation layer is formed to cover an electric conductor layer pattern formed on the surface of the substrate, and the semiconductor chip is mounted through an adhesive material on the insulation layer.

The above insulation layer is divided into the plural number of part that is mutually discontinuous in the area under the above semiconductor chip. By this divided insulation layer, the short circuit between above semiconductor chip and above electric conductor layer pattern is prevented and the deformation of the substrate that comprises the above flexible films is suppressed.

Figure 1