WHAT IS CLAIMED IS:

1. A memory device comprising:

a memory cell array in a first semiconductor layer and including word lines stacked in a first direction, and channel structures passing through the word lines in the first direction;

a control logic circuit in a second semiconductor layer located below the first semiconductor layer in the first direction; and

a physical unclonable function (PUF) circuit including a plurality of through electrodes passing through the first semiconductor layer and the second semiconductor layer in the first direction, and configured to

generate PUF data according to resistance values of the plurality of through electrodes, and

generate the PUF data based on a node voltage between through electrodes connected in series, from among the plurality of through electrodes.

2. The memory device of claim 1, wherein

the first semiconductor layer is divided into a cell region in which the channel structures are arranged, a word line step region, and a peripheral region;

the plurality of through electrodes include at least one of a first through electrode formed in the cell region;

a second through electrode formed in the word line step region; and

a third through electrode formed in the peripheral region.

3. The memory device of claim 2, wherein the first through electrode, the second through electrode, and the third through electrode have different resistance values.

4. The memory device of claim 1, wherein the PUF circuit includes

a PUF cell array configured to generate an output voltage by distributing a power supply voltage using the plurality of through electrodes, the PUF cell array includes a plurality of PUF cells;

a reference voltage generator circuit configured to generate a first reference voltage by distributing the power supply voltage; and

a comparison circuit configured to output a comparison result by comparing the output voltage with the first reference voltage.

5. The memory device of claim 4, wherein each of the plurality of PUF cells includes

a first resistive element including a through electrode between a power supply voltage terminal to which the power supply voltage is applied and a first node; and

a second resistive element including a through electrode between the first node and a ground voltage terminal to which a ground voltage is applied, a voltage of the first node is supplied to the comparison circuit as the node voltage.

6. The memory device of claim 4, wherein each of the plurality of PUF cells includes

a first resistive element including a plurality of through electrodes connected in series between a power supply voltage terminal to which the power supply voltage is applied and a first node, and

a second resistive element including a plurality of through electrodes connected in series between the first node and a ground voltage terminal to which a ground voltage is applied, and wherein a voltage of the first node is supplied to the comparison circuit as the node voltage.

7. The memory device of claim 4, wherein the reference voltage generator circuit includes

a first resistive element between a power supply voltage terminal to which the power supply voltage is applied and a first node; and

a second resistive element between the first node and a ground voltage terminal to which a ground voltage is applied, and

wherein a voltage of the first node is supplied to the comparison circuit as the first reference voltage.

8. The memory device of claim 7, wherein each of the first resistive element and the second resistive element includes at least one through electrode.

9. The memory device of claim 7 or claim 8, wherein the reference voltage generator circuit is configured to generate a second reference voltage greater than the first reference voltage, and a third reference voltage less than the first reference voltage, and

the comparison circuit is configured to further compare an output voltage of each of the plurality of PUF cells with at least one of the second reference voltage and the third reference voltage.

10. The memory device of claim 9, wherein the PUF circuit further includes a combinational logic configured to generate validity data representing validity of each of the plurality of PUF cells based on a result of a comparison between the output voltage of each of the plurality of PUF cells and at least one of the second reference voltage and the third reference voltage.

11. The memory device of claim 1, wherein the plurality of through electrodes are arranged in a peripheral region of the first semiconductor layer, and include first through electrodes passing through an upper insulating layer in the first direction.

12. A memory device comprising:

a memory cell region including word lines stacked in a first direction, channel structures passing through the word lines in the first direction, and a first metal pad;

a peripheral circuit region including a second metal pad and connected to the memory cell region in the first direction by the first metal pad and the second metal pad; and

a physical unclonable function (PUF) circuit including a plurality of through electrodes passing through the memory cell region in the first direction, and configured to

generate PUF data according to resistance values of the plurality of through electrodes, and

generate the PUF data based on a node voltage between through electrodes connected in series, from among the plurality of through electrodes.

13. The memory device of claim 12, wherein the memory cell region is divided into a cell region in which the channel structures are arranged, a word line step region, and a peripheral region, and

wherein the plurality of through electrodes include

at least one of a first through electrode formed in the cell region;

a second through electrode formed in the word line step region; and

a third through electrode formed in the peripheral region.

14. The memory device of claim 12, wherein the PUF circuit includes

a PUF cell array configured to generate an output voltage by distributing a power supply voltage using the plurality of through electrodes;

a reference voltage generator circuit configured to generate a first reference voltage by distributing the power supply voltage; and

a comparison circuit configured to output a comparison result by comparing the output voltage with the first reference voltage.

15. The memory device of claim 14, wherein the PUF cell array includes a plurality of PUF cells, and each of the plurality of PUF cells includes

a first resistive element including at least one through electrode between a power supply voltage terminal to which the power supply voltage is applied and a first node; and

a second resistive element including at least one through electrode between the first node and a ground voltage terminal to which a ground voltage is applied, and

wherein a voltage of the first node is supplied to the comparison circuit as the node voltage.

16. The memory device of claim 14, wherein the reference voltage generator circuit includes a first resistive element between a power supply voltage terminal to which the power supply voltage is applied and a first node; and

a second resistive element between the first node and a ground voltage terminal to which a ground voltage is applied, and

wherein a voltage of the first node is supplied to the comparison circuit as the first reference voltage.

17. The memory device of any one of claims 12 to 16, wherein

the memory cell region is formed in a first wafer, and

the peripheral circuit region is formed in a second wafer.

18. The memory device of any one of claims 12 to 17, wherein the first metal pad and the second metal pad are connected to each other in a bonded manner.

19. A memory system comprising:

a memory device; and

a memory controller configured to transmit a physical unclonable function (PUF) data request command to the memory device in response to an authentication request received from a host, and generate an authentication key based on PUF data received from the memory device,

wherein the memory device includes

a memory cell region including word lines stacked in a first direction, channel structures passing through the word lines in the first direction, and a first metal pad;

a peripheral circuit region including a second metal pad and connected to the memory cell region in the first direction by the first metal pad and the second metal pad; and

a PUF circuit including a plurality of through electrodes passing through the memory cell region in the first direction, and configured to

generate PUF data according to resistance values of the plurality of through electrodes, and

generate the PUF data based on a node voltage between through electrodes connected in series, among the plurality of through electrodes.

20. The memory system of claim 19, wherein the memory cell region is divided into a cell region in which the channel structures are arranged, a word line step region, and a peripheral region, and

wherein the plurality of through electrodes includes at least one of

a first through electrode formed in the cell region;

a second through electrode formed in the word line step region; and

a third through electrode formed in the peripheral region.