FIG. 1

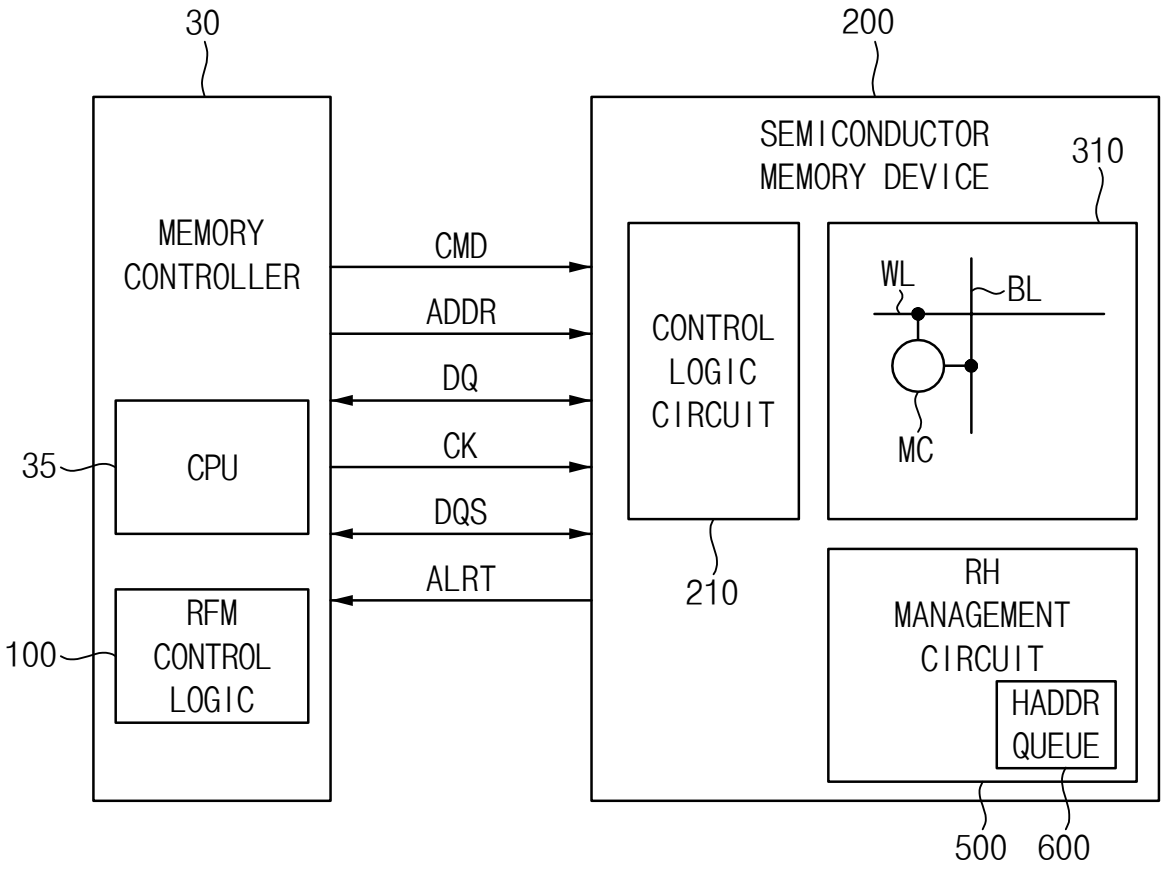

20
30
200
MEMORY CONTROLLER
SEMICONDUCTOR MEMORY DEVICE
310
CMD
ADDR
DQ
CK
DQS
ALRT
CONTROL LOGIC CIRCUIT
WL
BL
MC
35
CPU
RFM CONTROL LOGIC
100
210
RH MANAGEMENT CIRCUIT
HADDR QUEUE
500
600

FIG. 2

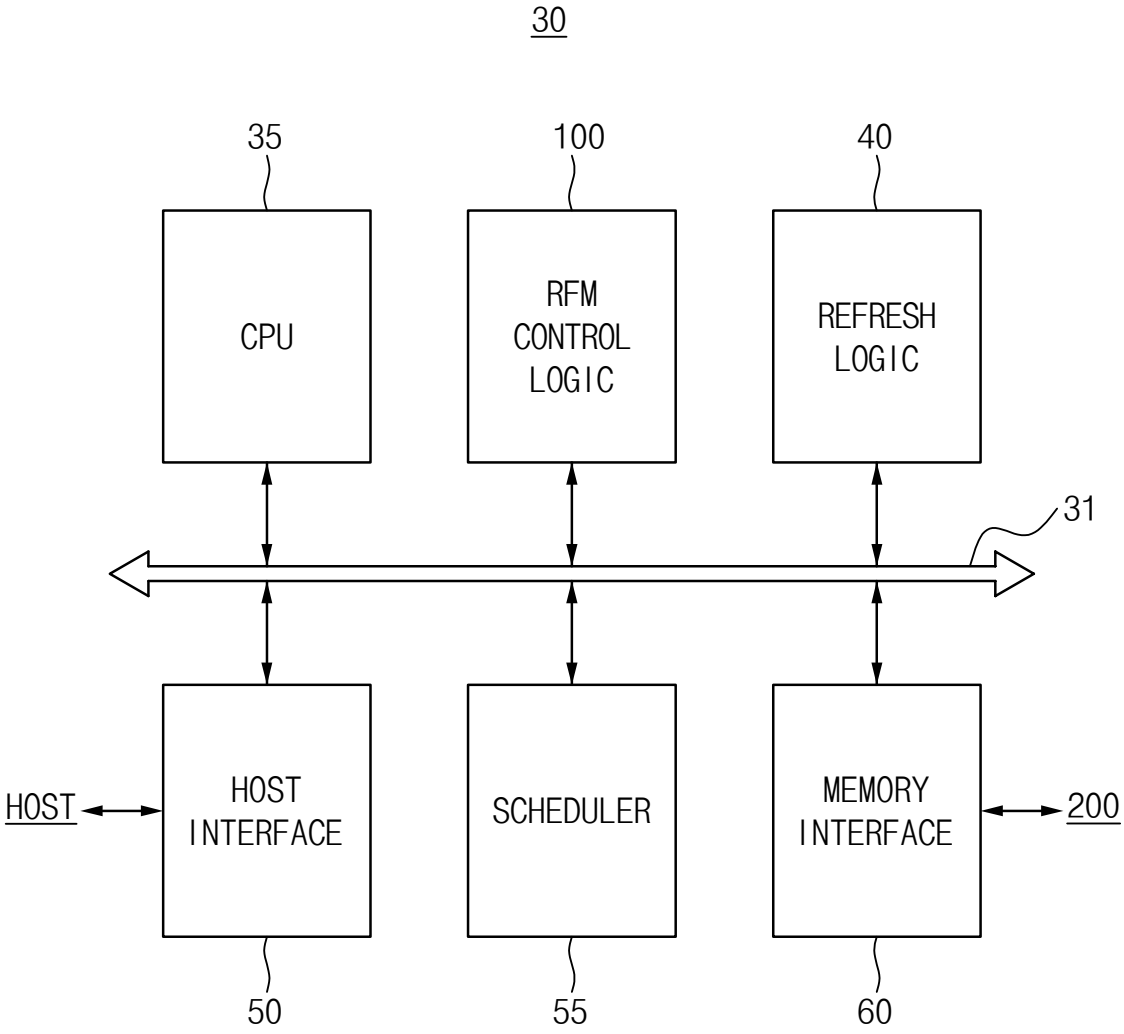

30
35
100
40
CPU
RFM CONTROL LOGIC
REFRESH LOGIC
31
HOST
HOST INTERFACE
SCHEDULER
MEMORY INTERFACE
200
50
55
60

FIG. 3

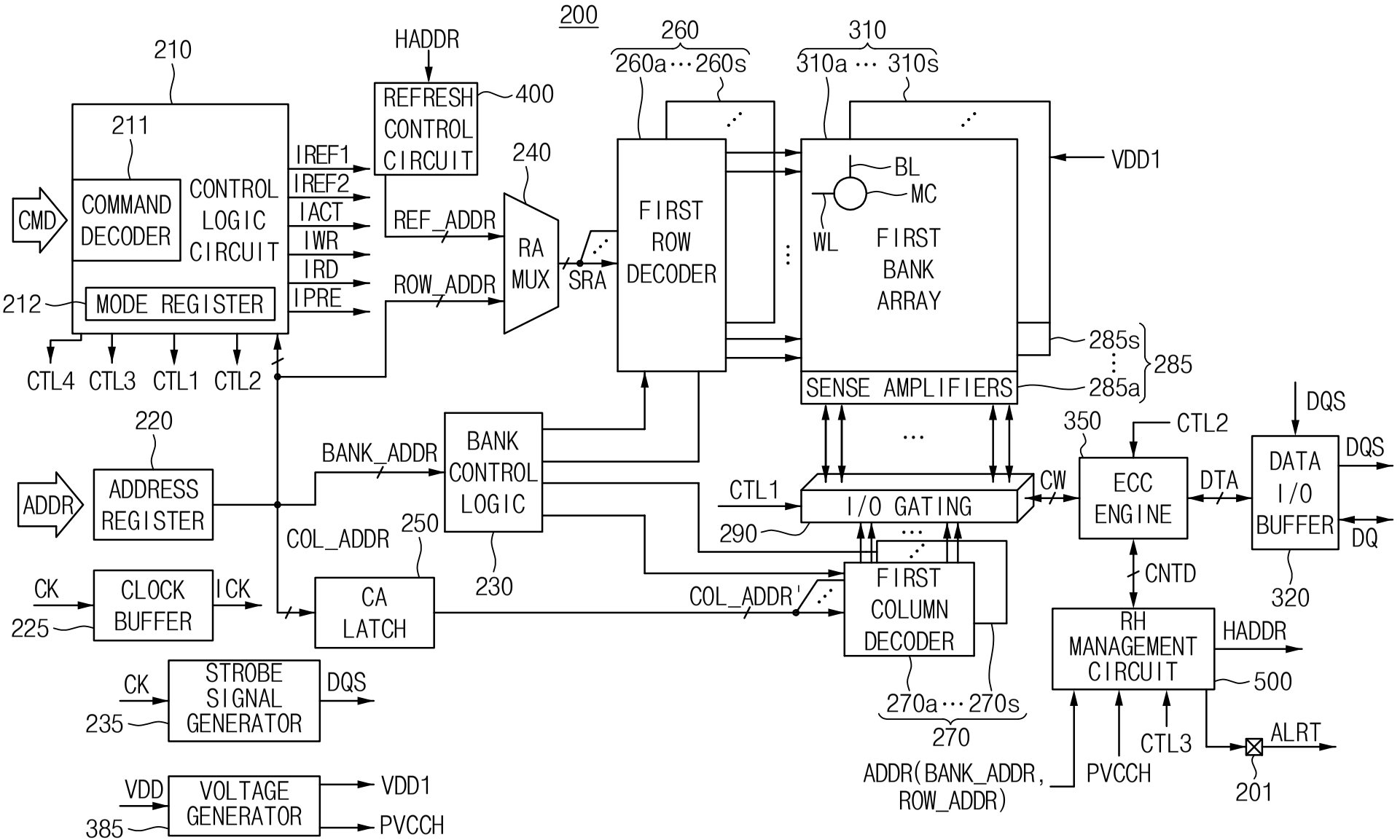

200
210
211
CONTROL LOGIC CIRCUIT
COMMAND DECODER
CMD
MODE REGISTER
212
CTL4 CTL3 CTL1 CTL2
IREF1
IREF2
IACT
IWR
IRD
IPRE
HADDR
REFRESH CONTROL CIRCUIT
400
REF_ADDR
ROW_ADDR
240
RA MUX
SRA
260
260a ··· 260s
FIRST ROW DECODER
310
310a ··· 310s
BL
MC
WL
FIRST BANK ARRAY
VDD1
285s
285
285a
SENSE AMPLIFIERS
220
ADDRESS REGISTER
ADDR
BANK_ADDR
BANK CONTROL LOGIC
230
COL_ADDR
250
CA LATCH
CK
CLOCK BUFFER
ICK
225
CK
STROBE SIGNAL GENERATOR
DQS
235
VDD
VOLTAGE GENERATOR
VDD1
PVCCH
385
CTL1
I/O GATING
290
CW
350
CTL2
ECC ENGINE
DTA
DATA I/O BUFFER
DQS
DQ
320
CNTD
COL_ADDR'
FIRST COLUMN DECODER
270a ··· 270s
270
RH MANAGEMENT CIRCUIT
HADDR
500
ALRT
201
CTL3
PVCCH
ADDR(BANK_ADDR, ROW_ADDR)

FIG. 4

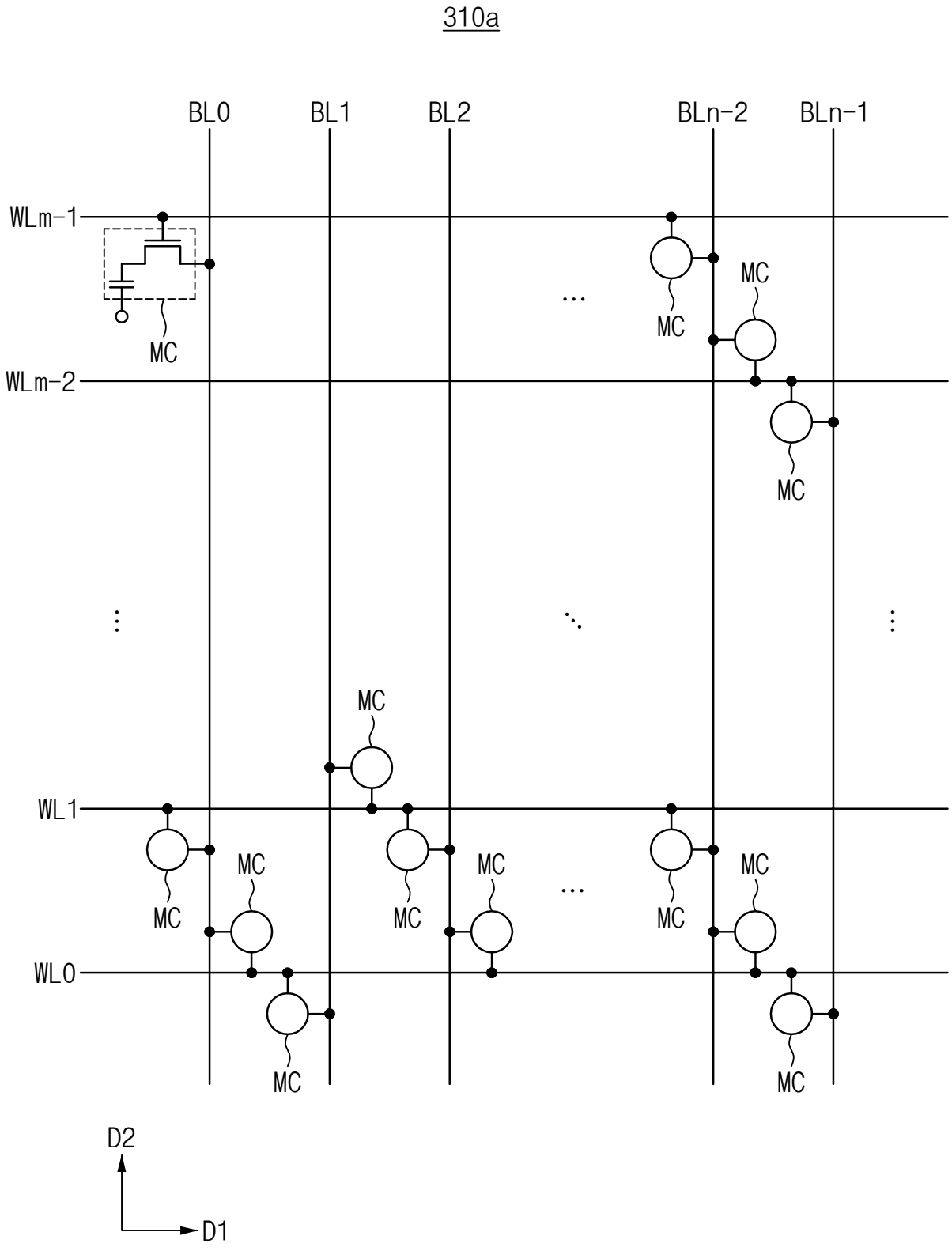


FIG. 5

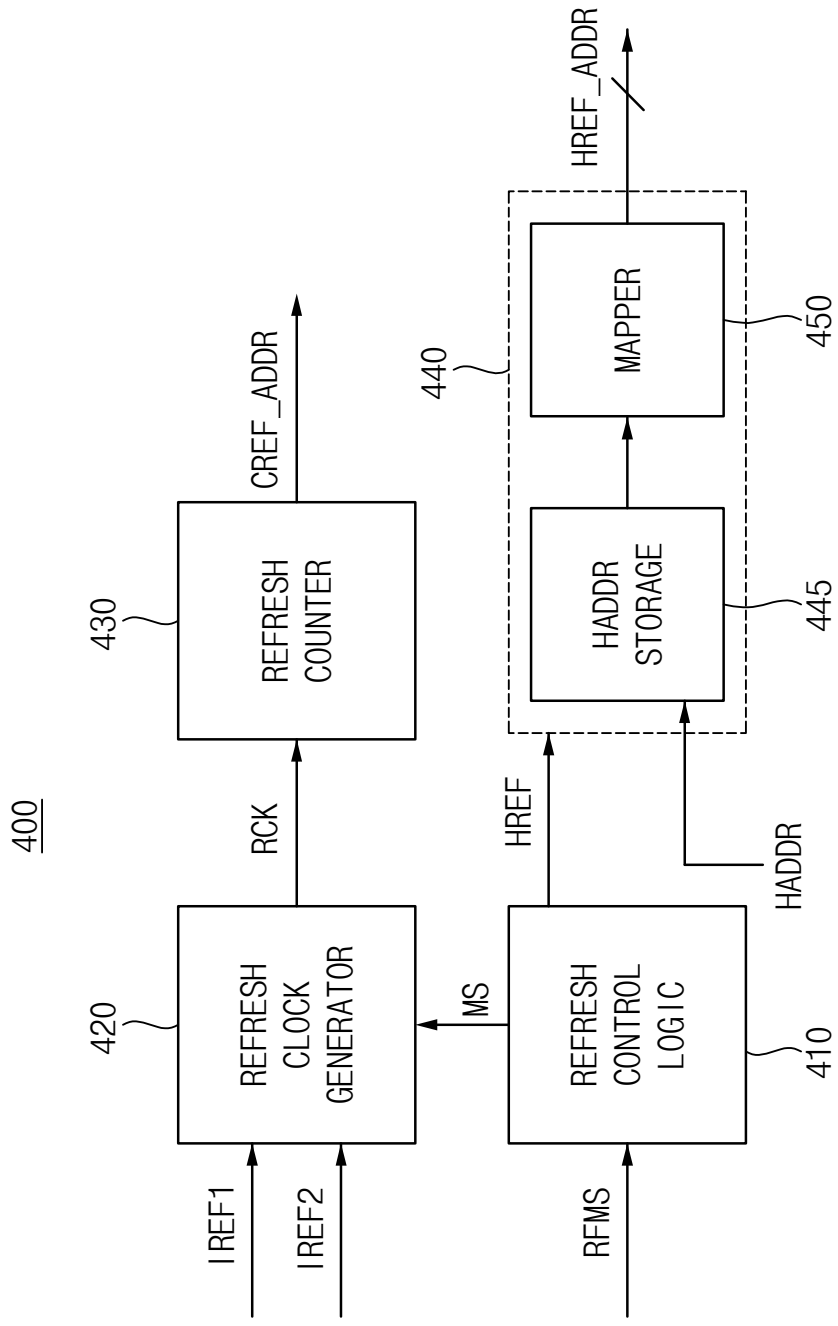

400
IREF1
IREF2
RFMS
420
REFRESH CLOCK GENERATOR
RCK
430
REFRESH COUNTER
CREF_ADDR
MS
410
REFRESH CONTROL LOGIC
HREF
440
HADDR STORAGE
445
HADDR
MAPPER
450
HREF_ADDR

FIG. 6

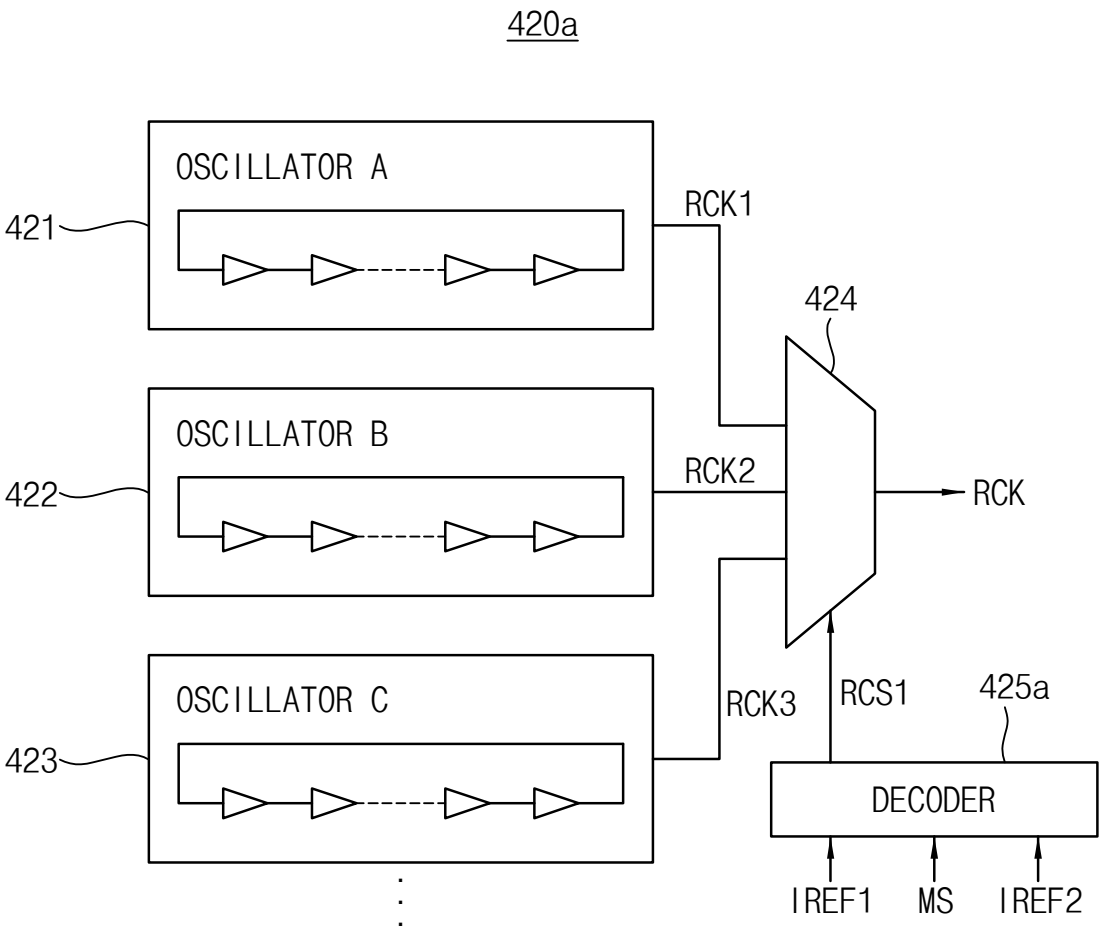

420a
OSCILLATOR A
421
RCK1
424
OSCILLATOR B
422
RCK2
RCK
OSCILLATOR C
423
RCK3
RCS1
425a
DECODER
IREF1
MS
IREF2

FIG. 7

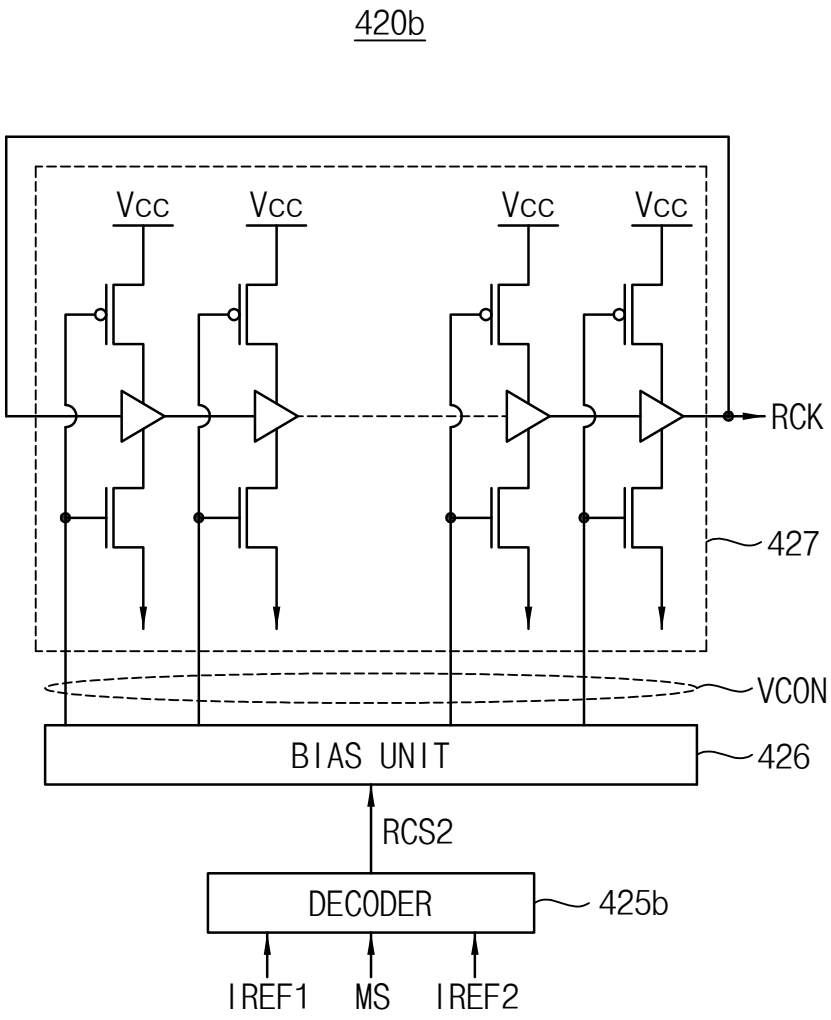

420b
Vcc
Vcc
Vcc
Vcc
RCK
427
VCON
BIAS UNIT
426
RCS2
DECODER
425b
IREF1
MS
IREF2

FIG. 8

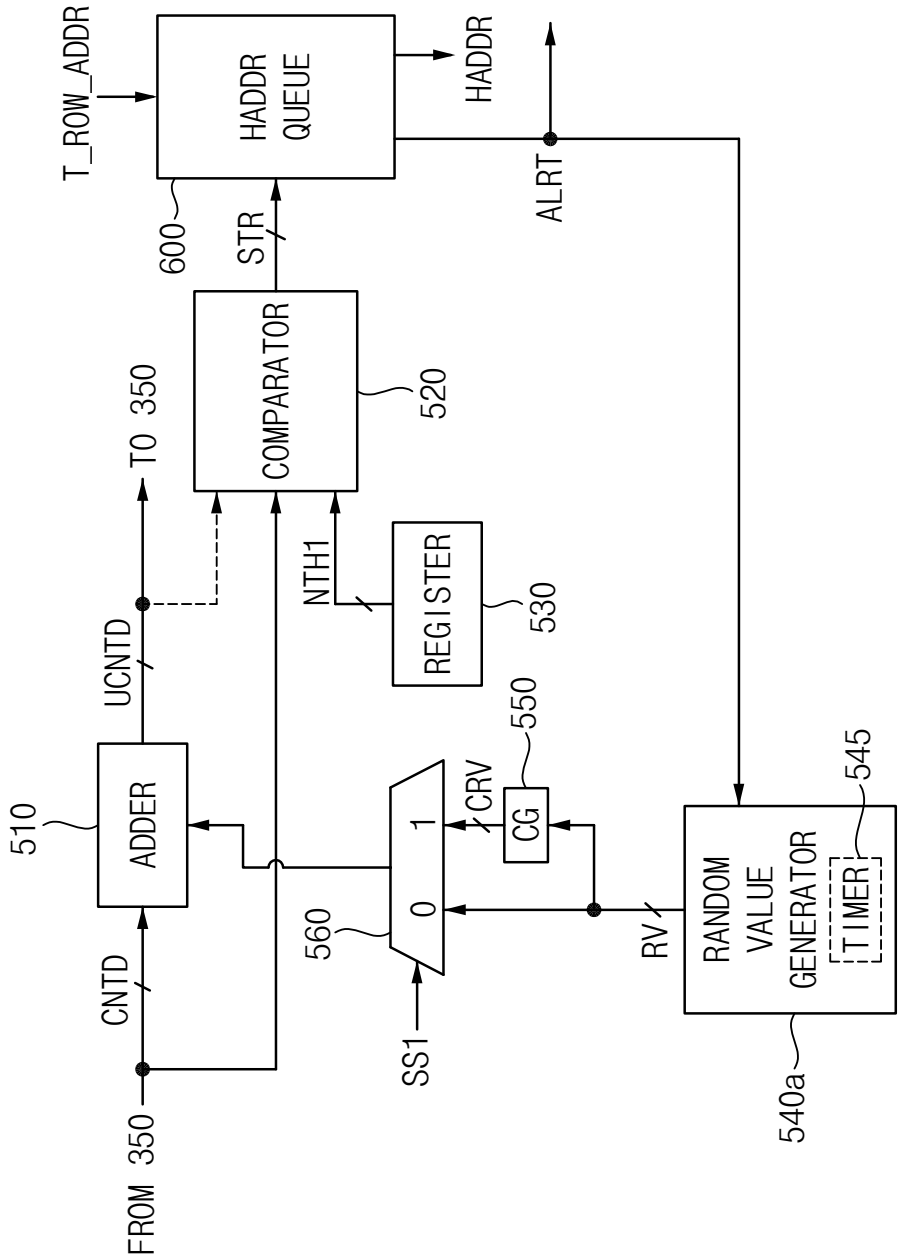

500a
T_ROW_ADDR
HADDR QUEUE
HADDR
600
STR
ALRT
COMPARATOR
520
TO 350
NTH1
REGISTER
530
UCNTD
510
ADDER
CRV
550
CG
560
1
0
SS1
RV
RANDOM VALUE GENERATOR
TIMER
545
540a
CNTD
FROM 350

FIG. 9

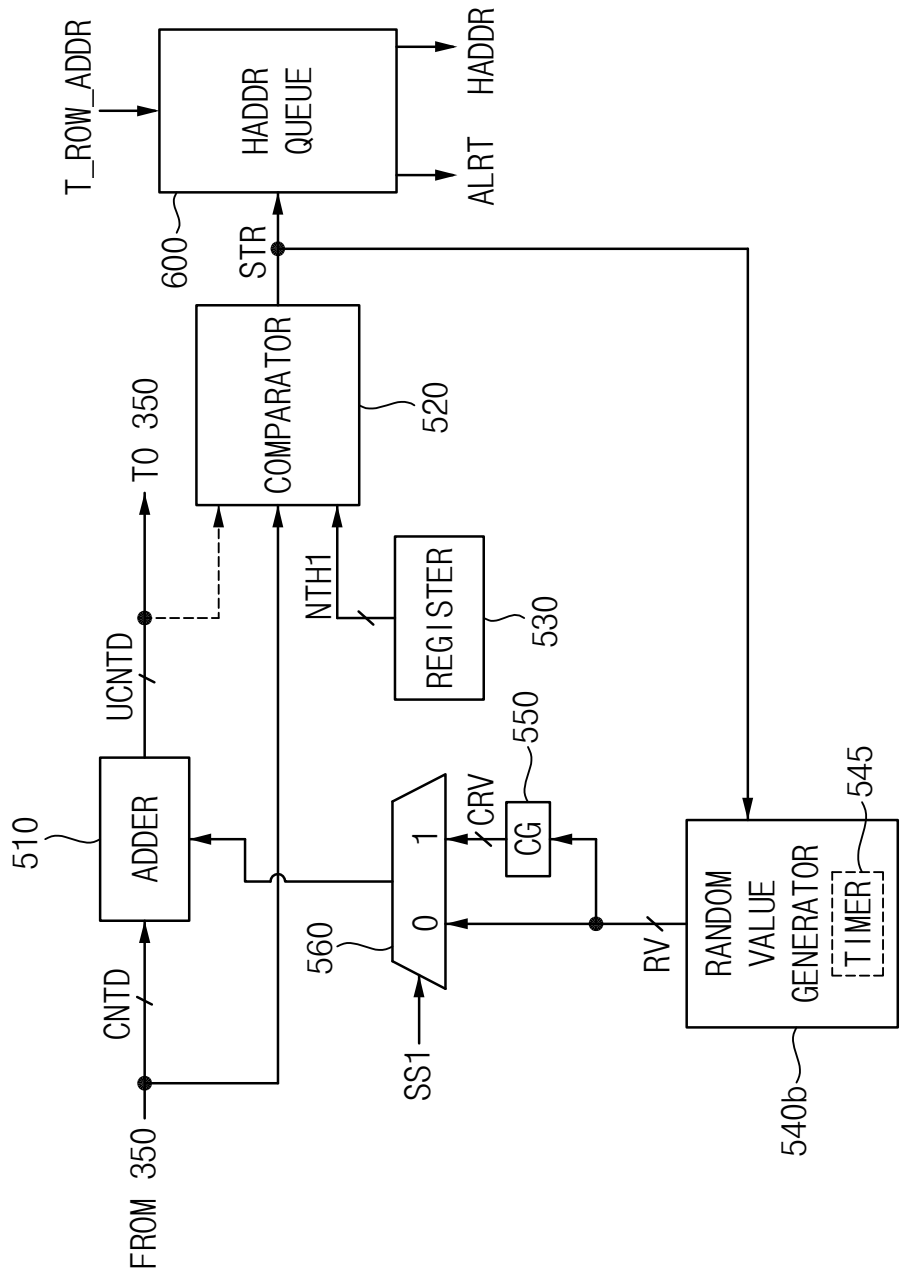

500b
T_ROW_ADDR
HADDR QUEUE
ALRT HADDR
600
STR
COMPARATOR
520
TO 350
NTH1
REGISTER
530
UCNTD
550
CRV
CG
510
ADDER
1
0
560
SS1
RV
RANDOM VALUE GENERATOR
TIMER
545
540b
CNTD
FROM 350

FIG. 10

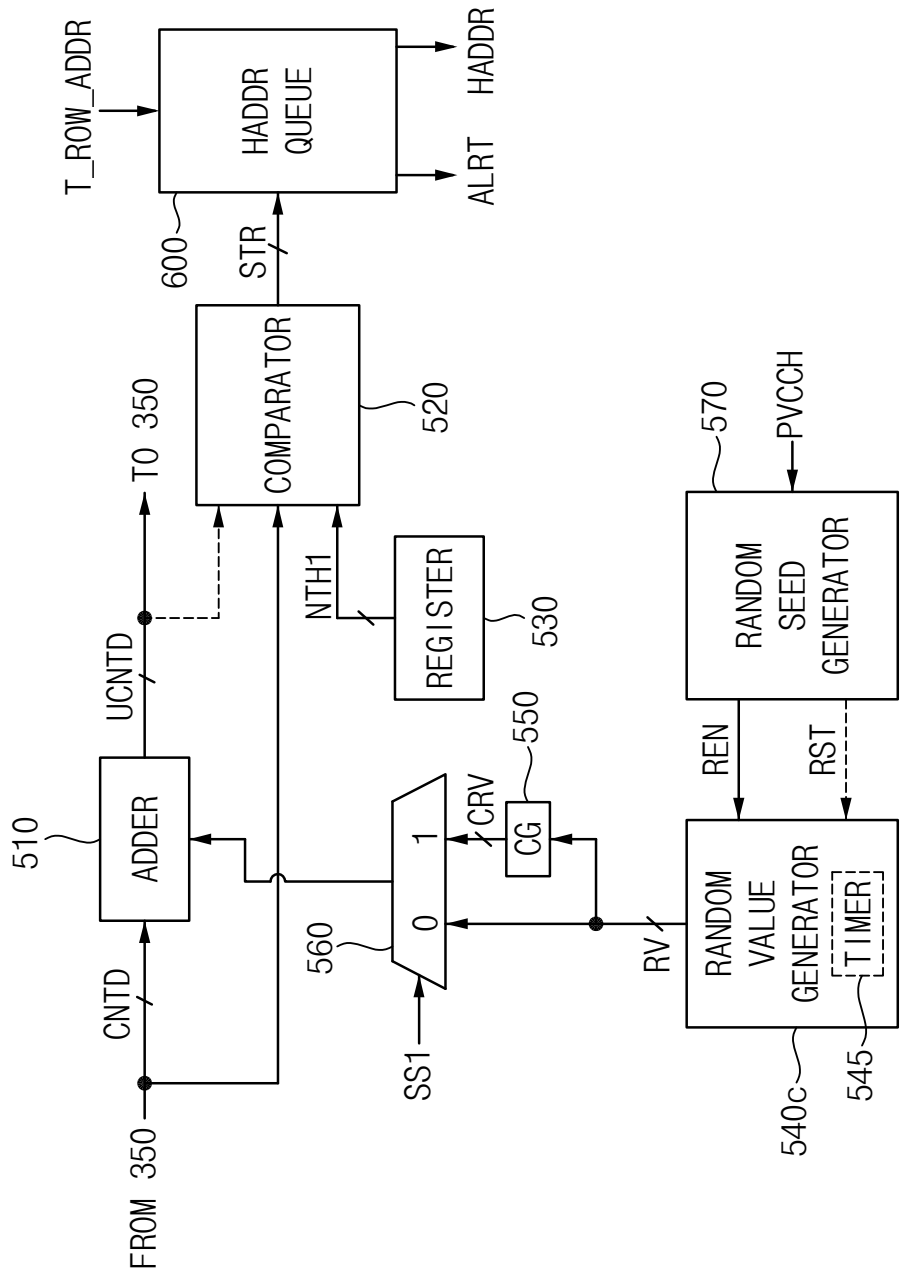

500c
T_ROW_ADDR
HADDR QUEUE
ALRT
HADDR
600
STR
COMPARATOR
520
TO 350
UCNTD
NTH1
REGISTER
530
570
PVCCH
RANDOM SEED GENERATOR
510
ADDER
CRV
550
CG
REN
RST
560
0
1
SS1
RV
RANDOM VALUE GENERATOR
TIMER
CNTD
FROM 350
540c
545

FIG. 11

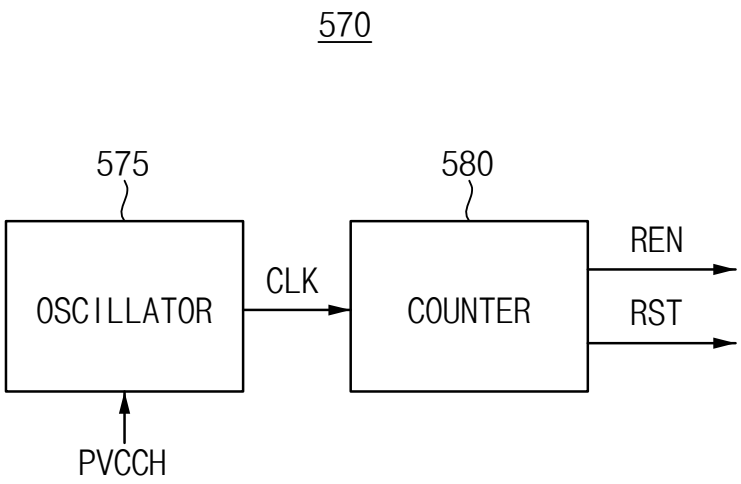


FIG. 12

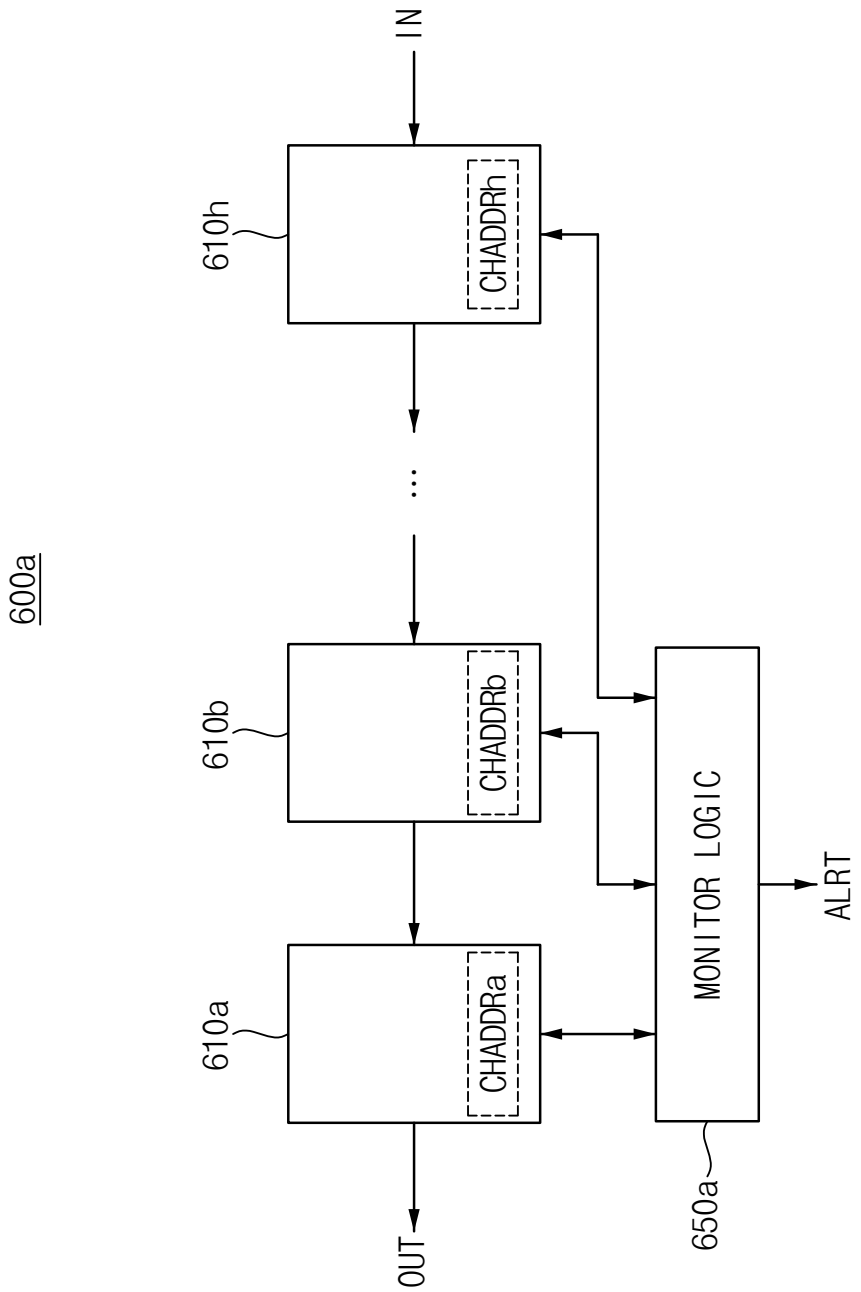

600a
IN
610h
CHADDRh
610b
CHADDRb
610a
CHADDRa
MONITOR LOGIC
ALRT
OUT
650a

FIG. 13

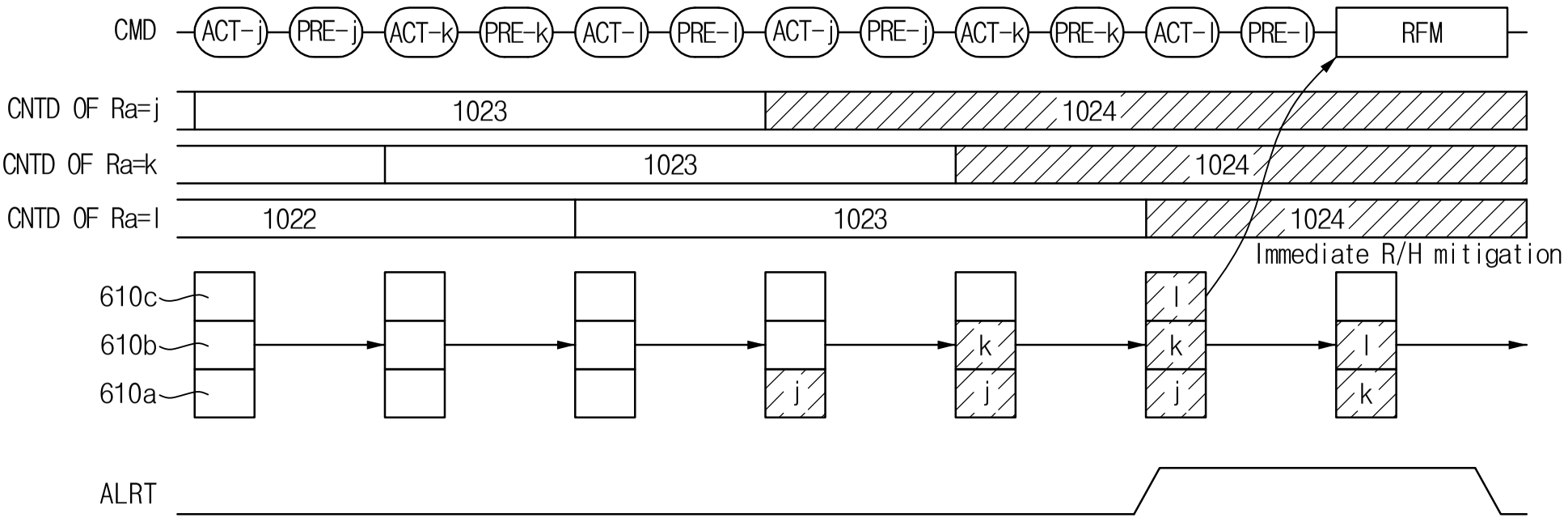

CMD
ACT-j
PRE-j
ACT-k
PRE-k
ACT-l
PRE-l
ACT-j
PRE-j
ACT-k
PRE-k
ACT-l
PRE-l
RFM
CNTD OF Ra=j
1023
1024
CNTD OF Ra=k
1023
1024
CNTD OF Ra=l
1022
1023
1024
Immediate R/H mitigation
610c
610b
610a
j
k
j
l
k
j
l
k
ALRT

FIG. 14

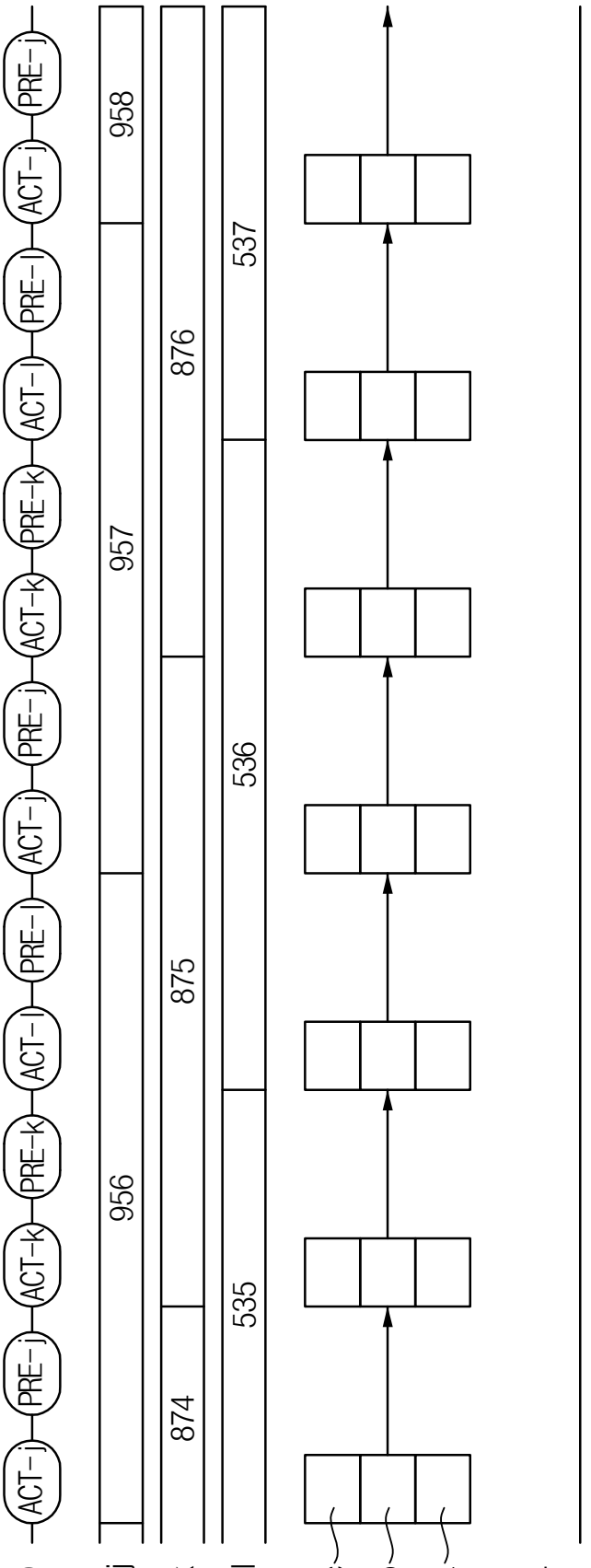

CMD
ACT-j
PRE-j
ACT-k
PRE-k
ACT-l
PRE-l
ACT-j
PRE-j
ACT-k
PRE-k
ACT-l
PRE-l
ACT-j
PRE-j
CNTD OF Ra=j
956
957
958
CNTD OF Ra=k
874
875
876
CNTD OF Ra=l
535
536
537
610c
610b
610a
ALRT

FIG. 15

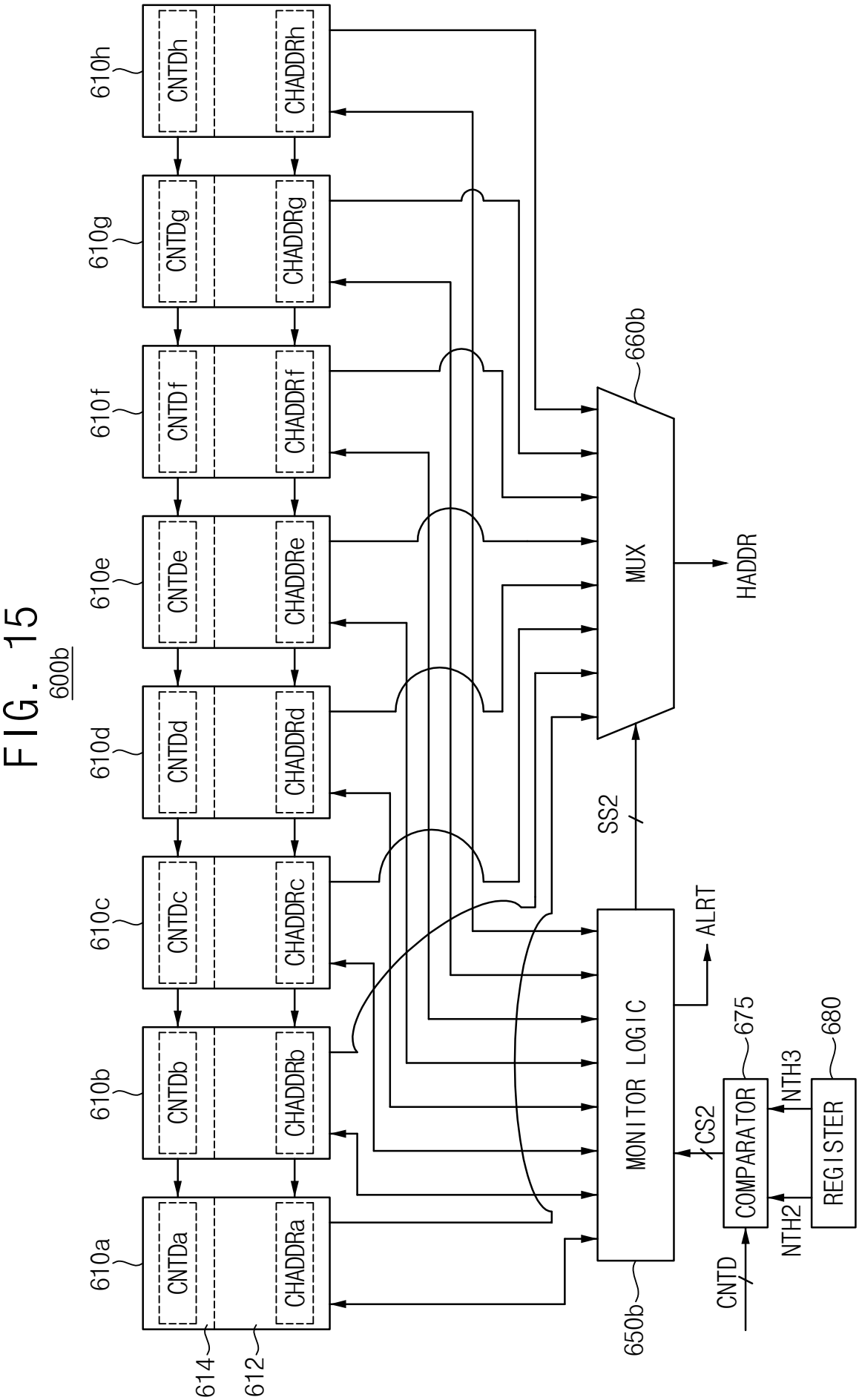

600b
610h
CNTDh
CHADDRh
610g
CNTDg
CHADDRg
610f
CNTDf
CHADDRf
610e
CNTDe
CHADDRe
610d
CNTDd
CHADDRd
610c
CNTDc
CHADDRc
610b
CNTDb
CHADDRb
610a
CNTDa
CHADDRa
614
612
660b
MUX
HADDR
SS2
650b
MONITOR LOGIC
ALRT
CS2
675
COMPARATOR
NTH3
680
REGISTER
NTH2
CNTD

FIG. 16

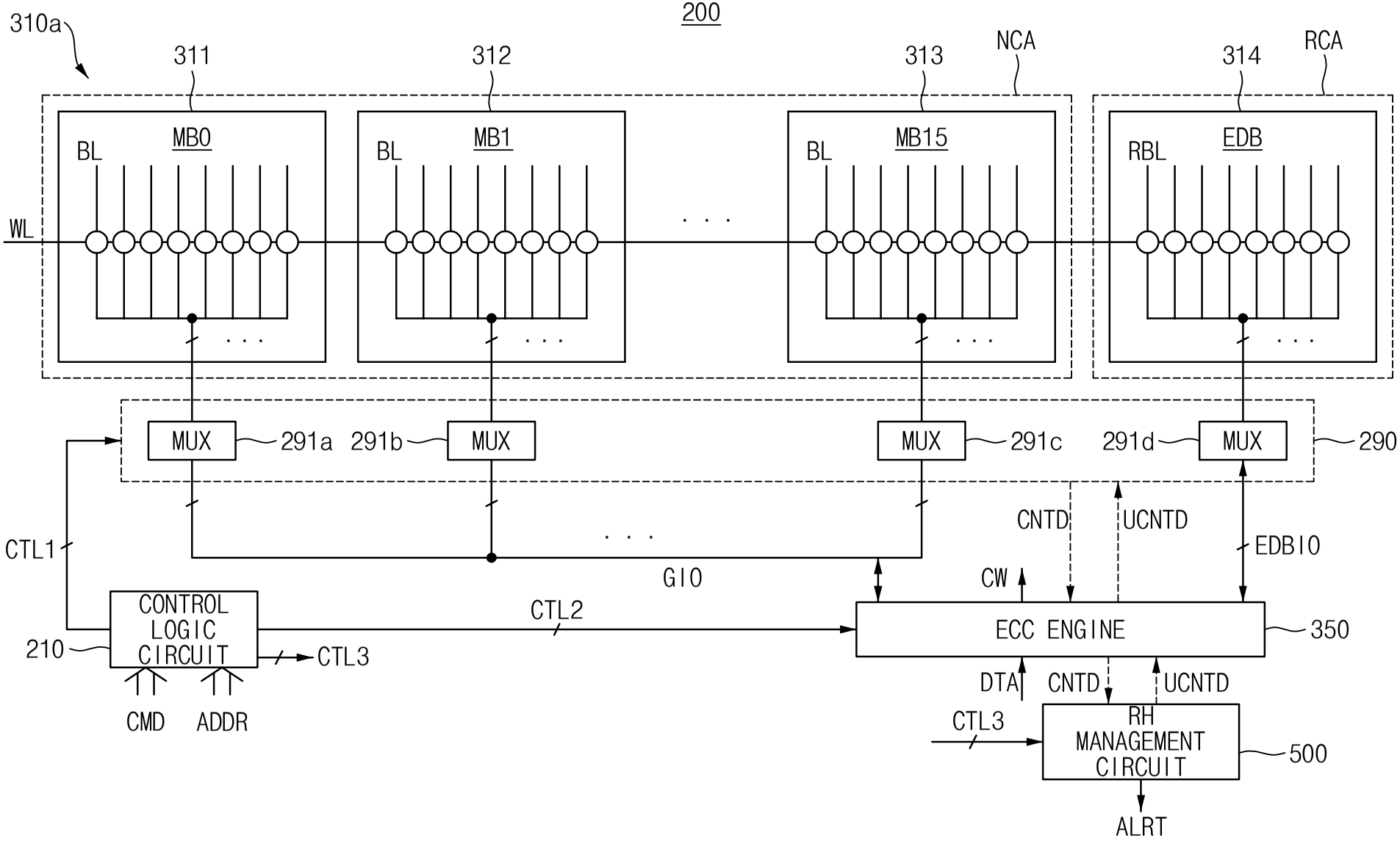

200
310a
311
312
313
NCA
314
RCA
MB0
MB1
MB15
EDB
BL
RBL
WL
MUX
291a
291b
291c
291d
290
CNTD
UCNTD
EDBIO
GIO
CW
CTL1
CONTROL LOGIC CIRCUIT
210
CTL2
CTL3
ECC ENGINE
350
DTA
CMD
ADDR
RH MANAGEMENT CIRCUIT
500
ALRT

FIG. 17

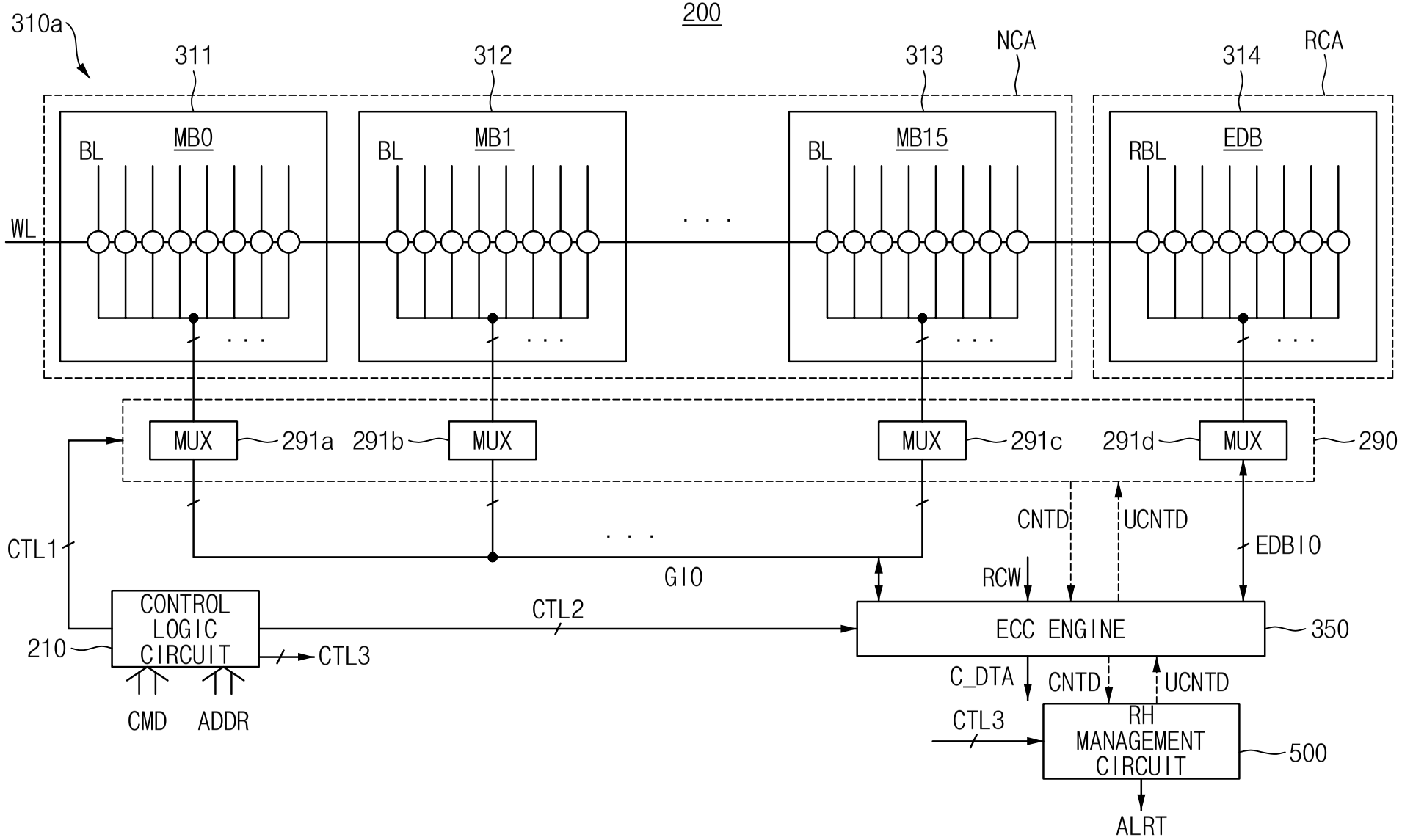

200
310a
311
312
313
NCA
314
RCA
MB0
MB1
MB15
EDB
BL
RBL
WL
MUX
291a
291b
291c
291d
290
CTL1
GIO
CNTD
UCNTD
EDBIO
RCW
CONTROL LOGIC CIRCUIT
210
CTL2
CTL3
ECC ENGINE
350
C_DTA
RH MANAGEMENT CIRCUIT
500
CMD
ADDR
ALRT

FIG. 18

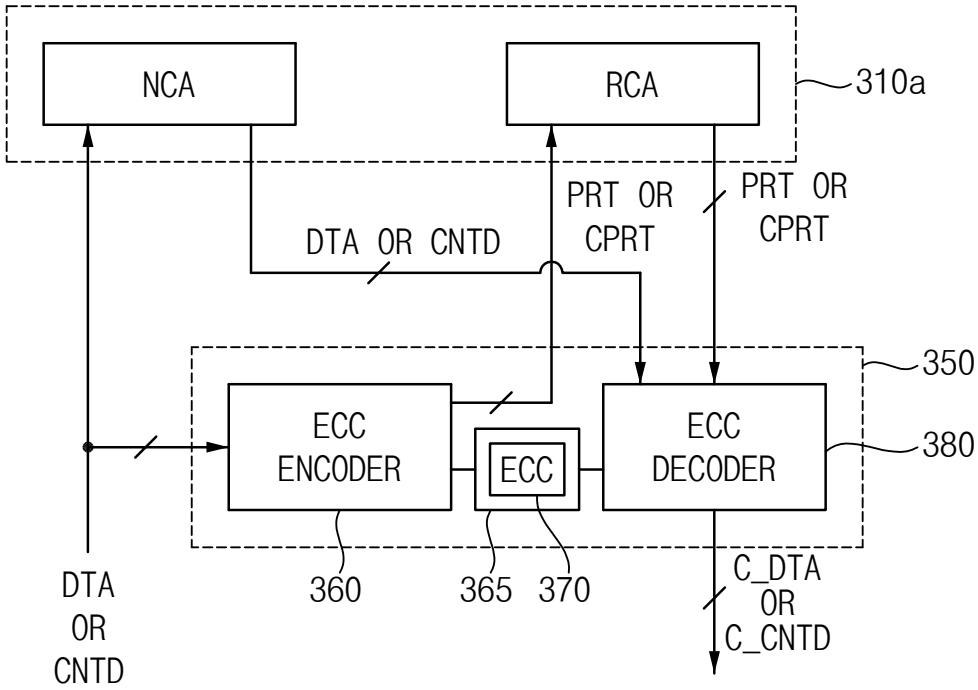

NCA
RCA
310a
PRT OR CPRT
PRT OR CPRT
DTA OR CNTD
350
ECC ENCODER
ECC
ECC DECODER
380
DTA OR CNTD
360
365
370
C_DTA OR C_CNTD

FIG. 19

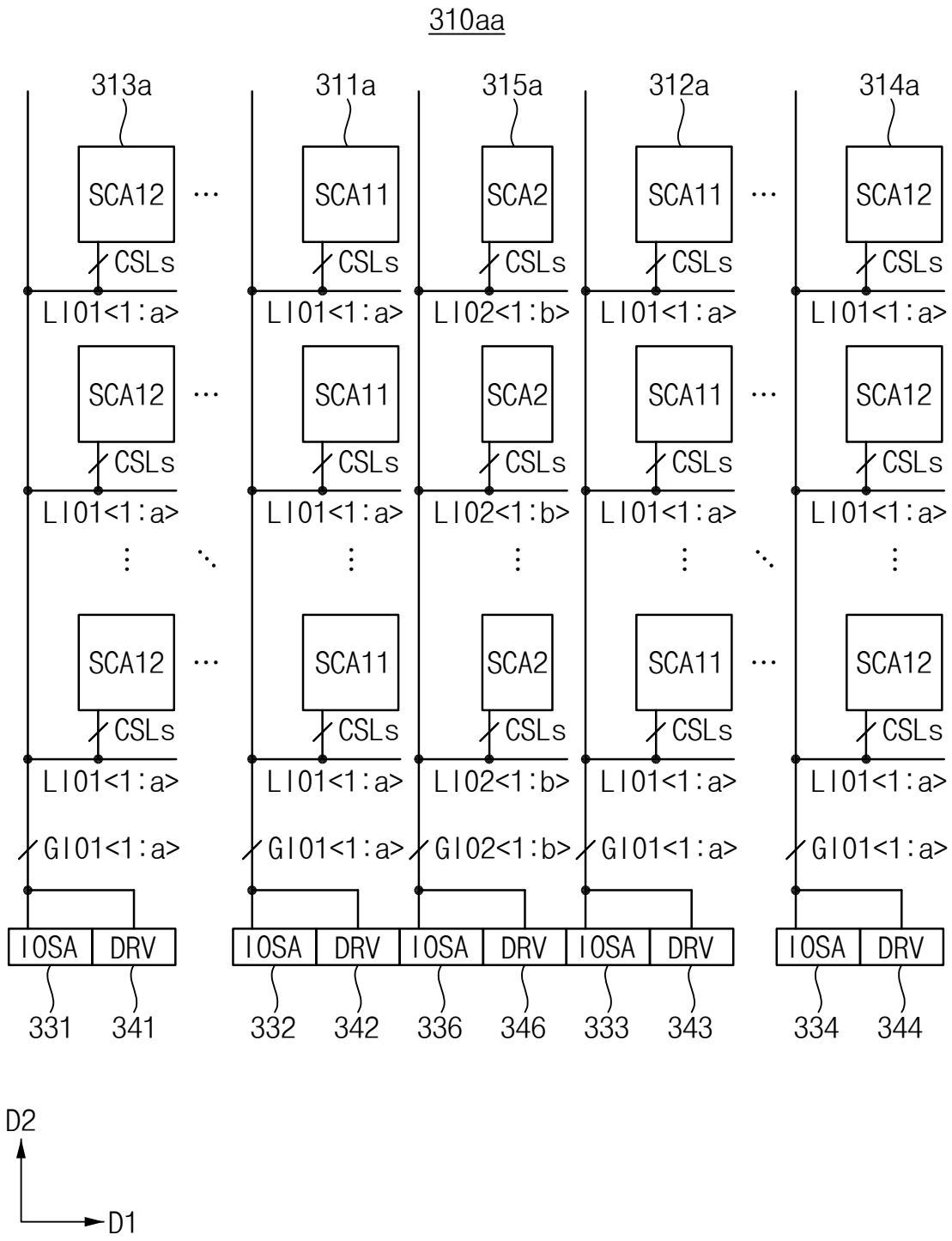

310aa
313a
311a
315a
312a
314a
SCA12
SCA11
SCA2
CSLs
LIO1<1:a>
LIO2<1:b>
GIO1<1:a>
GIO2<1:b>
IOSA
DRV
331
341
332
342
336
346
333
343
334
344
D2
D1

FIG. 20

CMD	CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13
ACT	L	L	L	R0	R1	R2	R3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2
	H	R4	R5	R6	R7	R8	R9	R10	R11	R12	R13	R14	R15	R16	CID3/ R17
WR	L	H	L	H	H	L	BLT	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2
	H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	H	L	V	CID3
RD	L	H	L	H	H	H	BLT	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2
	H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	H	V	V	CID3

FIG. 21

CMD	CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13
WRA	L	H	L	H	H	L	BLT	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2
	H	V	C3	C4	C5	C6	C7	C8	C9	C10	V	AP	L	V	CID3
RDA	L	H	L	H	H	H	BLT	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2
	H	C2	C3	C4	C5	C6	C7	C8	C9	C10	V	AP	V	V	CID3

FIG. 22

CMD	CS_n	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11	CA12	CA13
PREab	L	H	H	L	H	L	CID3	V	V	V	V	L	CID0	CID1	CID2
PREsb	L	H	H	L	H	L	CID3	BA0	BA1	V	V	H	CID0	CID1	CID2
PREpb	L	H	H	L	H	H	CID3	BA0	BA1	BG0	BG1	BG2	CID0	CID1	CID2

FIG. 23

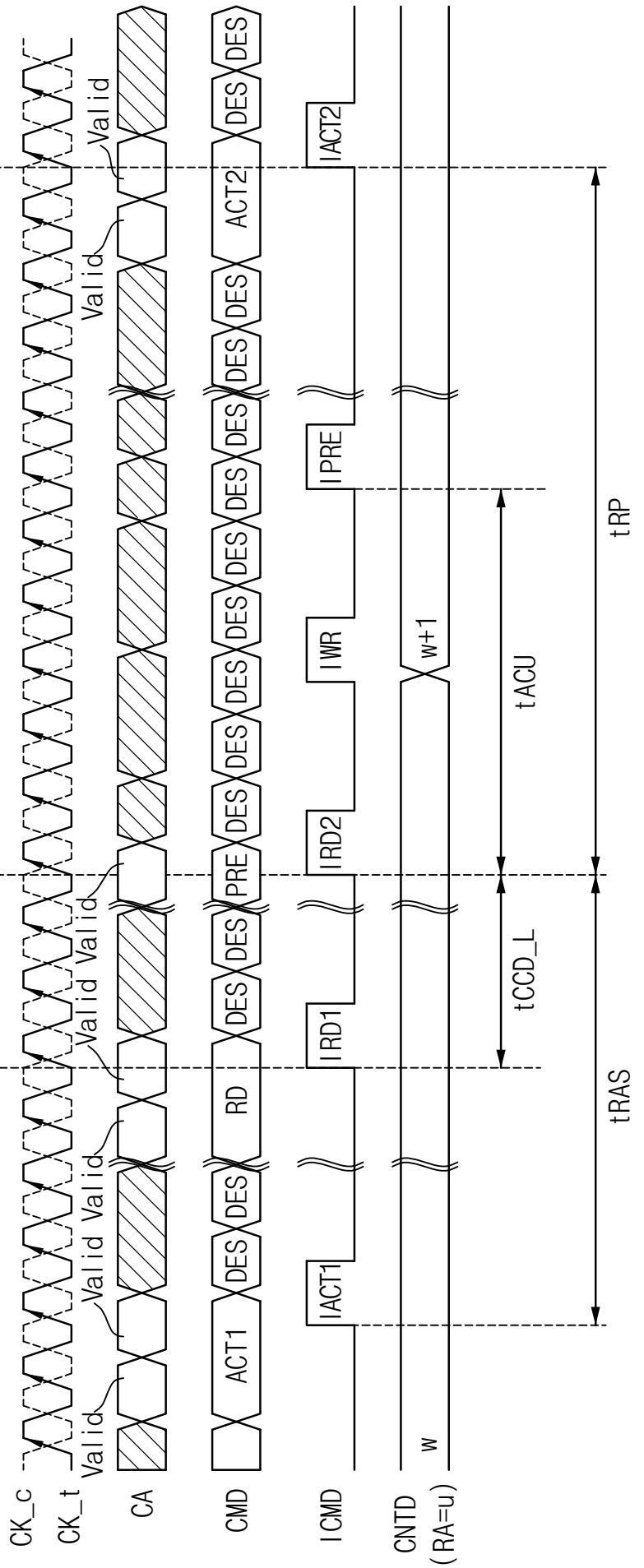

CK_c
CK_t
CA
CMD
ICMD
CNTD
(RA=u)
Valid
ACT1
DES
IACT1
RD
IRD1
PRE
IRD2
IWR
IPRE
ACT2
IACT2
w
w+1
tCCD_L
tACU
tRP
tRAS

FIG. 24

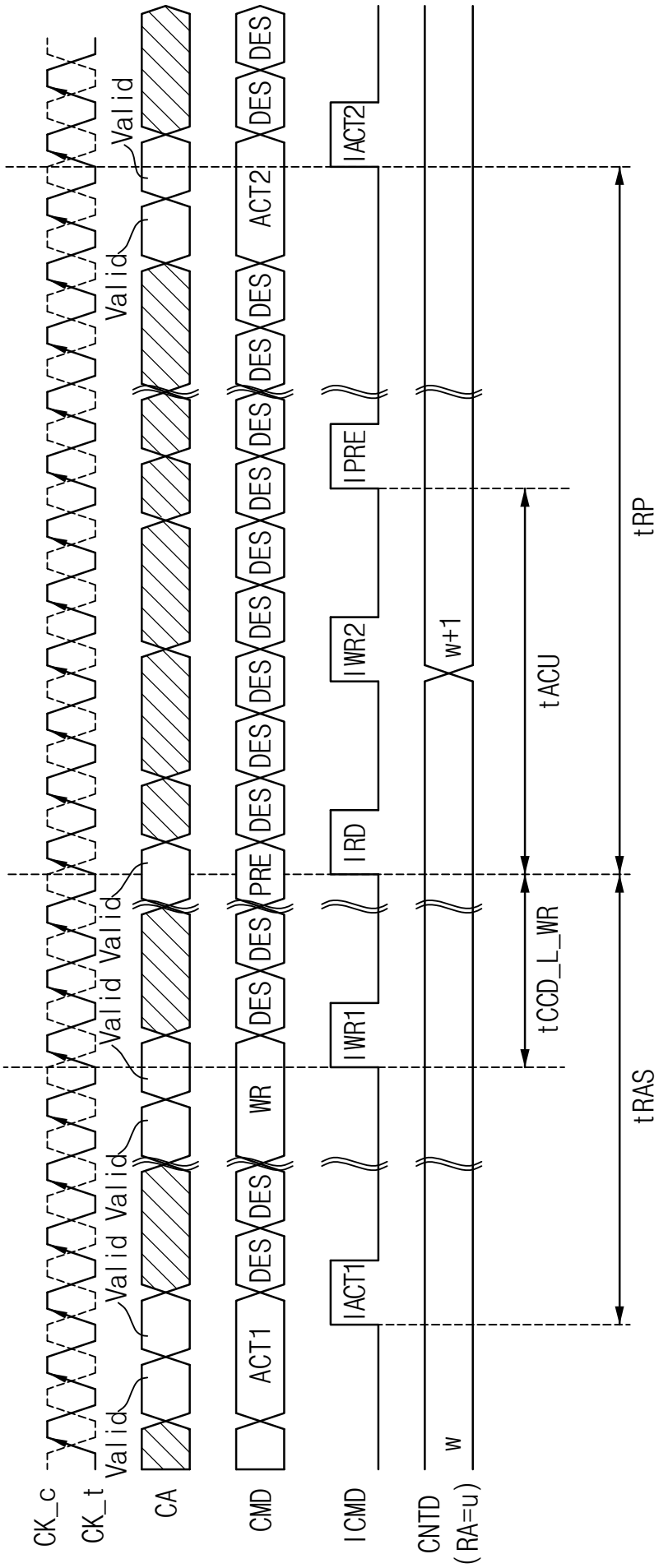

CK_c
CK_t
CA
CMD
ICMD
CNTD (RA=u)
Valid
ACT1
DES
WR
PRE
ACT2
IACT1
IWR1
IRD
IWR2
IPRE
IACT2
w
w+1
tCCD_L_WR
tACU
tRAS
tRP

FIG. 25

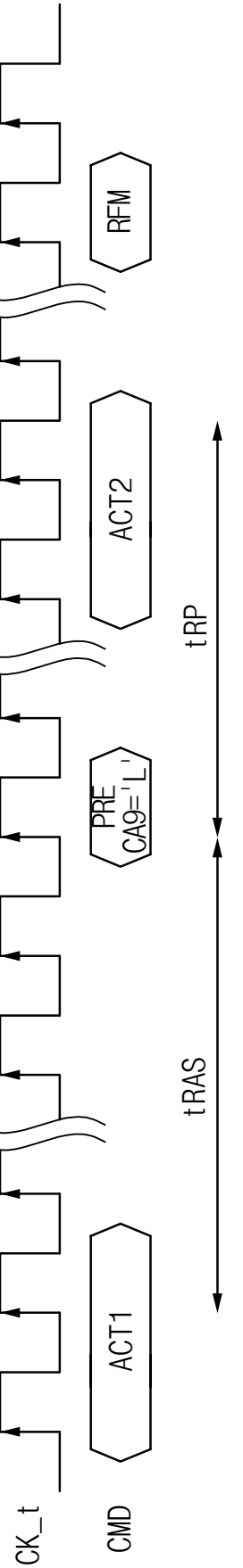


FIG. 26

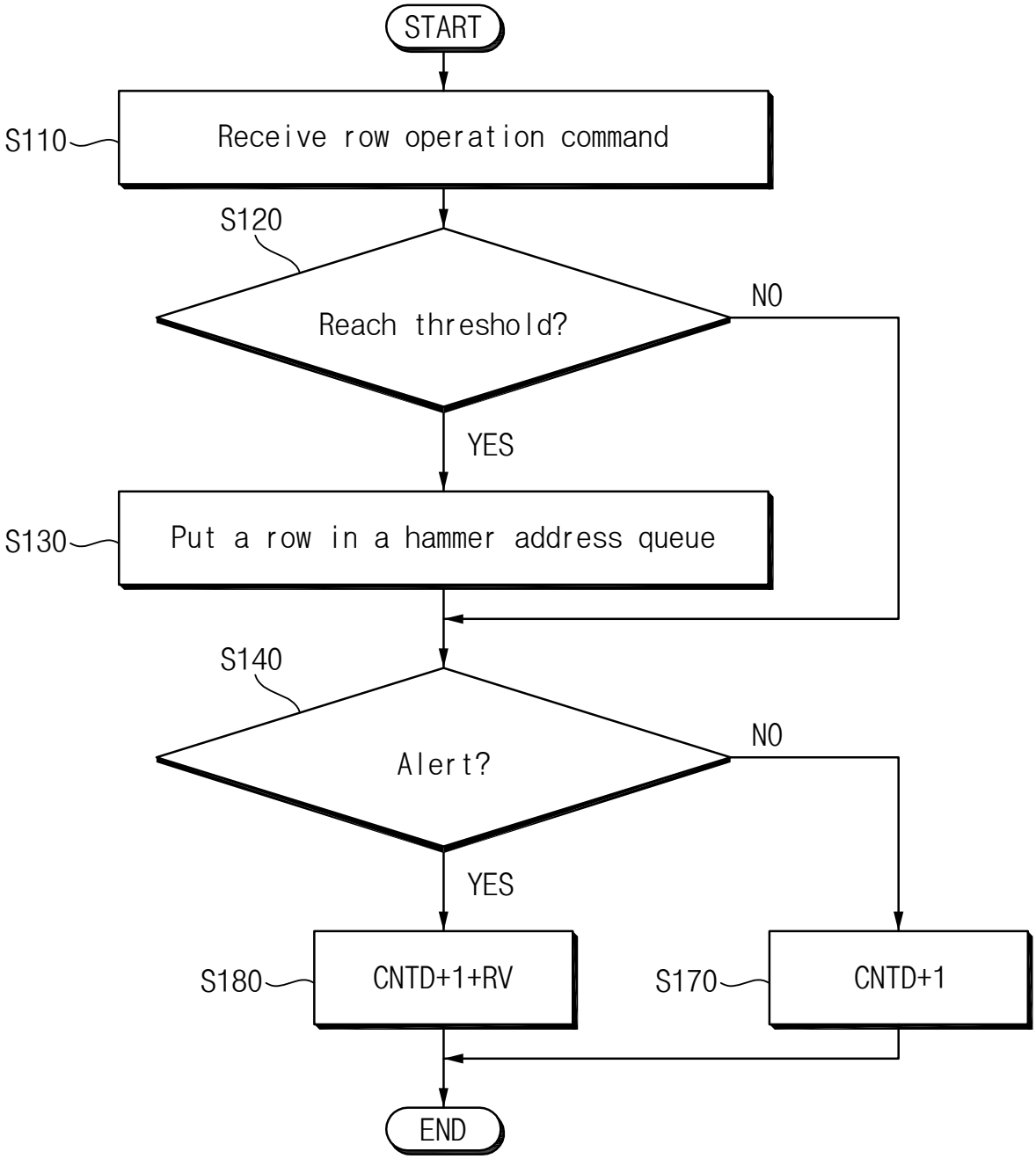

START
S110
Receive row operation command
S120
Reach threshold?
NO
YES
S130
Put a row in a hammer address queue
S140
Alert?
NO
YES
S180
CNTD+1+RV
S170
CNTD+1
END

FIG. 27

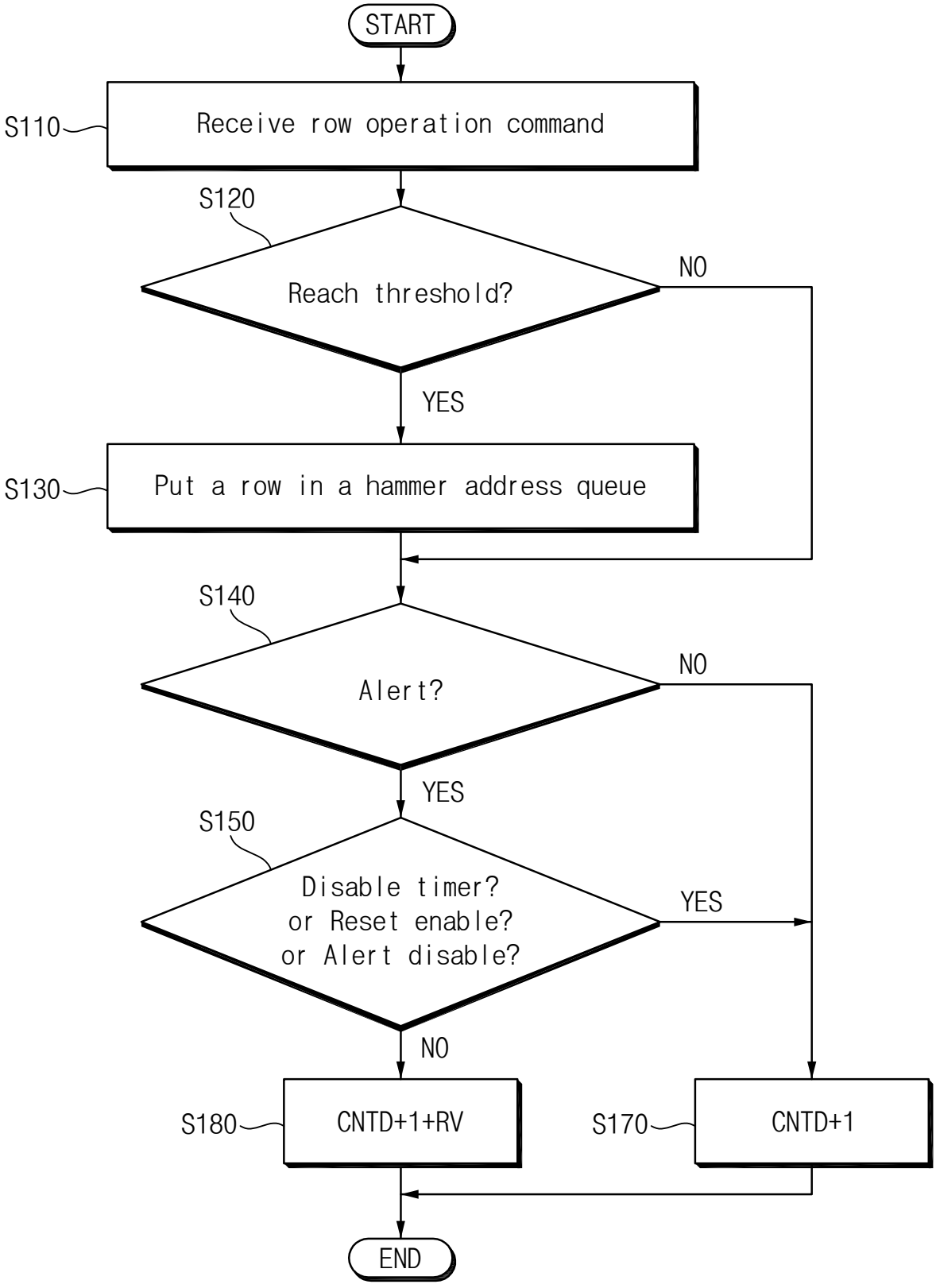

START
S110
Receive row operation command
S120
Reach threshold?
NO
YES
S130
Put a row in a hammer address queue
S140
Alert?
NO
YES
S150
Disable timer?
or Reset enable?
or Alert disable?
YES
NO
S180
CNTD+1+RV
S170
CNTD+1
END

FIG. 28

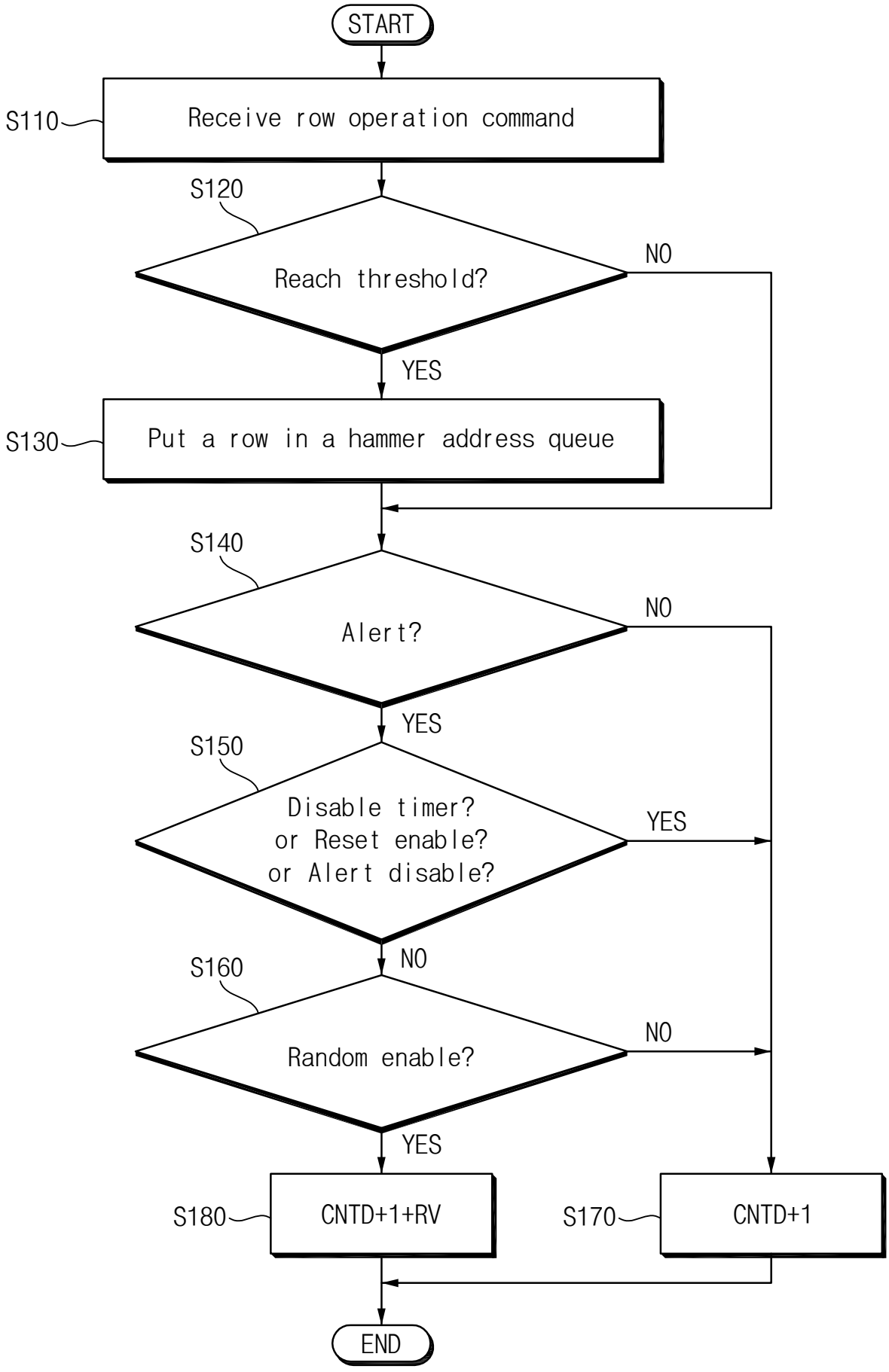

START
S110
Receive row operation command
S120
Reach threshold?
NO
YES
S130
Put a row in a hammer address queue
S140
Alert?
NO
YES
S150
Disable timer?
or Reset enable?
or Alert disable?
YES
NO
S160
Random enable?
NO
YES
S180
CNTD+1+RV
S170
CNTD+1
END

FIG. 29

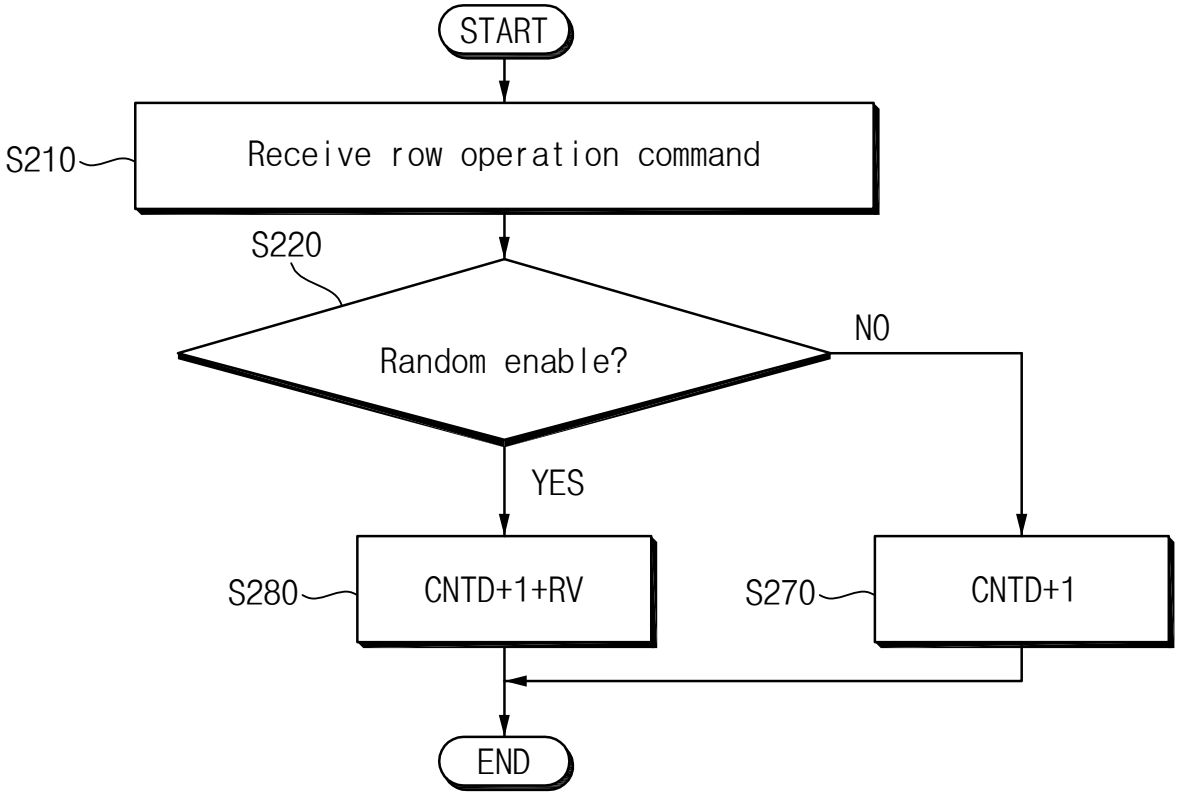

START
S210
Receive row operation command
S220
Random enable?
NO
YES
S280
CNTD+1+RV
S270
CNTD+1
END

FIG. 30

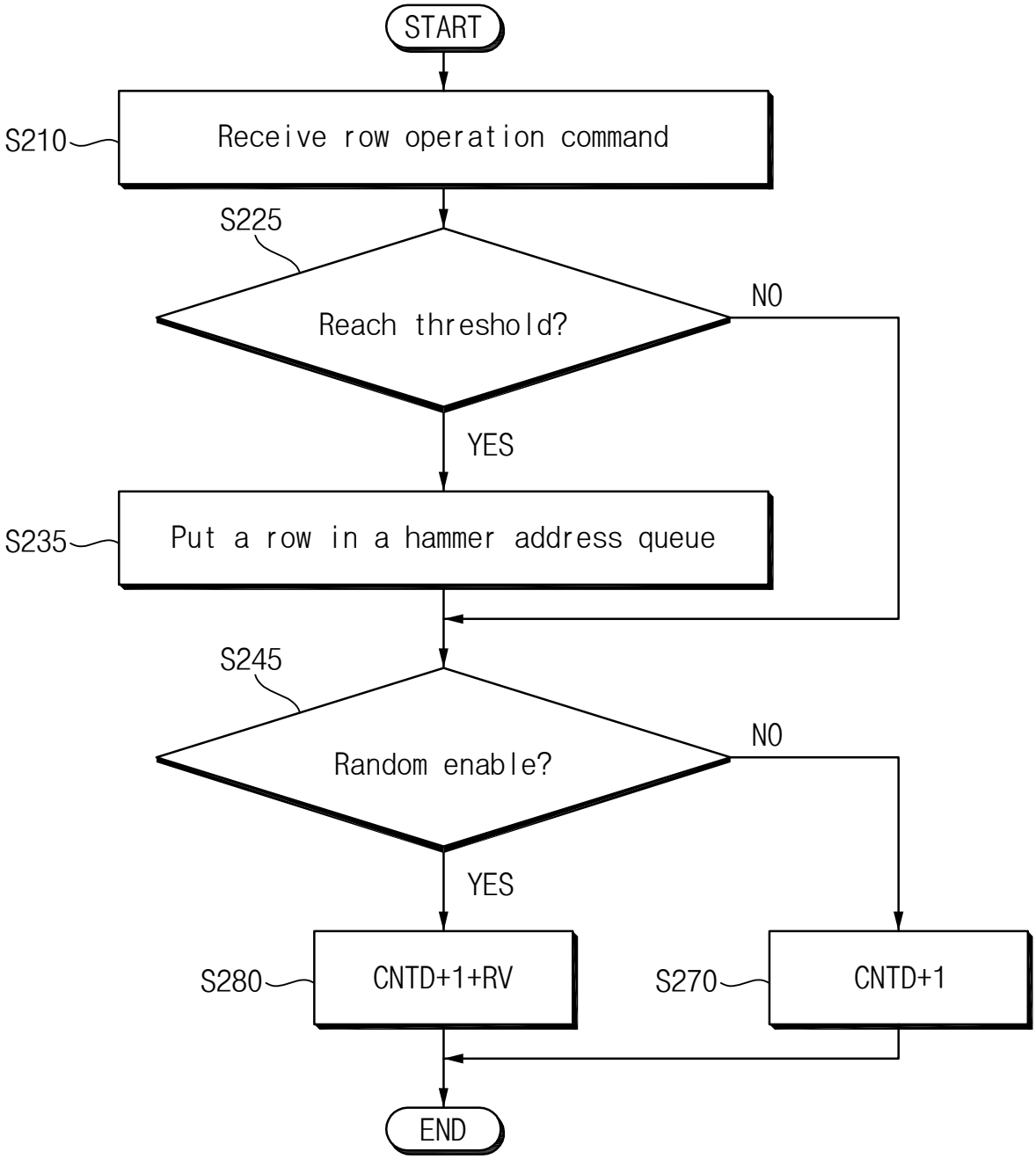

START
S210
Receive row operation command
S225
Reach threshold?
NO
YES
S235
Put a row in a hammer address queue
S245
Random enable?
NO
YES
S280
CNTD+1+RV
S270
CNTD+1
END

FIG. 31

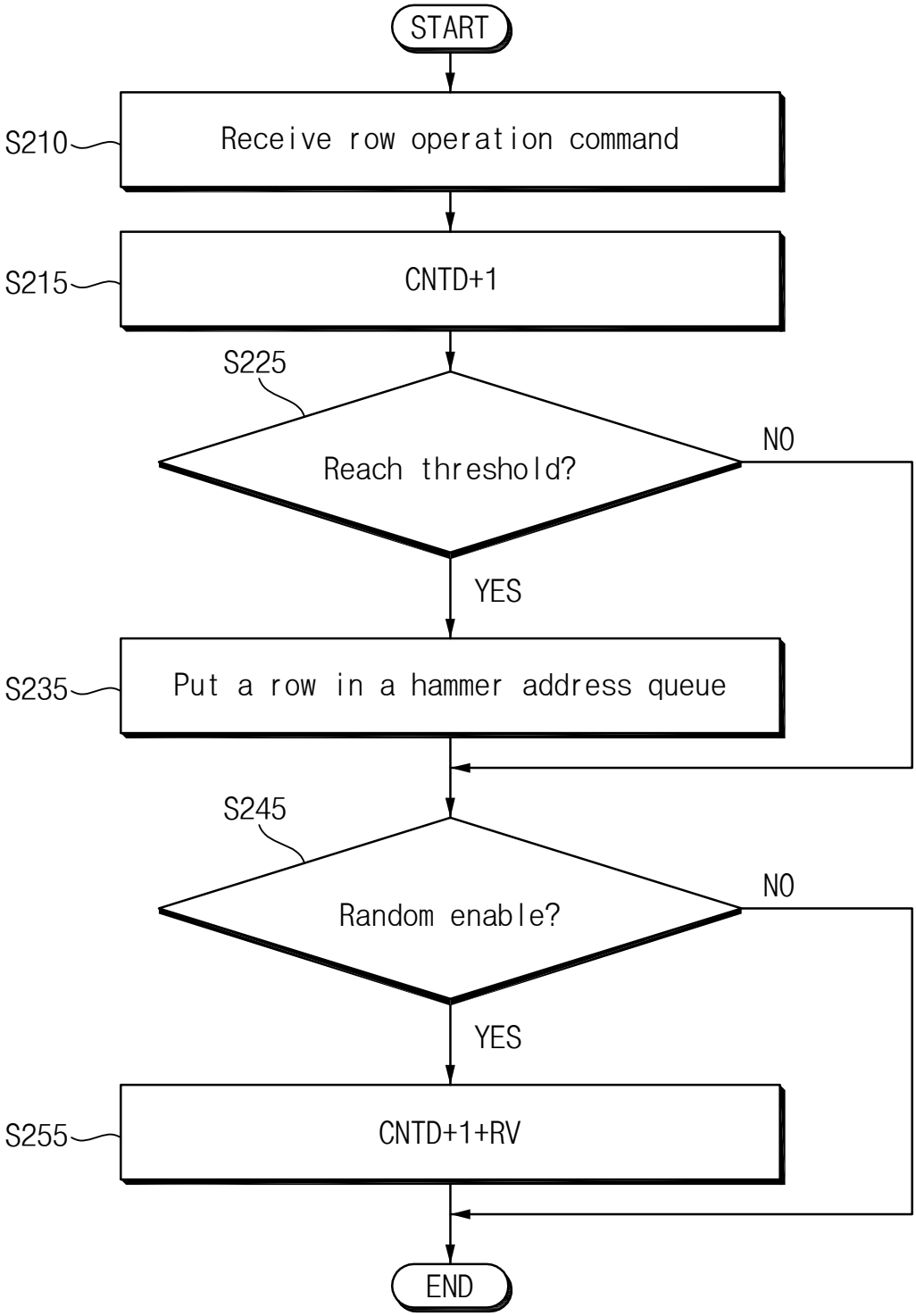

START
S210
Receive row operation command
S215
CNTD+1
S225
Reach threshold?
NO
YES
S235
Put a row in a hammer address queue
S245
Random enable?
NO
YES
S255
CNTD+1+RV
END

FIG. 32

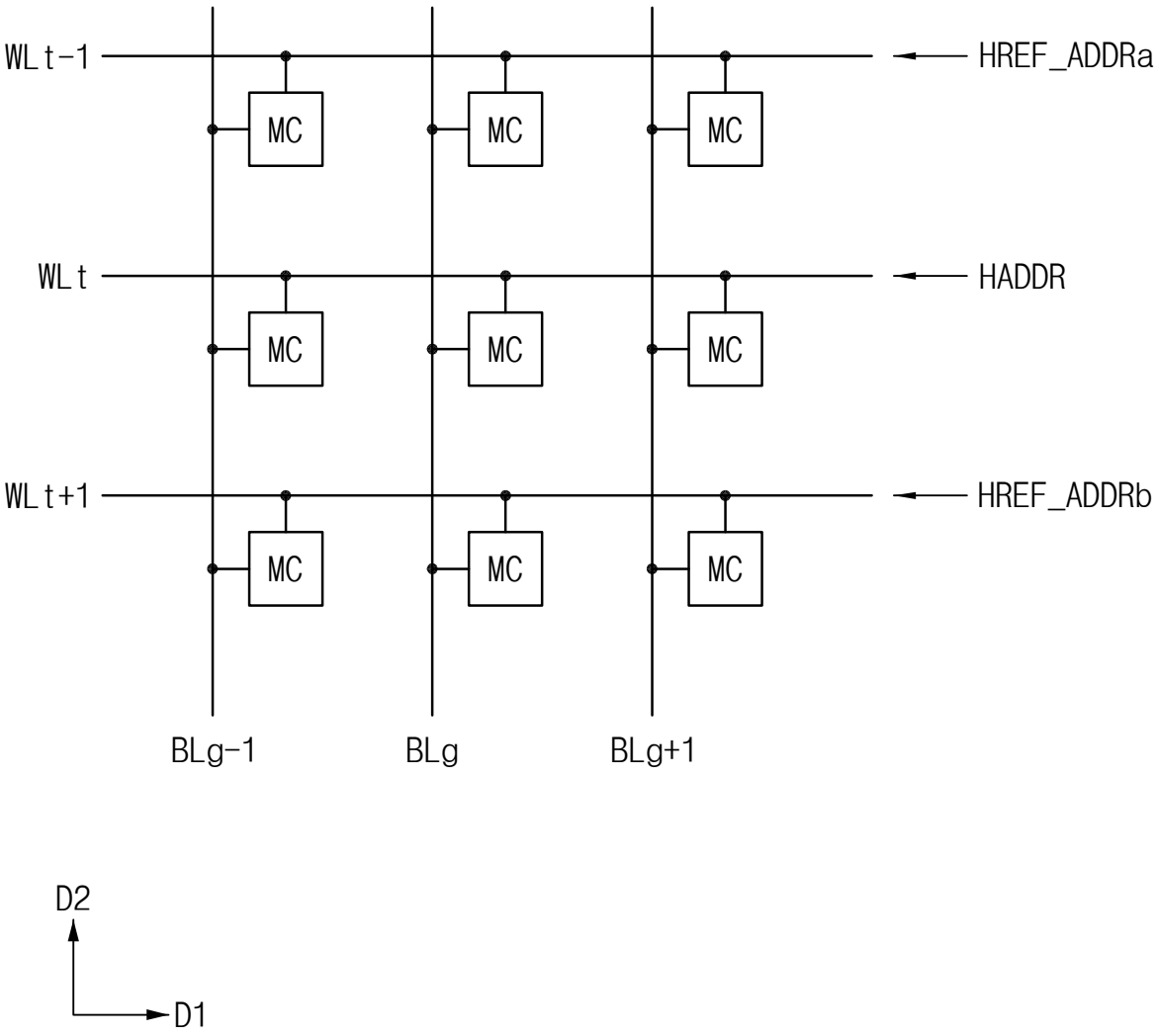

WLt-1
WLt
WLt+1
HREF_ADDRa
HADDR
HREF_ADDRb
MC
BLg-1
BLg
BLg+1
D2
D1

FIG. 33

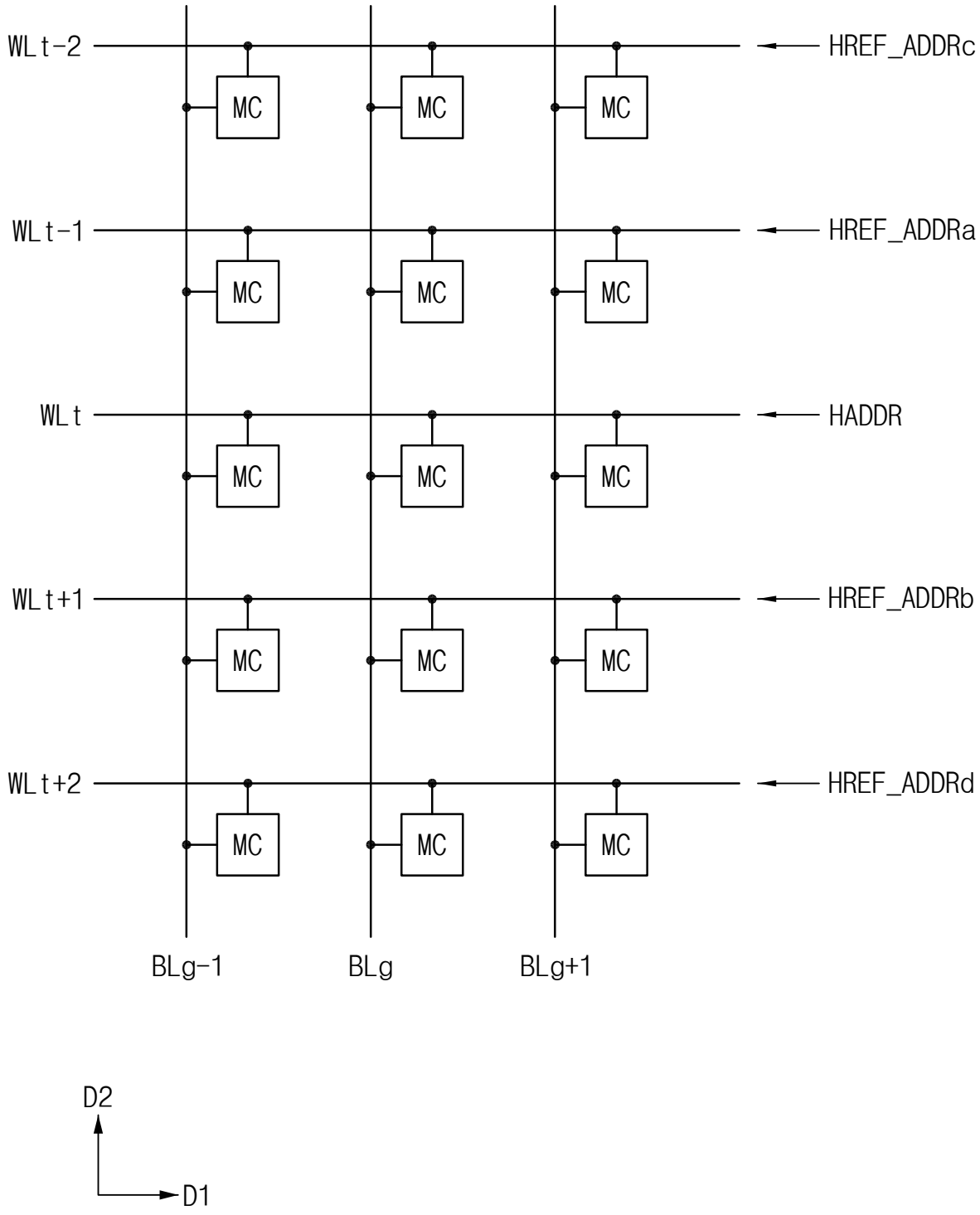

WLt-2
WLt-1
WLt
WLt+1
WLt+2
HREF_ADDRc
HREF_ADDRa
HADDR
HREF_ADDRb
HREF_ADDRd
MC
BLg-1
BLg
BLg+1
D2
D1

FIG. 34A

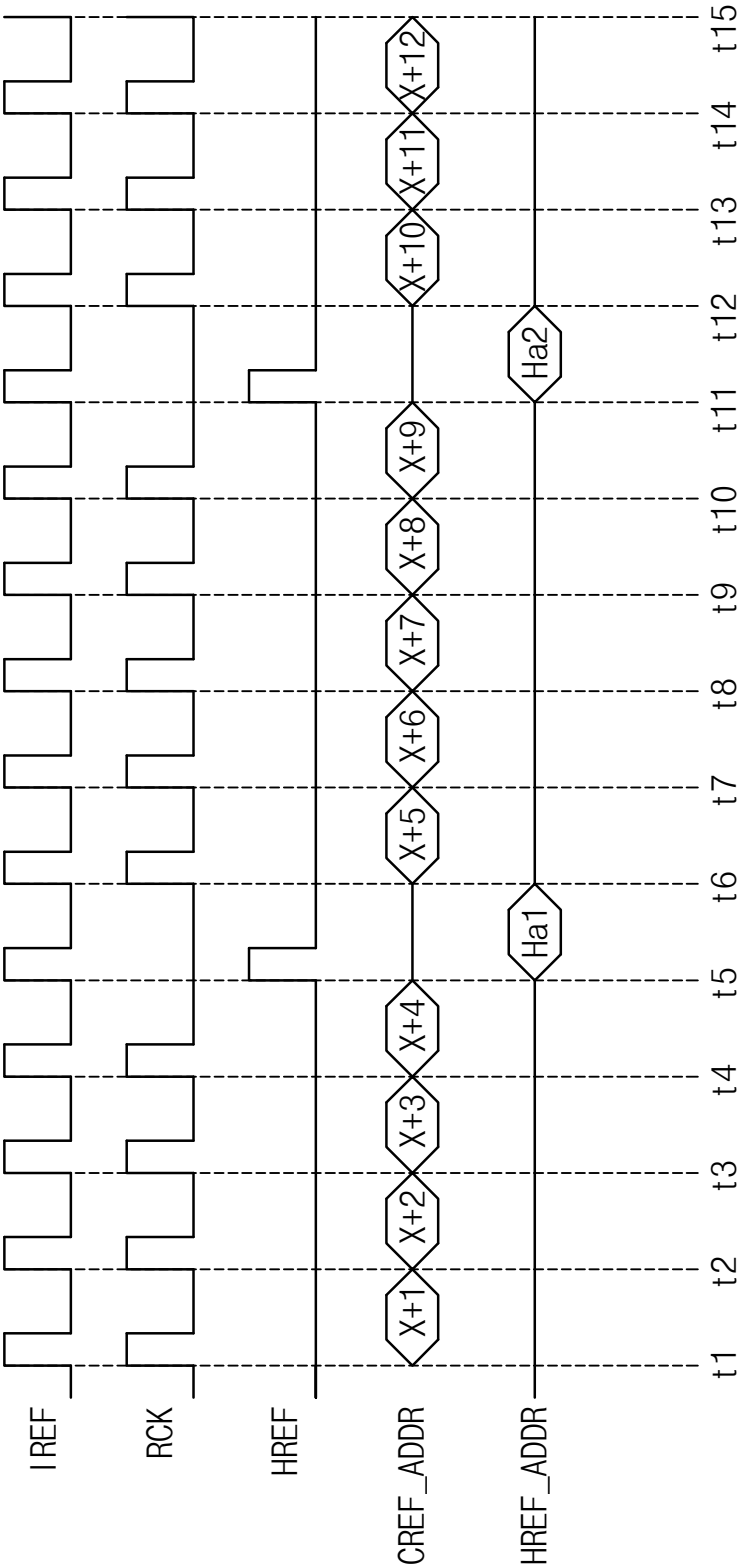

IREF
RCK
HREF
CREF_ADDR
HREF_ADDR
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10
t11
t12
t13
t14
t15
X+1
X+2
X+3
X+4
X+5
X+6
X+7
X+8
X+9
X+10
X+11
X+12
Ha1
Ha2

FIG. 34B

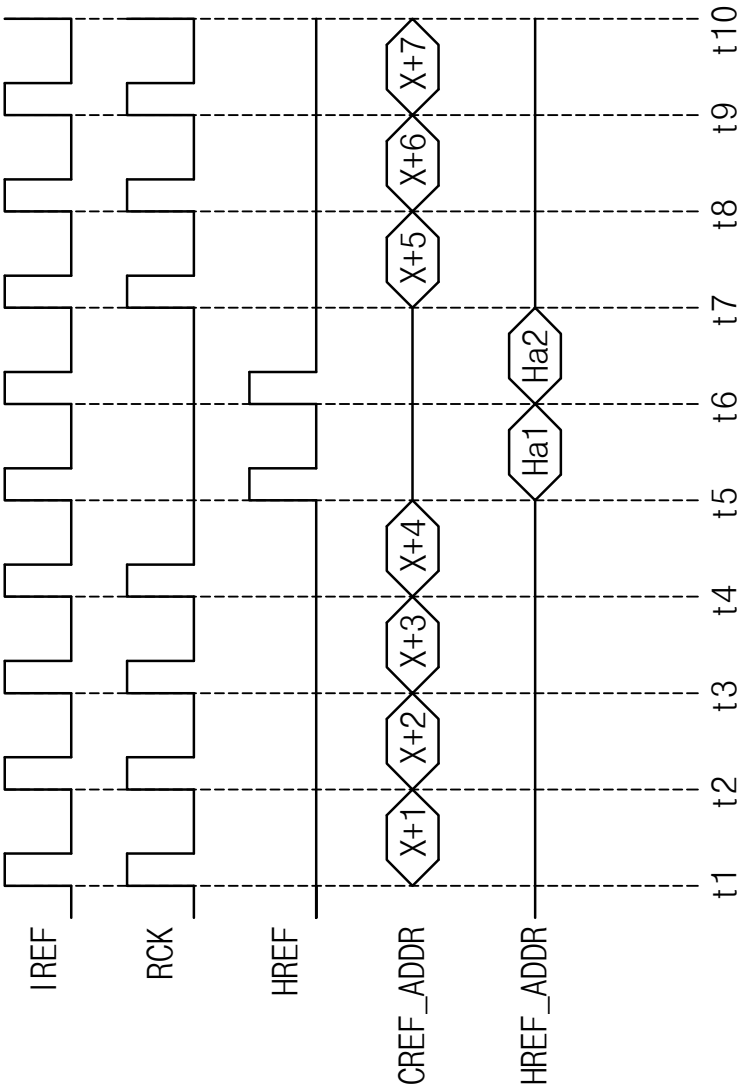

IREF
RCK
HREF
CREF_ADDR
HREF_ADDR
X+1
X+2
X+3
X+4
X+5
X+6
X+7
Ha1
Ha2
t1
t2
t3
t4
t5
t6
t7
t8
t9
t10

FIG. 35

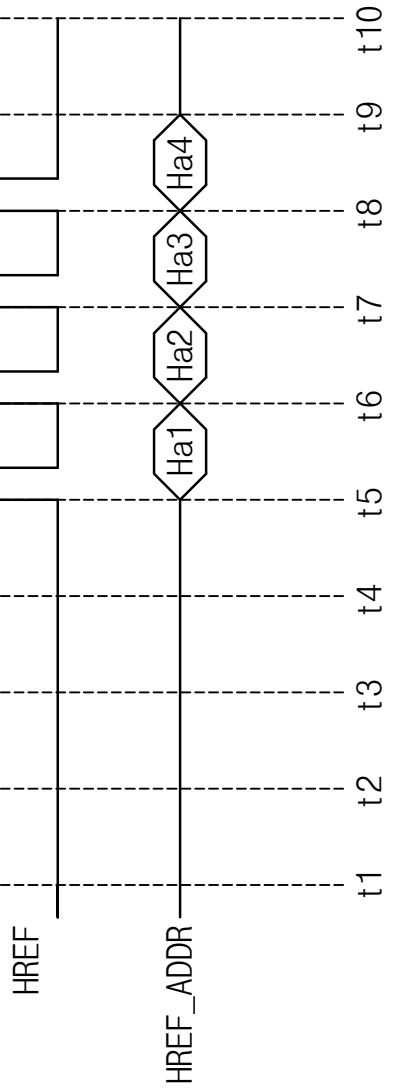


FIG. 36

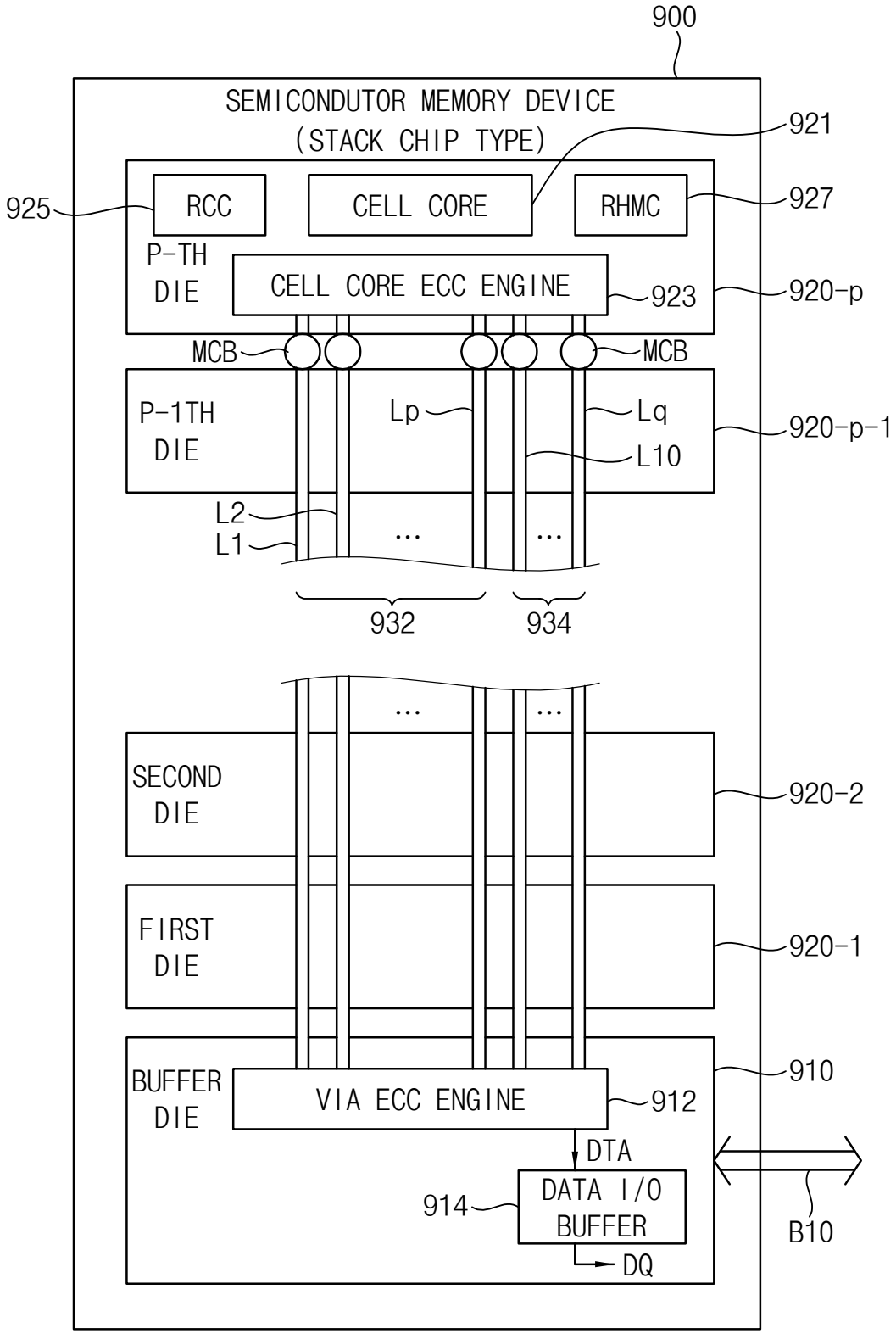

900
SEMICONDUTOR MEMORY DEVICE
(STACK CHIP TYPE)
921
925
RCC
CELL CORE
RHMC
927
P-TH
DIE
CELL CORE ECC ENGINE
923
920-p
MCB
MCB
P-1TH
DIE
Lp
Lq
L10
920-p-1
L2
L1
...
...
932
934
...
...
SECOND
DIE
920-2
FIRST
DIE
920-1
BUFFER
DIE
VIA ECC ENGINE
912
910
DTA
914
DATA I/O
BUFFER
DQ
B10

FIG. 37

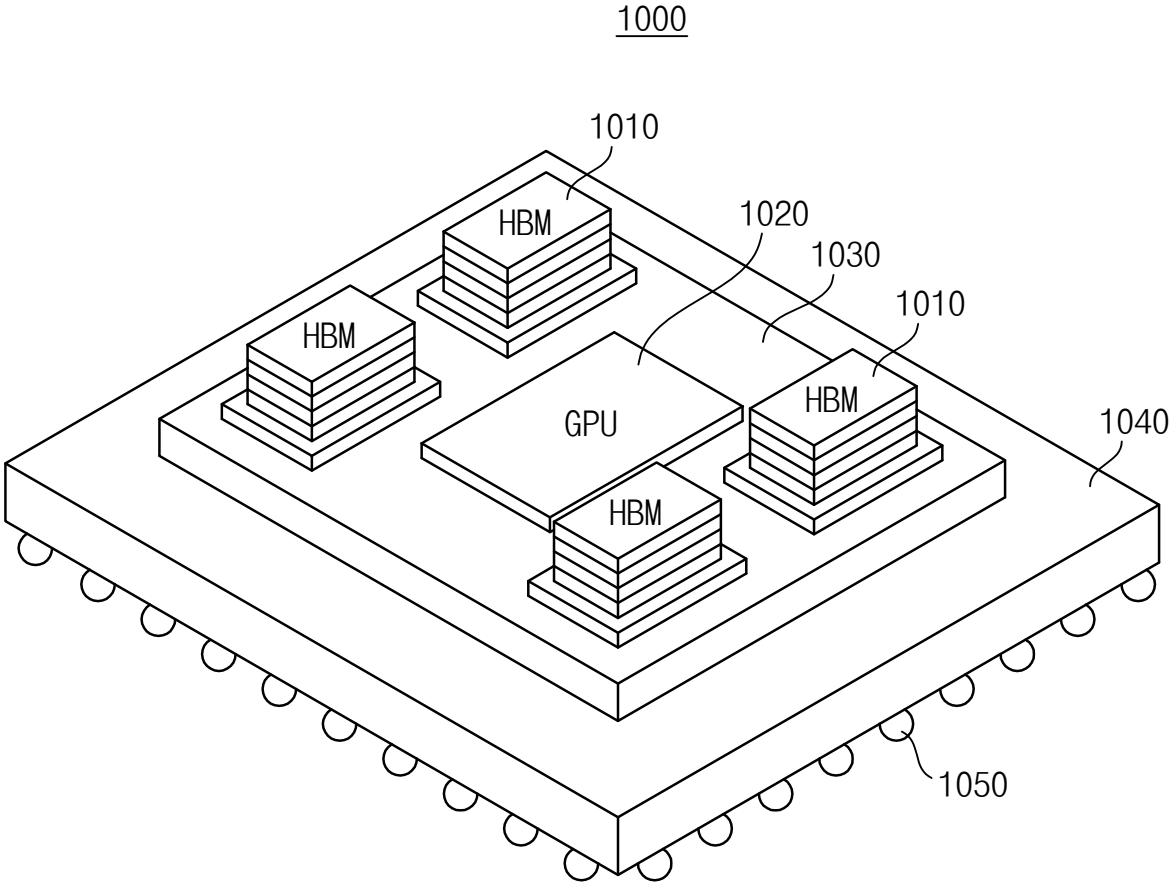
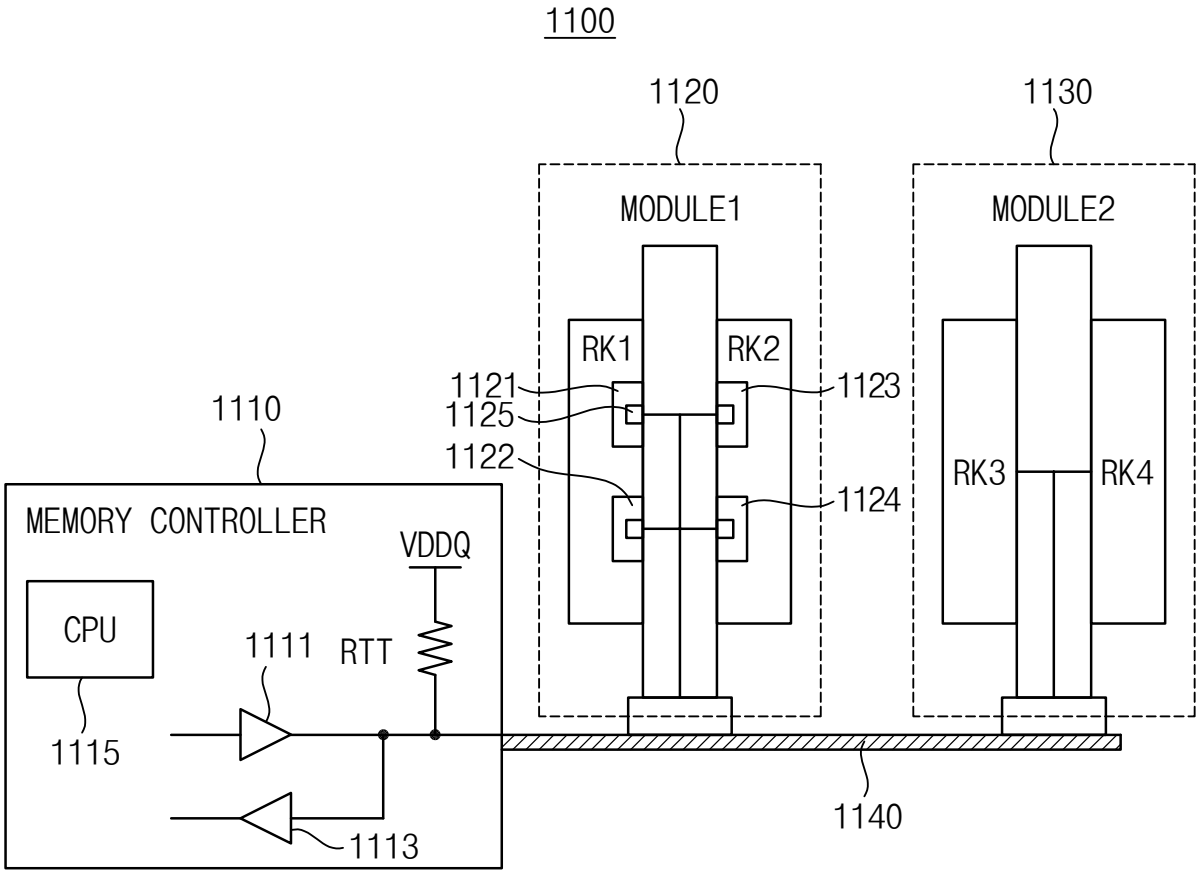


FIG. 38


1100
1120
1130
MODULE1
MODULE2
RK1
RK2
RK3
RK4
1121
1125
1122
1123
1124
1110
MEMORY CONTROLLER
VDDQ
CPU
1111
RTT
1115
1113
1140