

ABSTRACT

A memory device includes a first command address decoder configured to decode a first chip selection signal and first command address signals and generate first control signals, a second command address decoder configured to decode a second chip selection signal and second command address signals and generate second control signals during a multi-channel mode and configured to decode the second chip selection signal and the first command address signals and generate second control signals during a multi-rank mode, a first memory core including first memory cells and being controlled by the first control signals, and a second memory core including second memory cells and being controlled by the second control signals.

FIG.1